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Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

FAIRCHILD

SEMICONDUCTOR ™

October 1987
Revised January 2004

MM74C373 • MM74C374
3-STATE Octal D-Type Latch •
3-STATE Octal D-Type Flip-Flop

General Description

The MM74C373 and MM74C374 are integrated, complementary MOS (CMOS), 8-bit storage elements with 3-STATE outputs. These outputs have been specially designed to drive high capacitive loads, such as one might find when driving a bus, and to have a fan out of 1 when driving standard TTL. When a high logic level is applied to the OUTPUT DISABLE input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

The MM74C373 is an 8-bit latch. When LATCH ENABLE is high, the Q outputs will follow the D inputs. When LATCH ENABLE goes low, data at the D inputs, which meets the set-up and hold time requirements, will be retained at the outputs until LATCH ENABLE returns high again.

The MM74C374 is an 8-bit, D-type, positive-edge triggered flip-flop. Data at the D inputs, meeting the set-up and hold time requirements, is transferred to the Q outputs on positive-going transitions of the CLOCK input.

Both the MM74C373 and the MM74C374 are being assembled in 20-pin dual-in-line packages with 0.300" pin centers.

Features

- Wide supply voltage range: 3V to 15V
- High noise immunity: 0.45 V_{CC} (typ.)
- Low power consumption
- TTL compatibility:
     Fan out of 1 driving standard TTL
- Bus driving capability
- 3-STATE outputs
- Eight storage elements in one package
- Single CLOCK/LATCH ENABLE and OUTPUT DISABLE control inputs
- 20-pin dual-in-line package with 0.300" centers takes half the board space of a 24-pin package

Ordering Code:

Order Number	Package Number	Package Description
MM74C373M (Note 1)	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
MM74C373N	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
MM74C374N	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Note 1: Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

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Connection Diagrams
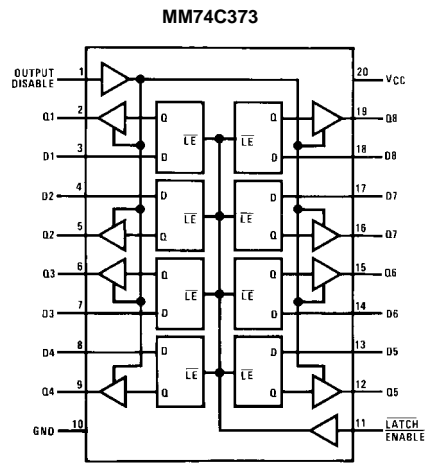
MM74C373
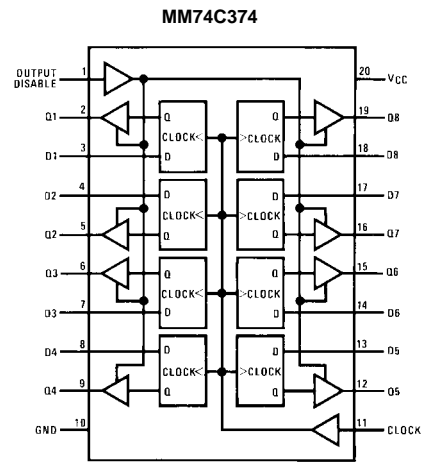
Top View

MM74C374

Top View

Truth Tables

MM74C373

Output Disable	LATCH ENABLE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q
H	X	X	Hi-Z

L = LOW logic level
H = HIGH logic level
X = Irrelevant

MM74C374

Output Disable	Clock	D	Q
L	╱	H	H
L	╱	L	L
L	L	X	Q
L	H	X	Q
H	X	X	Hi-Z

╱ = LOW-to-HIGH logic level transition
Q = Preexisting output level
Hi-Z = High impedance output state

Block Diagrams

MM74C373 (1 of 8 Latches)
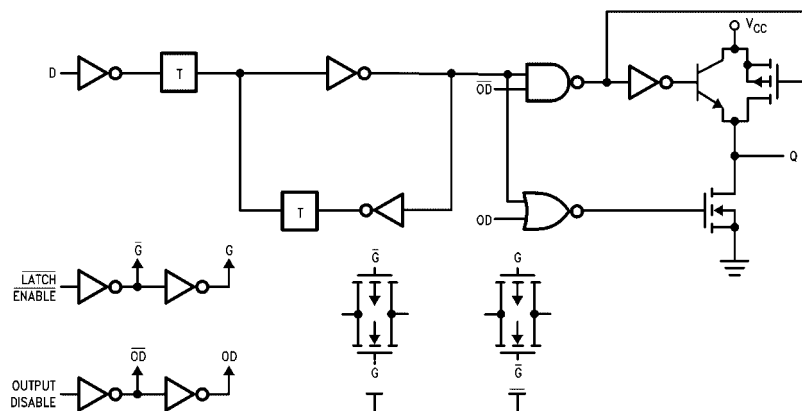
MM74C374 (1 of 8 Flip-Flops)

Absolute Maximum Ratings(Note 2)

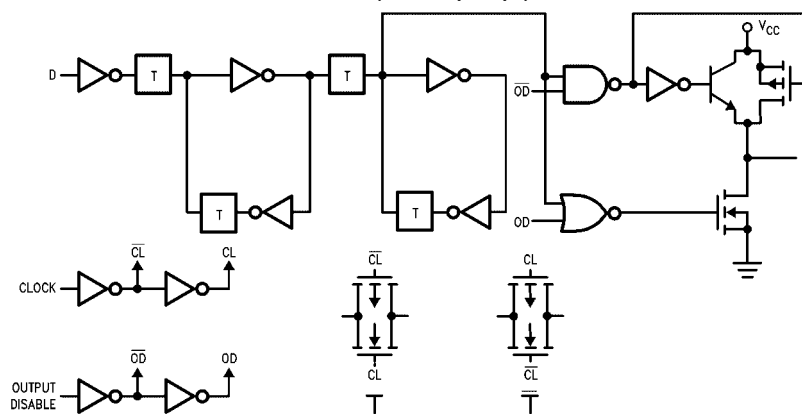|	
Voltage at Any Pin	−0.3V to V_{CC} + 0.3V
Operating Temperature Range (T_A)	
MM74C373	−55°C to +125°C
Storage Temperature Range (T_S)	−65°C to +150°C
Power Dissipation	
Dual-In-Line	700 mW
Small Outline	500 mW
Operating V_{CC} Range	3V to 15V
Absolute Maximum V_{CC}	18V
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C

Note 2: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

DC Electrical Characteristics

Min/Max limits apply across temperature range unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 5V	3.5			V
		V_{CC} = 10V	8.0			
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 5V			1.5	V
		V_{CC} = 10V			2.0	
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{CC} = 5V, I_O = −10 µA	4.5			V
		V_{CC} = 10V, I_O = −10 µA	9.0			
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = 5V, I_O = 10 µA			0.5	V
		V_{CC} = 10V, I_O = 10 µA			1.0	
$I_{IN(1)}$	Logical "1" Input Current	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	µA
$I_{IN(0)}$	Logical "0" Input Current	V_{CC} = 15V, V_{IN} = 0V	−1.0	−0.005		µA
I_{OZ}	3-STATE Leakage Current	V_{CC} = 15V, V_O = 15V		0.005	1.0	µA
		V_{CC} = 15V, V_O = 0V	−1.0	−0.005		
I_{CC}	Supply Current	V_{CC} = 15V		0.05	300	µA
CMOS/LPTTL INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 4.75V	V_{CC} − 1.5			V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 4.75V			0.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{CC} = 4.75V, I_O = −360 µA	V_{CC} − 0.4			V
		V_{CC} = 4.75V, I_O = −1.6 mA	2.4			
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = 4.75V, I_O = 1.6 mA			0.4	V
OUTPUT DRIVE (Short Circuit Current)						
I_{SOURCE}	Output Source Current	V_{CC} = 5V, V_{OUT} = 0V	−12	−24		mA
		T_A = 25°C (Note 3)				
I_{SOURCE}	Output Source Current	V_{CC} = 10V, V_{OUT} = 0V	−24	−48		mA
		T_A = 25°C (Note 3)				
I_{SINK}	Output Sink Current	V_{CC} = 5V, V_{OUT} = V_{CC}	6	12		mA
	(N-Channel)	T_A = 25°C (Note 3)				
I_{SINK}	Output Sink Current	V_{CC} = 10V, V_{OUT} = V_{CC}	24	48		mA
	(N-Channel)	T_A = 25°C (Note 3)				

Note 3: These are peak output current capabilities. Continuous output current is rated at 12 mA max.

AC Electrical Characteristics (Note 4)

MM74C373, T_A = 25°C, C_L = 50 pF, t_r = t_f = 20 ns, unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd0}, t_{pd1}	Propagation Delay, LATCH ENABLE to Output	V_{CC} = 5V, C_L = 50 pF		165	330	ns
		V_{CC} = 10V, C_L = 50 pF		70	140	
		V_{CC} = 5V, C_L = 150 pF		195	390	
		V_{CC} = 10V, C_L = 150 pF		85	170	
t_{pd0}, t_{pd1}	Propagation Delay Data In to Output	LATCH ENABLE = V_{CC}				ns
		V_{CC} = 5V, C_L = 50 pF		155	310	
		V_{CC} = 10V, C_L = 50 pF		70	140	
		V_{CC} = 5V, C_L = 150 pF		185	370	
		V_{CC} = 10V, C_L = 150 pF		85	170	
t_{SET-UP}	Minimum Set-Up Time Data In to CLOCK/LATCH ENABLE	t_{HOLD} = 0 ns				ns
		V_{CC} = 5V		70	140	
		V_{CC} = 10V		35	70	
f_{MAX}	Maximum LATCH ENABLE Frequency	V_{CC} = 5V	3.5	6.7		MHz
		V_{CC} = 10V	4.5	9.0		
t_{PWH}	Minimum LATCH ENABLE Pulse Width	V_{CC} 5V		75	150	ns
		V_{CC} = 10V		55	110	
t_r, t_f	Maximum LATCH ENABLE Rise and Fall Time	V_{CC} = 5V		NA		μs
		V_{CC} = 10V		NA		
t_{1H}, t_{0H}	Propagation Delay OUTPUT DISABLE to High Impedance State (from a Logic Level)	R_L = 10k, C_L = 5 pF				ns
		V_{CC} = 5V		105	210	
		V_{CC} = 10V		60	120	
t_{H1}, t_{H0}	Propagation Delay OUTPUT DISABLE to Logic Level (from High Impedance State)	R_L = 10k, C_L = 50 pF				ns
		V_{CC} = 5V		105	210	
		V_{CC} = 10V		45	90	
t_{THL}, t_{TLH}	Transition Time	V_{CC} = 5V, C_L = 50 pF		65	130	ns
		V_{CC} = 10V, C_L = 50 pF		35	70	
		V_{CC} = 5V, C_L = 150 pF		110	220	
		V_{CC} = 10V, C_L = 150 pF		70	140	
C_{LE}	Input Capacitance	LE Input (Note 5)		7.5	10	pF
C_{OD}	Input Capacitance	OUTPUT DISABLE Input (Note 5)		7.5	10	pF
C_{IN}	Input Capacitance	Any Other Input (Note 5)		5	7.5	pF
C_{OUT}	Output Capacitance	High Impedance State (Note 5)		10	15	pF
C_{PD}	Power Dissipation Capacitance	Per Package (Note 6)		200		pF

Note 4: AC Parameters are guaranteed by DC correlated testing.

Note 5: Capacitance is guaranteed by periodic testing.

Note 6: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see Family Characteristics Application Note AN-90.

AC Electrical Characteristics (Note 7)

MM74C374, $T_A = 25°C$, $C_L = 50$ pF, $t_r = t_f = 20$ ns, unless otherwise noted

| Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd0}, t_{pd1}	Propagation Delay, CLOCK to Output	$V_{CC} = 5V$, $C_L = 50$ pF		150	300	ns
		$V_{CC} = 10V$, $C_L = 50$ pF		65	130	
		$V_{CC} = 5V$, $C_L = 150$ pF		180	360	
		$V_{CC} = 10V$, $C_L = 150$ pF		80	160	
t_{SET-UP}	Minimum Set-Up Time Data In to CLOCK/$\overline{\text{LATCH ENABLE}}$	$t_{HOLD} = 0$ ns				ns
		$V_{CC} = 5V$		70	140	
		$V_{CC} = 10V$		35	70	
t_{PWH}, t_{PWL}	Minimum CLOCK Pulse Width	$V_{CC} = 5V$		70	140	ns
		$V_{CC} = 10V$		50	100	
f_{MAX}	Maximum CLOCK Frequency	$V_{CC} = 5V$	3.5	7.0		MHz
		$V_{CC} = 10V$	5	10		
t_{1H}, t_{0H}	Propagation Delay OUTPUT DISABLE to High Impedance State (from a Logic Level)	$R_L = 10k$, $C_L = 50$ pF				ns
		$V_{CC} = 5V$		105	210	
		$V_{CC} = 10V$		60	120	
t_{H1}, t_{H0}	Propagation Delay OUTPUT DISABLE to Logic Level (from High Impedance State)	$R_L = 10k$, $C_L = 50$ pF				ns
		$V_{CC} = 5V$		105	210	
		$V_{CC} = 10V$		45	90	
t_{THL}, t_{TLH}	Transition Time	$V_{CC} = 5V$, $C_L = 50$ pF		65	130	ns
		$V_{CC} = 10V$, $C_L = 50$ pF		35	70	
		$V_{CC} = 5V$, $C_L = 150$ pF		110	220	
		$V_{CC} = 10V$, $C_L = 150$ pF		70	140	
t_r, t_f	Maximum CLOCK Rise and Fall Time	$V_{CC} = 5V$	15	>2000		μs
		$V_{CC} = 10V$	5	>2000		
C_{CLK}	Input Capacitance	CLOCK Input (Note 8)		7.5	10	pF
C_{OD}	Input Capacitance	OUTPUT DISABLE Input (Note 8)		7.5	10	pF
C_{IN}	Input Capacitance	Any Other Input (Note 8)		5	7.5	pF
C_{OUT}	Output Capacitance	High Impedance State (Note 8)		10	15	pF
C_{PD}	Power Dissipation Capacitance	Per Package (Note 9)		250		pF

Note 7: AC Parameters are guaranteed by DC correlated testing.

Note 8: Capacitance is guaranteed by periodic testing.

Note 9: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see Family Characteristics Application Note AN-90.
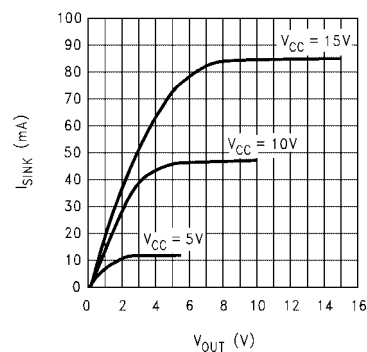
Typical Performance Characteristics

MM74C373
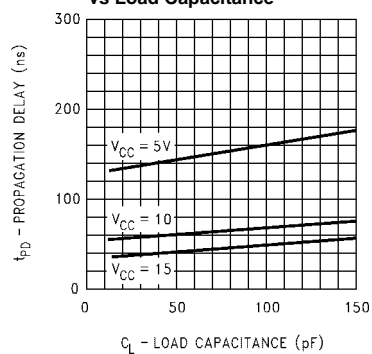**Propagation Delay, LATCH ENABLE to Output**
vs Load Capacitance

MM74C373, MM74C374
Change in Propagation Delay
per pF of Load Capacitance
(Δt_{PD}/pF) vs Power Supply Voltage
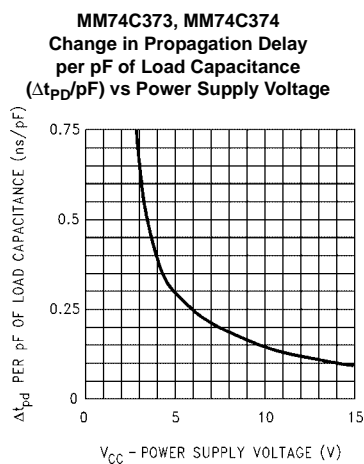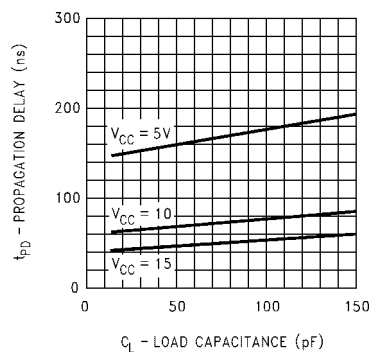
MM74C373
Propagation Delay, Data In to Output
vs Load Capacitance
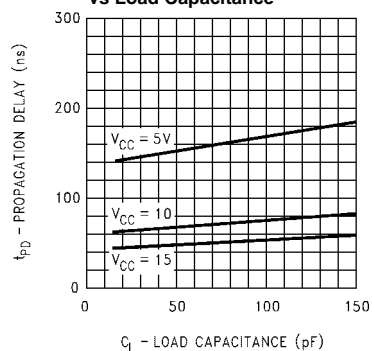
MM74C373, MM74C374
Output Sink Current vs V_{OUT}
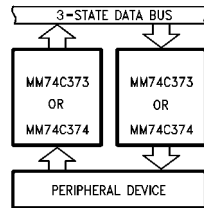

MM74C373
Propagation Delay, CLOCK to Output
vs Load Capacitance

MM74C373, MM74C374
Source Current vs $V_{CC} - V_{OUT}$
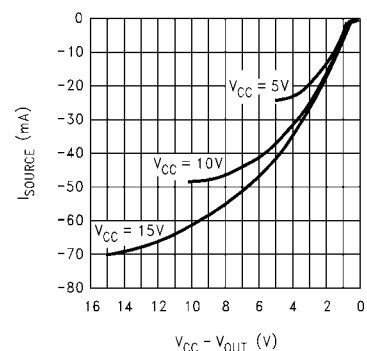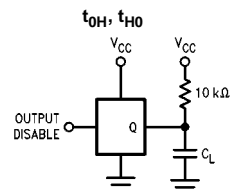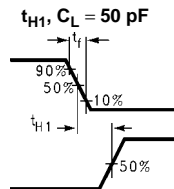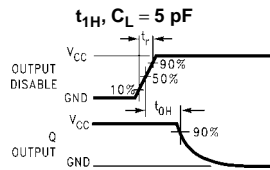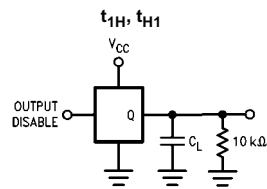
Typical Applications

Data Bus Interfacing Element

**Simple, Latching, Octal, LED Indicator
Driver with Blanking for Use as Data Display,
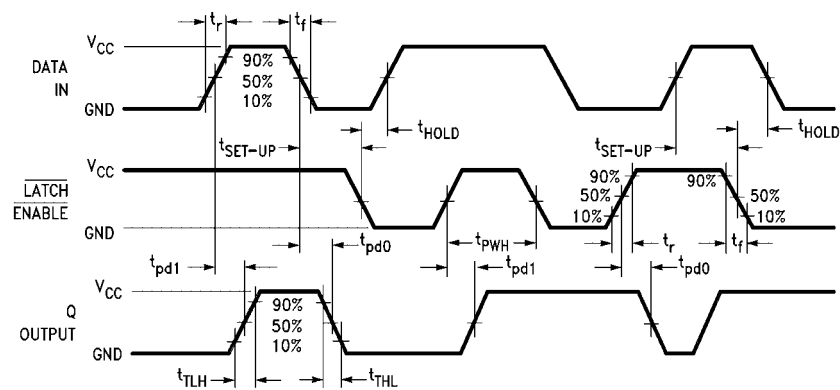Bus Monitor, μP Front Panel Display, Etc.**
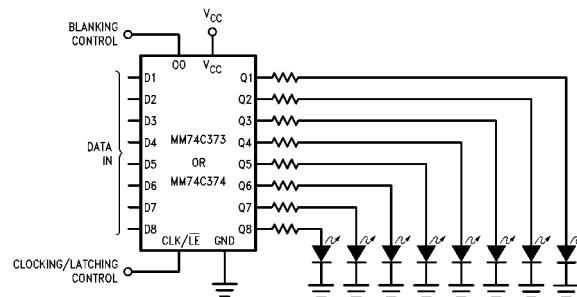
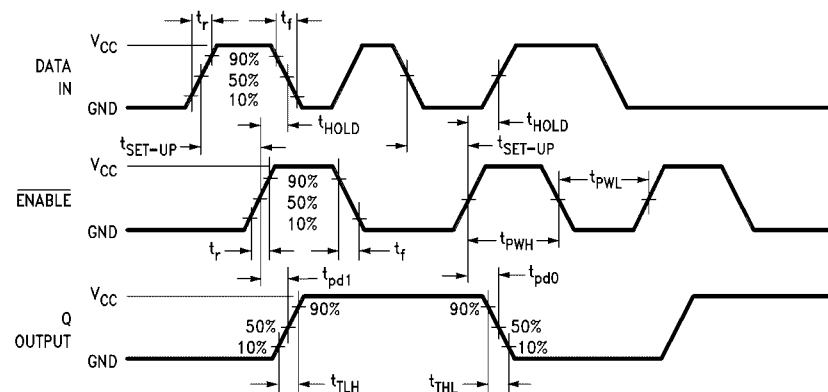# 3-STATE Test Circuits and Switching Time Waveforms

t_{1H}, t_{H1}

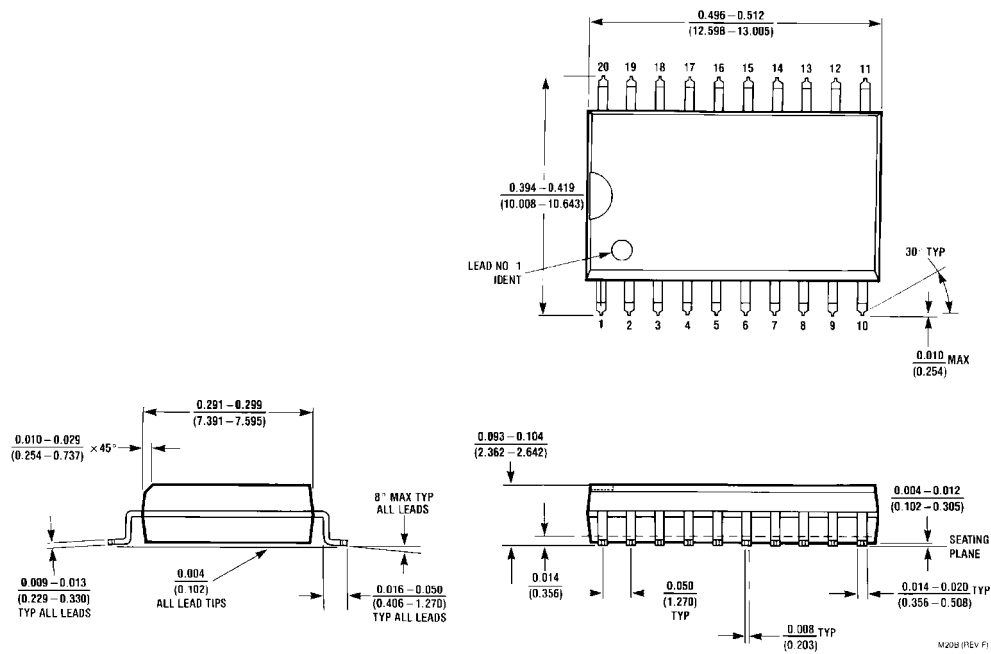t_{1H}, $C_L = 5$ pF

t_{H1}, $C_L = 50$ pF

t_{0H}, t_{H0}

t_{0H}, $C_L = 5$ pF

t_{H0}, $C_L = 50$ pF

8
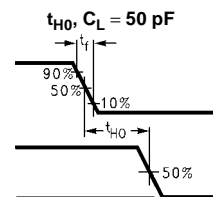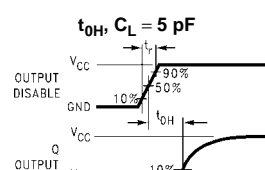
Switching Time Waveforms

MM74C373

Output Disable = GND

MM74C374

Output Disable = GND

Physical Dimensions inches (millimeters) unless otherwise noted

0.496 – 0.512
(12.598 – 13.005)

20 19 18 17 16 15 14 13 12 11

0.394 – 0.419
(10.008 – 10.643)

LEAD NO. 1
IDENT

1   2   3   4   5   6   7   8   9   10

30° TYP

0.010 MAX
(0.254)

0.291 – 0.299
(7.391 – 7.595)

0.010 – 0.029
(0.254 – 0.737) × 45°

8° MAX TYP
ALL LEADS

0.009 – 0.013
(0.229 – 0.330)
TYP ALL LEADS

0.004
(0.102)
ALL LEAD TIPS

0.016 – 0.050
(0.406 – 1.270)
TYP ALL LEADS

0.093 – 0.104
(2.362 – 2.642)

0.004 – 0.012
(0.102 – 0.305)

SEATING
PLANE

0.014
(0.356)

0.050
(1.270)
TYP

0.008 TYP
(0.203)

0.014 – 0.020 TYP
(0.356 – 0.508)

M20B (REV F)

20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
Package Number M20B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N20A

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