



High-Speed, Low r_{ON} , 1.8-V/2.5-V/3.3-V/5-V, SPST Analog Switch (1-Bit Bus Switch)

DESCRIPTION

The DG2303 is a high-speed, 1-bit, low power, TTL-compatible bus switch. Using sub-micron CMOS technology, DG2303 achieves low on-resistance and negligible propagation delay.

The DG2303 consist of a bi-directional input/output pins A and B. When the output enable (OE) is low, the input/output pins are connected. When the OE is high, the switch is open and a high-impedance state exists between input/output pins A and B.

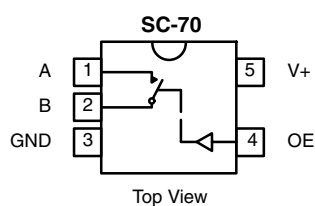
FEATURES

- SC-70 5-Lead Package
- $5\ \Omega$ Switch Connection Between Two Ports
- Minimal Propagation Delay Through The Switch
- Low I_{CC}
- Zero Bounce In Flow-Through Mode
- Control Inputs Compatible with TTL Level



Available
RoHS*
COMPLIANT

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



Device Marking: E6

TRUTH TABLE

| OE | B | Function |
|----|-----------|------------|
| L | HiZ State | Disconnect |
| H | A | Connect |

ORDERING INFORMATION

| Temp Range | Package | Part Number |
|---------------|---------|-------------------------------|
| - 40 to 85 °C | SC70-5 | DG2303DL-T1 DG2303DL-T1-E3 |

* Pb containing terminations are not RoHS compliant, exemptions may apply



| ABSOLUTE MAXIMUM RATINGS | | | |
|--|-------------------------|-----------------------|------|
| Parameter | | Limit | Unit |
| Reference V+ to GND | | - 0.3 to + 6 V | V |
| OE, A, B ^a | | - 0.3 to (V+ + 0.3 V) | |
| Continuous Current (Any Terminal) | | ± 50 | mA |
| Peak Current (Pulsed at 1 ms, 10 % duty cycle) | | ± 200 | |
| Storage Temperature (D Suffix) | | - 65 to 150 | °C |
| Power Dissipation (Packages) ^b | 5-Pin SC70 ^c | 250 | mW |

Notes:

a. Signals on A, or B or OE exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.

b. All leads welded or soldered to PC Board.

c. Derate 3.1 mW/°C above 70 °C.

| SPECIFICATIONS (V+ = 5.0 V) | | | | | | | |
|---------------------------------------|------------------------------------|--|-------------------|-------------------------|------------------|------------------|------|
| Parameter | Symbol | Test Conditions Otherwise Unless Specified V+ = 1.65 V to 5.5 V, V _{IN} = V _{IH} or V _{IL} ^e | Temp ^a | Limits - 40 to 85 °C | | | Unit |
| | | | | Min ^b | Typ ^c | Max ^b | |
| DC Characteristics | | | | | | | |
| On-Resistance | r _{ON} | V+ = 1.8 V, V _A = 0 V, I _B = 4 mA | Full | | | 28.0 | Ω |
| | | V+ = 1.8 V, V _A = 1.8 V, I _B = 4 mA | Full | | | 60.0 | |
| | | V+ = 2.3 V, V _A = 0 V, I _B = 8 mA | Full | | | 12.0 | |
| | | V+ = 2.3 V, V _A = 2.3 V, I _B = 8 mA | Full | | | 30.0 | |
| | | V+ = 3.0 V, V _A = 0 V, I _B = 24 mA | Full | | | 9.0 | |
| | | V+ = 3.0 V, V _A = 3.0 V, I _B = 24 mA | Full | | | 20.0 | |
| | | V+ = 4.5 V, V _A = 0 V, I _B = 30 mA | Full | | | 7.0 | |
| | | V+ = 4.5 V, V _A = 2.4 V, I _B = 15 mA | Full | | | 12.0 | |
| | | V+ = 4.5 V, V _A = 4.5 V, I _B = 30 mA | Full | | | 15.0 | |
| r _{ON} Flatness ^d | r _{ON} Flatness | V+ = 1.8 V, V _A = 0 V to V+, I _B = 4 mA | Full | | 125 | | |
| | | V+ = 2.5 V, V _A = 0 V to V+, I _B = 8 mA | Full | | 28 | | |
| | | V+ = 3.3 V, V _A = 0 V to V+, I _B = 24 mA | Full | | 12 | | |
| | | V+ = 5.0 V, V _A = 0 V to V+, I _B = 30 mA | Full | | 6 | | |
| Switch Off Leakage Current | I _(off) | V+ = 5.5 V, V _A = 1 V/4.5 V, V _B = 4.5 V/1 V | Full | - 10 | | 10 | μA |
| Switch-On Leakage Current | I _(on) | V+ = 5.5 V, V _A = V _B = 1 V/4.5 V | Full | - 10 | | 10 | |
| Input High Voltage | V _{IH} | V+ = 1.65 V to 1.95 V | Full | 1.35 | | | V |
| | | V+ = 2.3 V to 2.7 V | Full | 1.6 | | | |
| | | V+ = 3.0 V to 3.6 V | Full | 2.0 | | | |
| | | V+ = 4.5 V to 5.5 V | Full | 2.4 | | | |
| Input Low Voltage | V _{IL} | V+ = 1.65 V to 1.95 V | Full | | | 0.4 | |
| | | V+ = 2.3 V to 2.7 V | Full | | | 0.4 | |
| | | V+ = 3.0 V to 3.6 V | Full | | | 0.6 | |
| | | V+ = 4.5 V to 5.5 V | Full | | | 0.8 | |
| Input Current | I _{IL} or I _{IH} | V _{OE} = 0 or V+ | Full | - 1 | | 1 | μA |



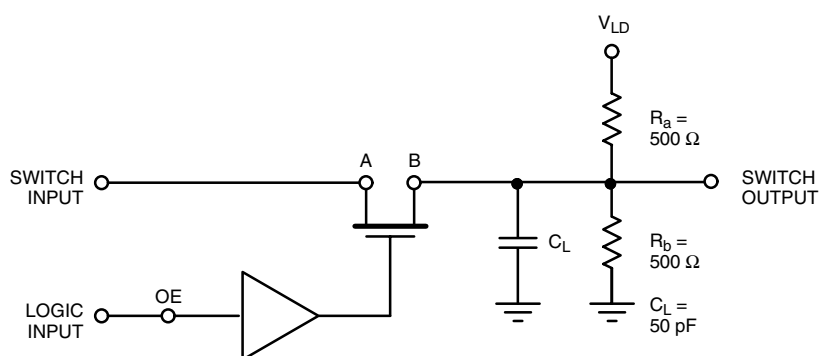
| SPECIFICATIONS | | | | | | | |
|--------------------------------------|------------|--|-------------------|-------------------------|------------------|------------------|------|
| Parameter | Symbol | Test Conditions Otherwise Unless Specified V+ = 1.65 V to 5.5 V, VIN = VIH or VIL ^e | Temp ^a | Limits - 40 to 85 °C | | | Unit |
| | | | | Min ^b | Typ ^c | Max ^b | |
| Dynamic Characteristics | | | | | | | |
| Prop Delay Bus-to-Bus ^f | tPHL, tPLH | VLD = Open, V = 1.65 V to 1.95 V, (Figure 1 and 2) | Full | | | 5 | ns |
| | | VLD = Open, V = 2.3 V to 2.7 V, (Figure 1 and 2) | Full | | | 2 | |
| | | VLD = Open, V = 3.0 V to 3.6 V, (Figure 1 and 2) | Full | | | 1 | |
| | | VLD = Open, V = 4.5 V to 5.5 V, (Figure 1 and 2) | Full | | | 1 | |
| Output Enable Time ^d | tPZL | VLD = 2 x V+, V+ = 1.65 V to 1.95 V (Figure 1 and 2) | Full | | 4.2 | | |
| | | VLD = 2 x V+, V+ = 2.3 V to 2.7 V (Figure 1 and 2) | Full | | 3.3 | | |
| | | VLD = 2 x V+, V+ = 3.0 V to 3.6 V (Figure 1 and 2) | Full | | 2.6 | | |
| | | VLD = 2 x V+, V+ = 4.5 V to 5.5 V (Figure 1 and 2) | Full | | 1.8 | | |
| | tPZH | VLD = 0 V, V+ = 1.65 V to 1.95 V (Figure 1 and 2) | Full | | 4.4 | | |
| | | VLD = 0 V, V+ = 2.3 V to 2.7 V (Figure 1 and 2) | Full | | 3.3 | | |
| | | VLD = 0 V, V+ = 3.0 V to 3.6 V (Figure 1 and 2) | Full | | 2.7 | | |
| | | VLD = 0 V, V+ = 4.5 V to 5.5 V (Figure 1 and 2) | Full | | 2.0 | | |
| Output Disable Time ^d | tPLZ | VLD = 2 x V+, V+ = 1.65 V to 1.95 V (Figure 1 and 2) | Full | | 14.3 | | |
| | | VLD = 2 x V+, V+ = 2.3 V to 2.7 V (Figure 1 and 2) | Full | | 10.5 | | |
| | | VLD = 2 x V+, V+ = 3.0 V to 3.6 V (Figure 1 and 2) | Full | | 8.6 | | |
| | | VLD = 2 x V+, V+ = 4.5 V to 5.5 V (Figure 1 and 2) | Full | | 7.4 | | |
| | tPHZ | VLD = 0 V, V+ = 1.65 V to 1.95 V (Figure 1 and 2) | Full | | 10.7 | | |
| | | VLD = 0 V, V+ = 2.3 V to 2.7 V (Figure 1 and 2) | Full | | 9.6 | | |
| | | VLD = 0 V, V+ = 3.0 V to 3.6 V (Figure 1 and 2) | Full | | 8.7 | | |
| | | VLD = 0 V, V+ = 4.5 V to 5.5 V (Figure 1 and 2) | Full | | 7.5 | | |
| Charge Injection ^d | QINJ | CL = 1 nF, VGEN = 0 V, RGEN = 0 Ω, (Figure 3) | Room | | 0.5 | | pC |
| Off Isolation ^d | OIRR | RL = 50 Ω, CL = 5 pF, f = 10 MHz | Room | | - 50 | | dB |
| Insertion Loss ^d | Loss | RL = 50 Ω | Room | | > 200 | | MHz |
| Input Capacitance ^d | Cin | | Room | | 4 | | pF |
| Channel-Off Capacitance ^d | C(off) | VOE = 0 or V+, f = 1 MHz | Room | | 9 | | |
| Channel-On Capacitance ^d | CON | | Room | | 20 | | |
| Power Supply | | | | | | | |
| Power Supply Range | V+ | | | 1.65 | | 5.5 | V |
| Power Supply Current | I+ | VOE = 0 or V+ | | | | 1.0 | μA |

Notes:

- Room = 25 °C, Full = as determined by the operating suffix.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Typical values are for design aid only, not guaranteed nor subject to production testing.
- Guarantee by design, nor subjected to production test.
- V_{IN} = input voltage to perform proper function.
- Guaranteed by design and not production tested. The bus switch propagation delay is a function of the RC time constant contributed by the on-resistance and the specified load capacitance with an ideal voltage source (zero output impedance) driving the switch.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

AC LOADING AND WAVEFORMS



Input driven by 50 Ω source terminated in 50 Ω
 C_L includes load and stray capacitance
 Input PRR = 1.0 MHz, t_W = 50 ns

Figure 1. AC Test Circuit

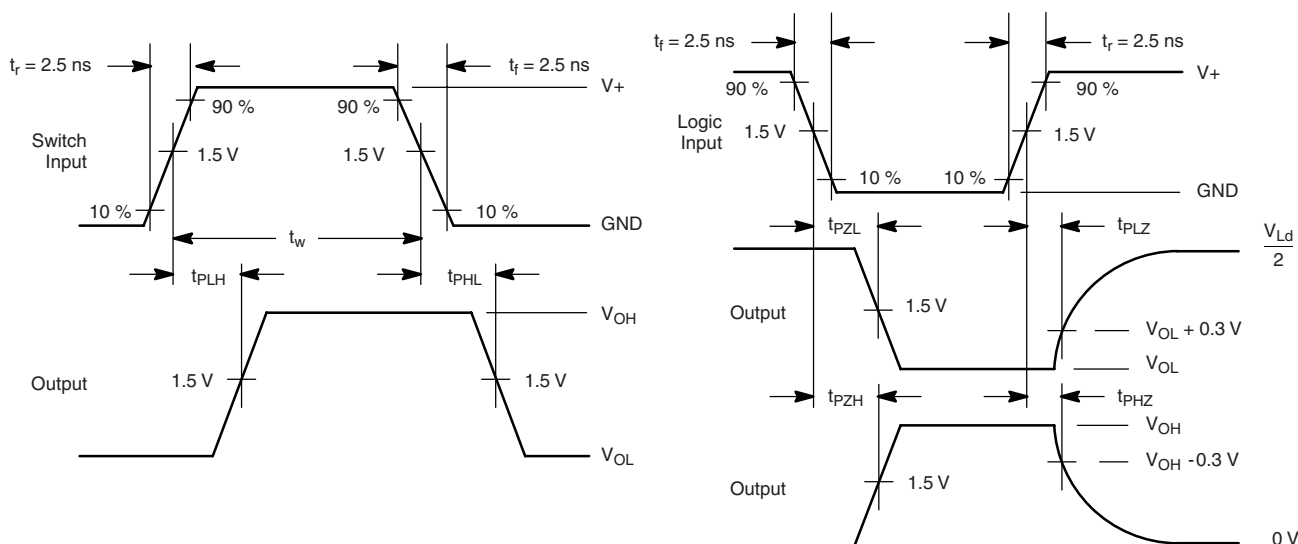
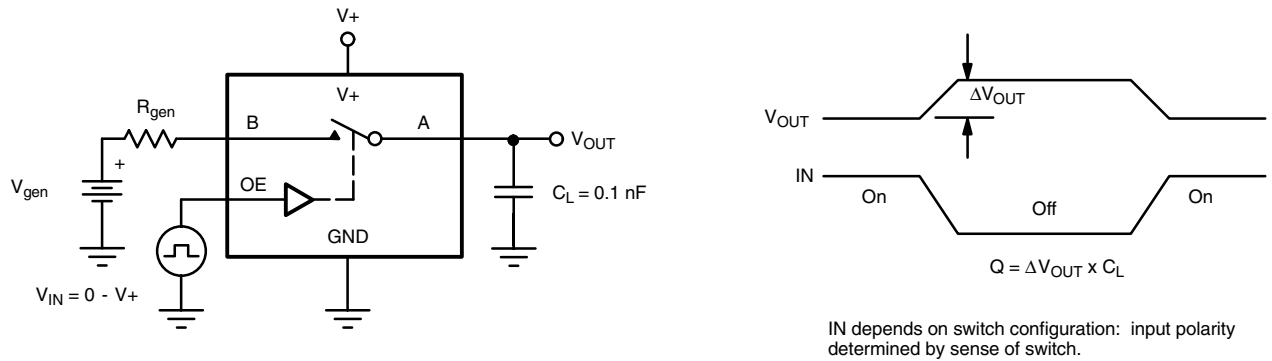
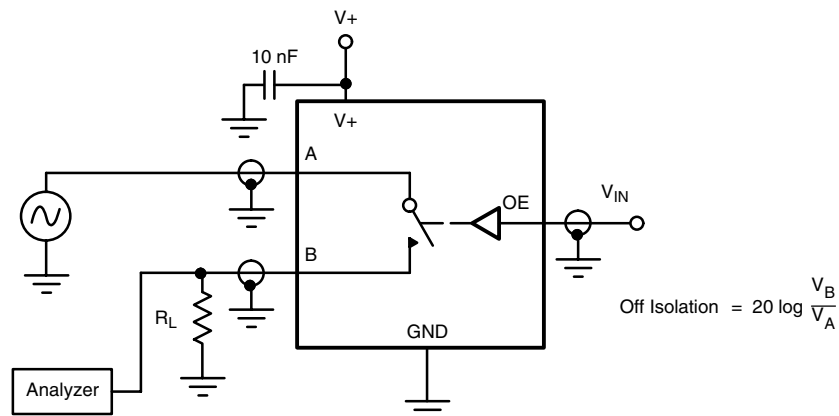
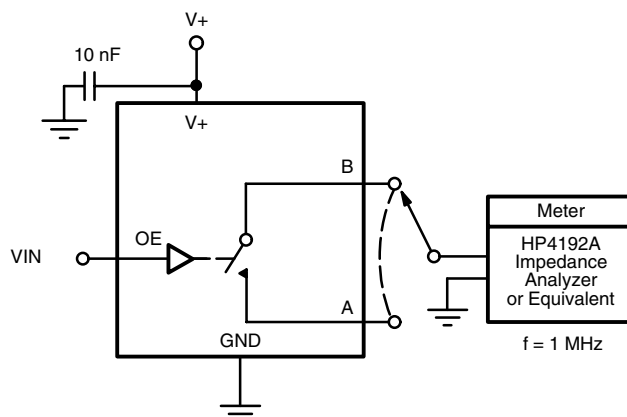


Figure 2. AC Waveforms

TEST CIRCUITS

Figure 3. Charge Injection

Figure 4. Off-Isolation

Figure 5. Channel Off/On Capacitance

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