

Automotive-grade dual N-channel 100 V, 25 mΩ typ., 7.8 A STripFET™ F3 Power MOSFET in a PowerFLAT™ 5x6 DI

Datasheet - production data

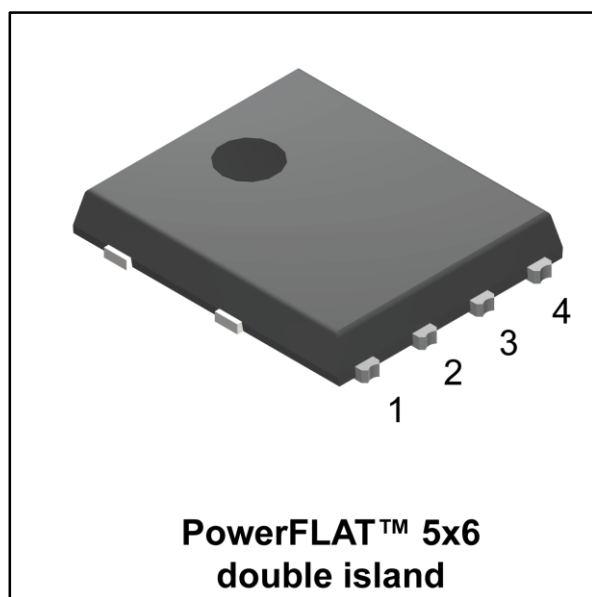
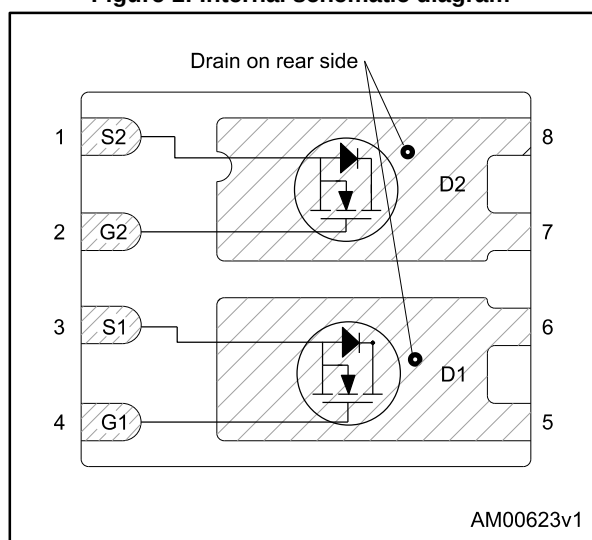


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max.	I _D
STL8DN10LF3	100 V	35 mΩ	7.8 A

- Designed for automotive applications and AEC-Q101 qualified
- Logic level V_{GS(th)}
- 175 °C maximum junction temperature
- 100% avalanche rated
- Wettable flank package

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using STripFET™ F3 technology. It is designed to minimize on-resistance and gate charge to provide superior switching performance.

Table 1: Device summary

Order code	Marking	Package	Packing
STL8DN10LF3	8DN10LF3	PowerFLAT™ 5x6 double island	Tape and reel

Contents

1	Electrical ratings	3
2	Electrical characteristics	4
	2.1 Electrical characteristics (curves).....	6
3	Test circuits	8
4	Package information	9
	4.1 PowerFLAT™ 5x6 double island package information.....	9
	4.2 Packing information.....	12
5	Revision history	14

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	100	V
V_{GS}	Gate-source voltage	± 20	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	20	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	20	A
$I_D^{(2)}$	Drain current (continuous) at $T_{pcb} = 25\text{ }^\circ\text{C}$	7.8	A
$I_D^{(2)}$	Drain current (continuous) at $T_{pcb} = 100\text{ }^\circ\text{C}$	5.5	A
$I_{DM}^{(2)(3)}$	Drain current (pulsed)	31.2	A
$P_{TOT}^{(1)}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	70	W
$P_{TOT}^{(2)}$	Total dissipation at $T_{pcb} = 25\text{ }^\circ\text{C}$	4.3	W
I_{AV}	Not-repetitive avalanche current	7.8	A
E_{AS}	Single pulse avalanche energy	190	mJ
T_j	Operating junction temperature range	-55 to 175	$^\circ\text{C}$
T_{stg}	Storage temperature range		

Notes:

⁽¹⁾This value is rated according to Rthj-case and limited by package

⁽²⁾The value is rated according to Rthj-pcb

⁽³⁾Pulse width limited by safe operating area.

Table 3: Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	2.1	$^\circ\text{C/W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	35	$^\circ\text{C/W}$

Notes:

⁽¹⁾When mounted on FR-4 board of 1 inch², 2oz Cu, t < 10 s.

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 4: On/Off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	I _D = 250 μA, V _{GS} = 0 V	100			V
I _{DSS}	Zero gate voltage drain current (V _{GS} = 0)	V _{DS} = 100 V			1	μA
I _{GSS}	Gate-body leakage current (V _{DS} = 0)	V _{GS} = ±20 V			±100	nA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 250 μA	1		3	V
R _{DS(on)}	Static drain-source on-resistance	V _{GS} = 10 V, I _D = 4 A		25	35	mΩ
		V _{GS} = 5 V, I _D = 4 A		40	50	mΩ

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C _{iss}	Input capacitance	V _{DS} = 25 V, f = 1 MHz, V _{GS} = 0 V	-	970	-	pF
C _{oss}	Output capacitance		-	115	-	
C _{rss}	Reverse transfer capacitance		-	11.5	-	
Q _g	Total gate charge	V _{DD} = 50 V, I _D = 7.8 A, V _{GS} = 10 V (see Figure 13: "Test circuit for gate charge behavior")	-	20.5	-	nC
Q _{gs}	Gate-source charge		-	4	-	
Q _{gd}	Gate-drain charge		-	5	-	
R _G	Intrinsic gate resistance	f = 1 MHz open drain	-	3.65	-	Ω

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t _{d(on)}	Turn-on delay time	V _{DD} = 50 V, I _D = 7.8 A, R _G = 4.7 Ω, V _{GS} = 10 V (see Figure 12: "Test circuit for resistive load switching times")	-	8.7	-	ns
t _r	Rise time		-	9.6	-	
t _{d(off)}	Turn-off delay time		-	50.6	-	
t _f	Fall time		-	5.2	-	

Table 7: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		7.8	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		31.2	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{DS} = 7.8 \text{ A}$, $V_{GS} = 0$			1.3	V
t_{rr}	Reverse recovery time	$I_{SD} = 7.8 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 48 \text{ V}$, $T_j = 150 \text{ }^\circ\text{C}$ (see <i>Figure 14: "Test circuit for inductive load switching and diode recovery times")</i>)	-	42.5		ns
Q_{rr}	Reverse recovery charge		-	87		nC
I_{RRM}	Reverse recovery current		-	4.08		A

Notes:

⁽¹⁾Pulse width limited by safe operating area

⁽²⁾Pulsed: pulse duration = 300 μs , duty cycle 1.5 %

2.1 Electrical characteristics (curves)

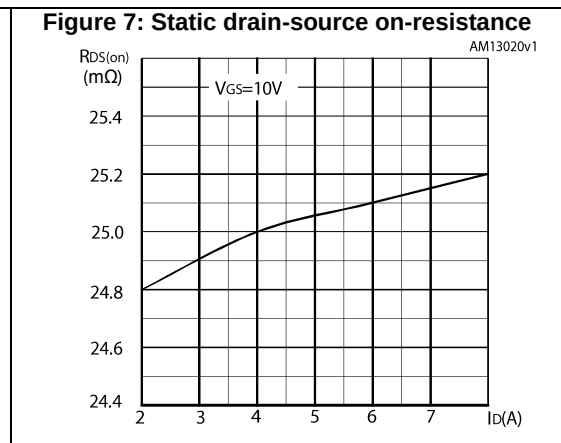
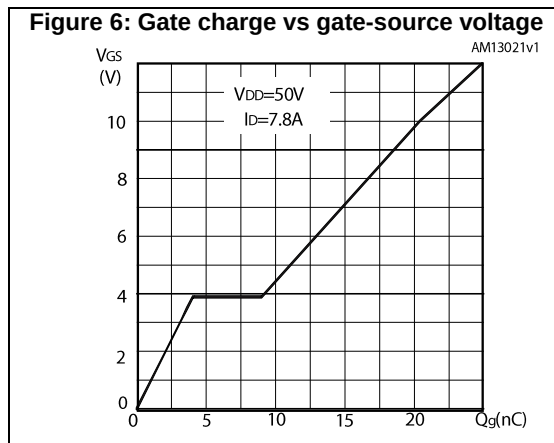
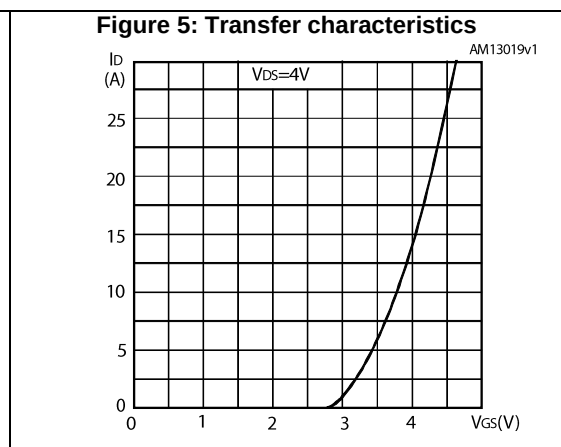
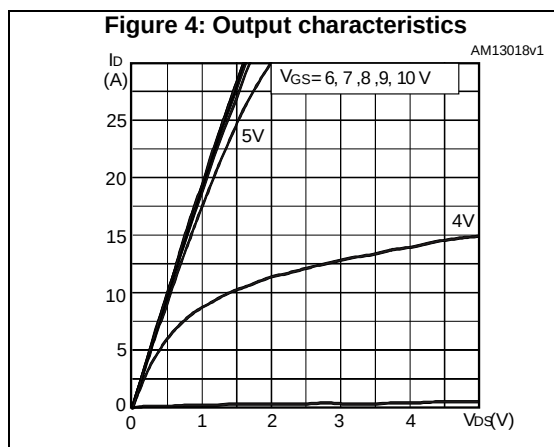
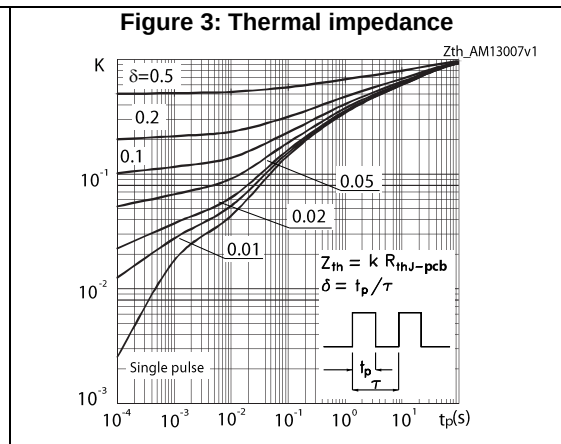
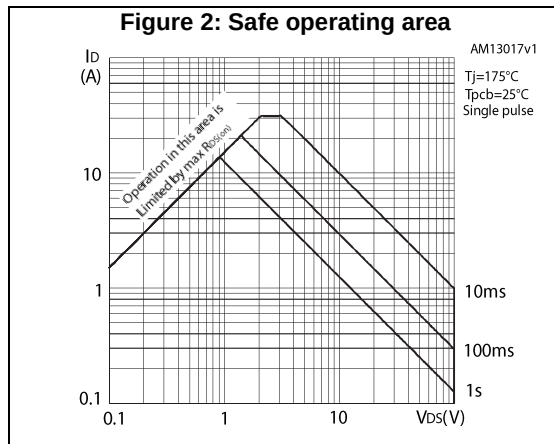


Figure 8: Capacitance variations

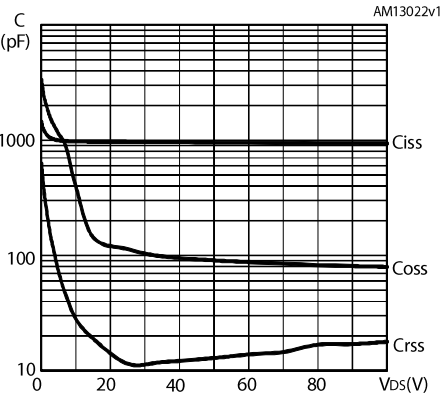


Figure 9: Normalized gate threshold voltage vs temperature

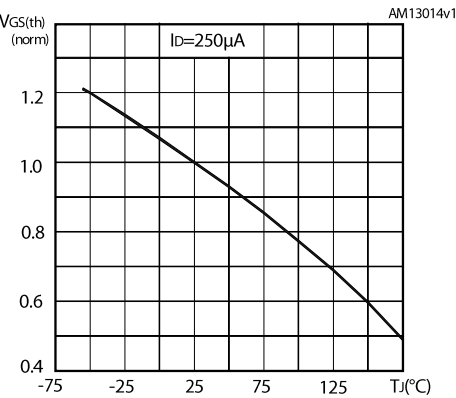


Figure 10: Normalized on-resistance vs temperature

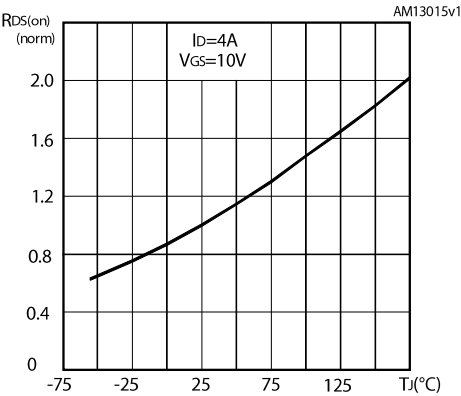
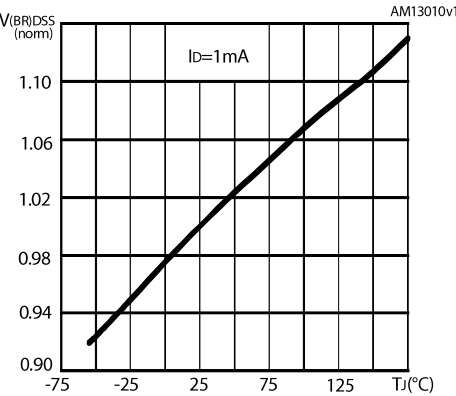
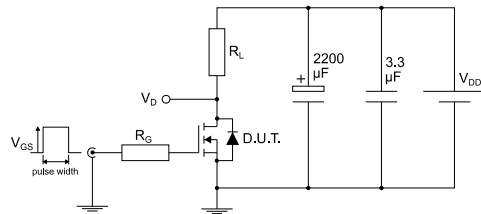


Figure 11: Normalized V(BR)DSS vs temperature



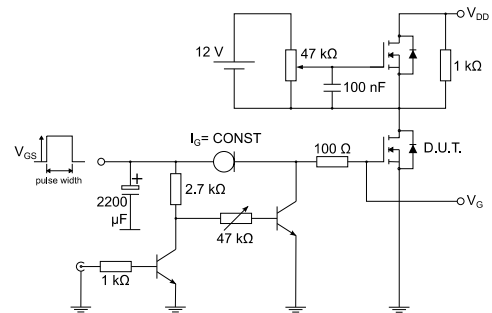
3 Test circuits

Figure 12: Test circuit for resistive load switching times



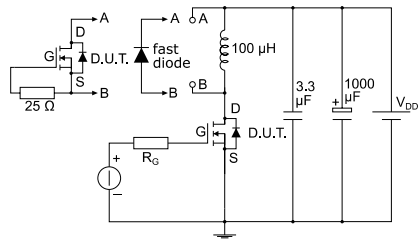
AM01468v1

Figure 13: Test circuit for gate charge behavior



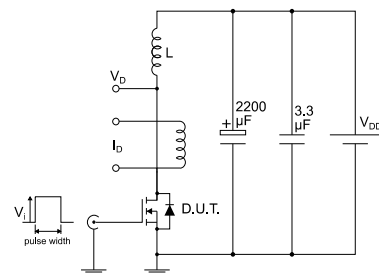
AM01469v1

Figure 14: Test circuit for inductive load switching and diode recovery times



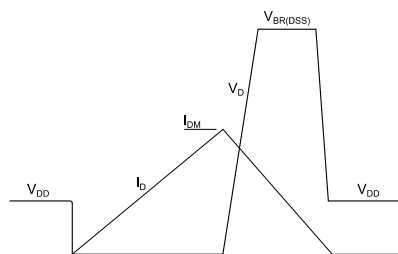
AM01470v1

Figure 15: Unclamped inductive load test circuit



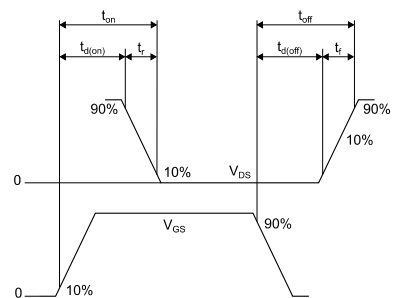
AM01471v1

Figure 16: Unclamped inductive waveform



AM01472v1

Figure 17: Switching time waveform



AM01473v1

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 PowerFLAT™ 5x6 double island package information

Figure 18: PowerFLAT™ 5x6 double island WF type R package outline

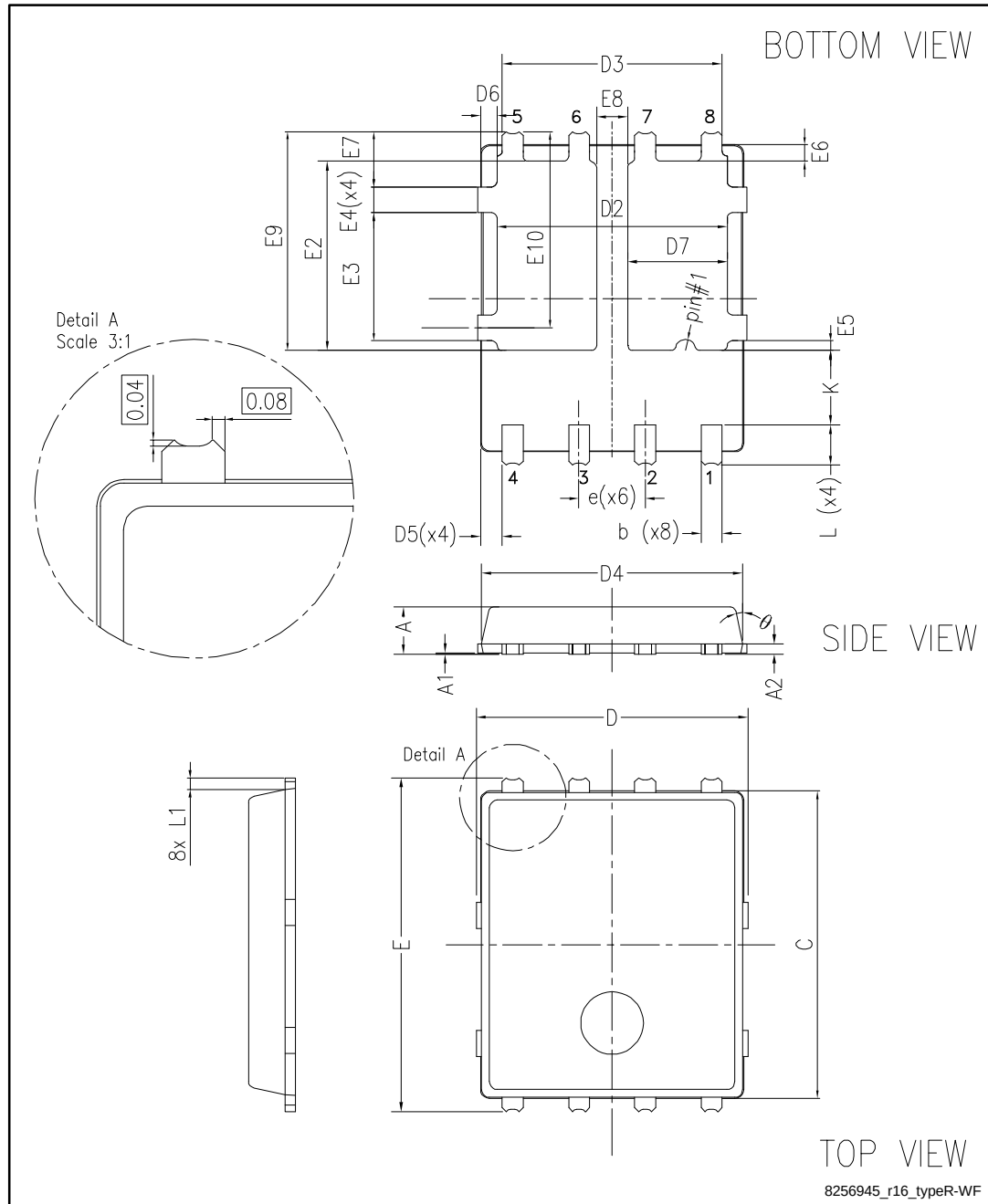
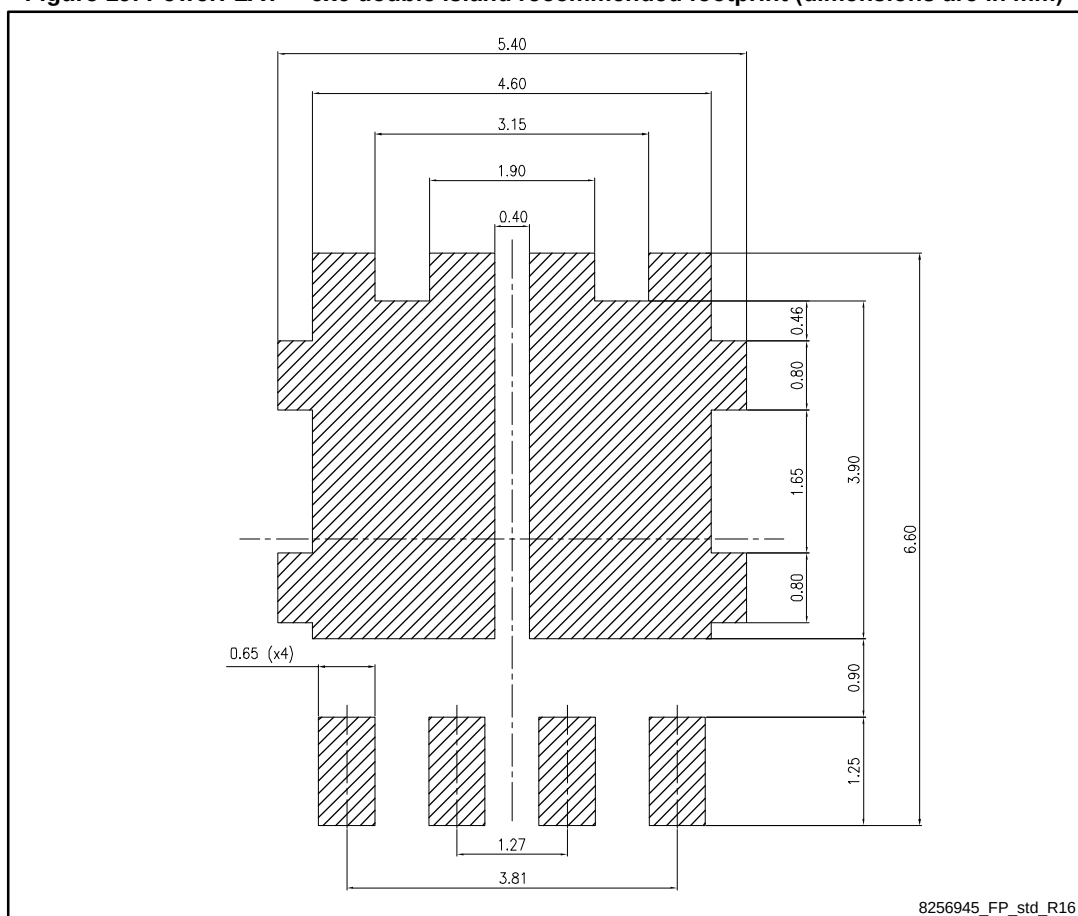


Table 8: PowerFLAT™ 5x6 double island WF type R mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
C	5.80	6.00	6.10
D	5.00	5.20	5.40
D2	4.15		4.45
D3	4.05	4.20	4.35
D4	4.80	5.00	5.10
D5	0.25	0.40	0.55
D6	0.15	0.30	0.45
D7	1.68		1.98
e		1.27	
E	6.20	6.40	6.60
E2	3.50		3.70
E3	2.35		2.55
E4	0.40		0.60
E5	0.08		0.28
E6	0.20	0.325	0.45
E7	0.85	1.00	1.15
E8	0.55		0.75
E9	4.00	4.20	4.40
E10	3.55	3.70	3.85
K	1.275		1.575
L	0.725	0.825	0.925
L1	0.175	0.275	0.375
θ	0°		12°

Figure 19: PowerFLAT™ 5x6 double island recommended footprint (dimensions are in mm)



4.2 Packing information

Figure 20: PowerFLAT™ 5x6 WF tape (dimensions are in mm)

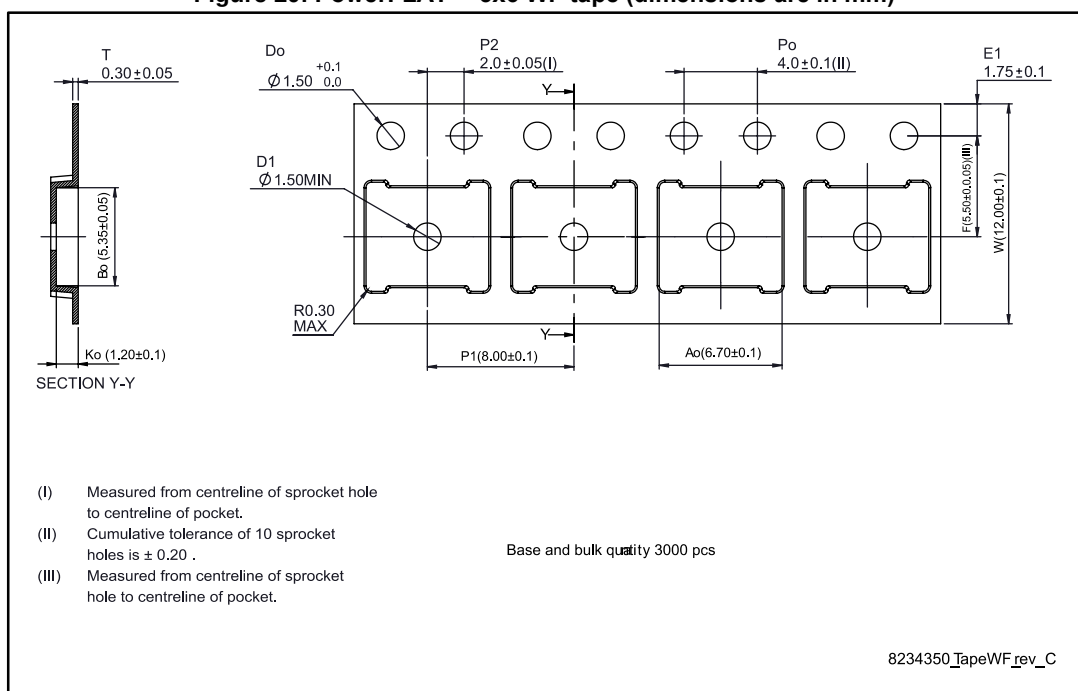


Figure 21: PowerFLAT™ 5x6 package orientation in carrier tape

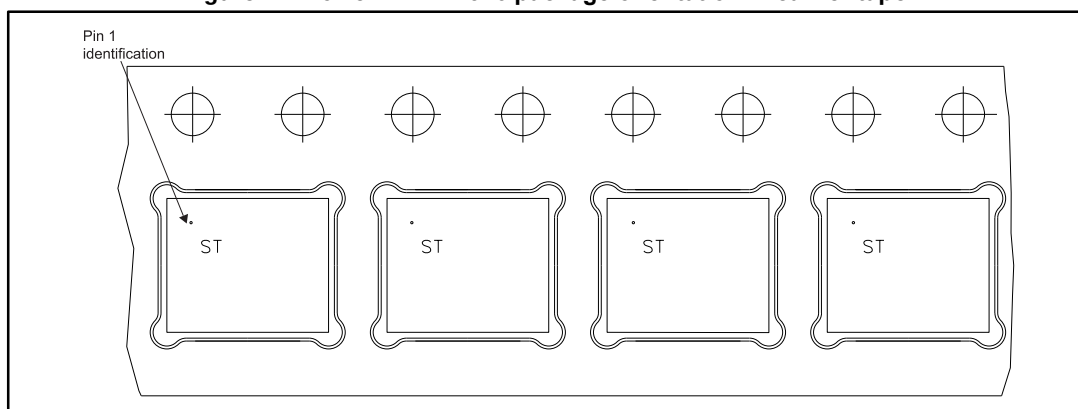
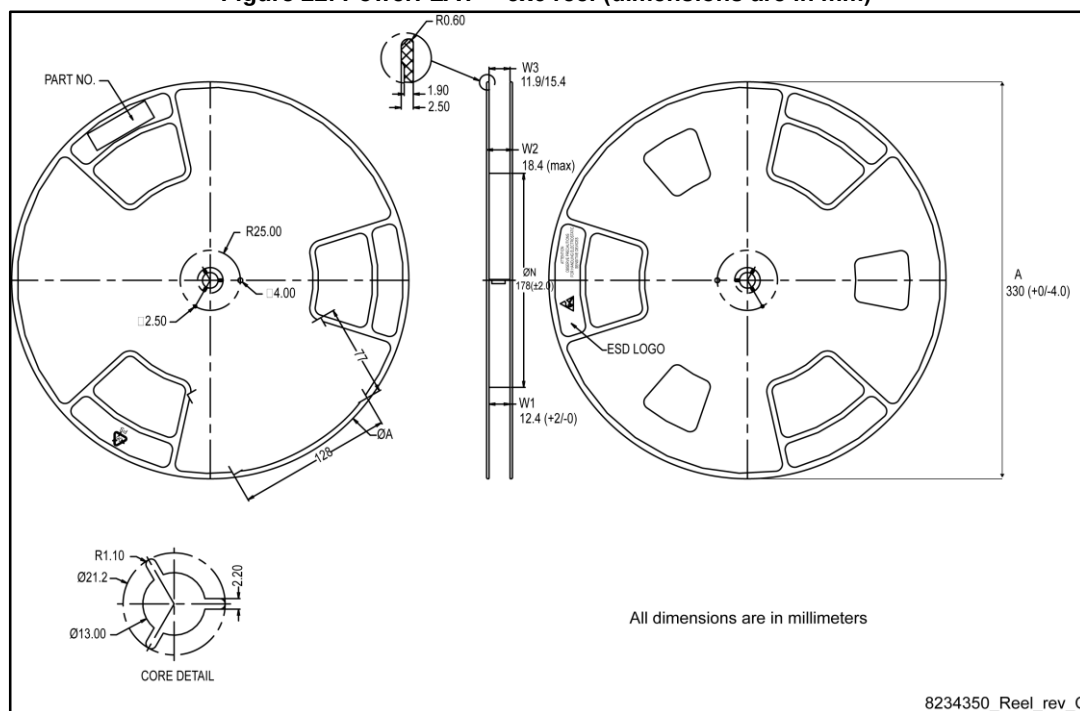


Figure 22: PowerFLAT™ 5x6 reel (dimensions are in mm)



5 Revision history

Table 9: Document revision history

Date	Revision	Changes
28-Mar-2012	1	First release.
20-Jun-2012	2	Added Section 2.1: Electrical characteristics (curves). Updated Section 4: Package information and title on the cover page..
26-Jun-2012	3	Updated Figure 9: Capacitance variations. Document status promoted from preliminary to production data
28-Oct-2013	4	– Updated: Section 4: Package information and Section 5: Packing information Updated title and features in cover page – Modified: VGS(th) value in Table 4 – Minor text changes
20-Feb-2014	5	Added: Features in cover page – Added: note 1 in Table 1 – Added: Table 19 and Table 9 – Added: Figure 20 – Minor text changes
10-Jul-2015	6	Updated title and description in cover page. – Updated Section 4: Package information.
09-Jun-2016	7	Updated Silhouette and description in cover page. Updated Figure 18: "PowerFLAT™ 5x6 double island WF type R package outline". Minor text changes.
21-Jun-2016	8	Updated <i>Figure 18: "PowerFLAT™ 5x6 double island WF type R package outline"</i> .

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2016 STMicroelectronics – All rights reserved