# TLIN1028-Q1 Automotive Local Interconnect Network (LIN) Transceiver with Integrated Voltage Regulator

## 1 Features

- AEC Q100 (Grade 1): Qualified for automotive applications
- Local interconnect network (LIN) physical layer specification ISO/DIS 17987–4.2 compliant and conforms to SAE J2602 recommended practice for LIN
- Supports 12 V applications
- Wide Operating Ranges
  - ±58 V LIN bus fault protection
  - LDO output supporting 3.3 V or 5 V
  - Sleep mode: ultra-low current consumption allows wake up event from:
    - LIN bus or local wake through EN pin
  - Power up and down glitch-free operation
- Protection Features:
  - ESD protection
  - Under voltage protection on $V_{SUP}$
  - TXD dominant time out (DTO) protection
  - Thermal shutdown protection
  - Unpowered node or ground disconnection failsafe at system level
- $V_{CC}$ sources 125 mA with DRB and DDA package
- Available in SOIC (8) and HSOIC (8) package and Leadless VSON (8) package with improved automated optical inspection (AOI) capability

## 2 Applications

- Body electronics and lighting
- Hybrid, electric & powertrain systems
- Automotive infotainment and cluster
- Appliances

## 3 Description

The TLIN1028-Q1 is a local interconnect network (LIN) physical layer transceiver, compliant to LIN 2.2A ISO/DIS 17987–4.2 standards, with an integrated low dropout (LDO) voltage regulator.

LIN is a single-wire bidirectional bus typically used for low speed in-vehicle networks using data rates up to 20 kbps. The LIN receiver supports data rates up to 100 kbps for end-of-line programming. The TLIN1028-Q1 converts the LIN protocol data stream on the TXD input into a LIN bus signal. The receiver converts the data stream to logic level signals that are sent to the microprocessor through the open-drain RXD pin. The TLIN1028-Q1 reduces system complexity by providing a 3.3 V or 5 V rail with up to 70 mA (D) and 125 mA (DRB and DDA) of current to power microprocessors, sensors or other devices. The TLIN1028-Q1 has an optimized current-limited wave-shaping driver which reduces electromagnetic emissions (EME).

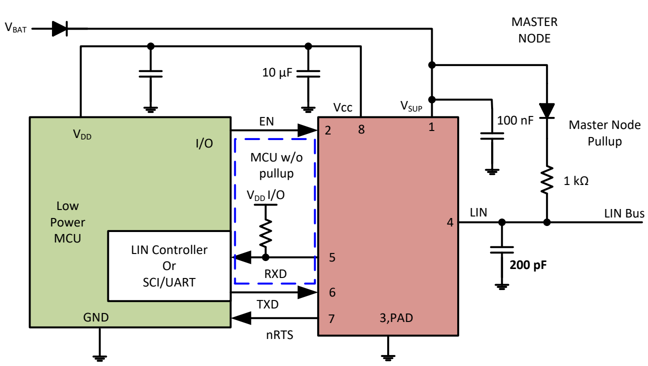
**Device Information**(1)

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| TLIN1028-Q1 | SOIC (8) | 4.90 mm x 3.91 mm |
| | HSOIC (8) | 4.90 mm x 3.91 mm |
| | VSON (8) | 3.00 mm x 3.00 mm |

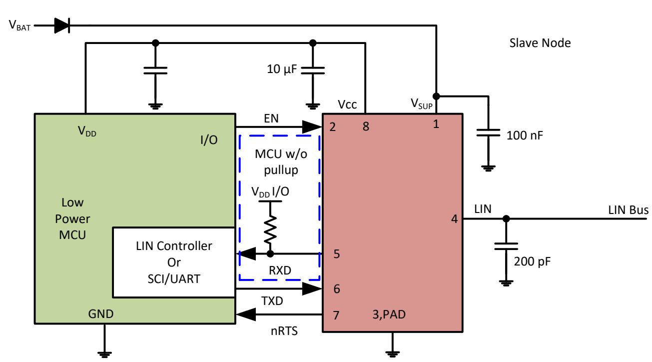
(1) For all available packages, see the orderable addendum at the end of the data sheet.

ADVANCE INFORMATION

**Simplified Schematics, Master Mode**




**Simplified Schematics, Slave Mode**



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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

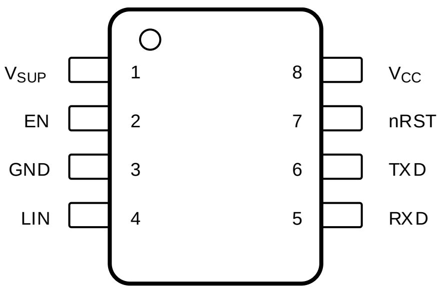
| DATE | REVISION | NOTES |
|---|---|---|
| August 2019 | * | Initial release. |

## 5 Description (continued)

Ultra-low current consumption is possible using the sleep mode which allows wake up via LIN bus or pin. The LIN bus has two states: dominant state (voltage near ground) and recessive state (voltage near battery). In the recessive state, the LIN bus is pulled high by the internal pull-up resistor (45 kΩ) and a series diode. No external pull-up components are required for slave applications. Master applications require an external pull-up resistor (1 kΩ) plus a series diode per the LIN specification.

## 6 Pin Configuration and Functions

**D Package**
**8-Pin (SOIC)**
**Top View**

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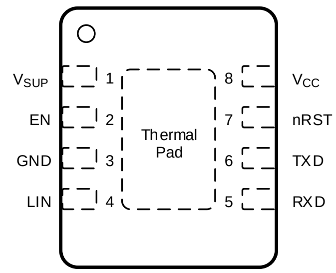
**DRB Package**
**8-Pin (VSON)**
**Top View**

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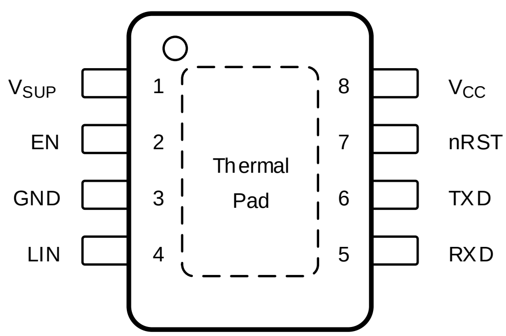
**DDA Package**
**8-Pin (HSOIC)**
**Top View**

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**Pin Functions**

| PIN | | TYPE(1) | DESCRIPTION |
|---|---|---|---|
| NO. | NAME | | |
| 1 | $V_{SUP}$ | HV Supply In | Device supply voltage (connected to battery in series with external reverse blocking diode) |
| 2 | EN | D I | Enable input |
| 3 | GND | GND | Ground (2) |
| 4 | LIN | HV I/O | LIN bus single-wire transmitter and receiver |
| 5 | RXD | D O | RXD output (open-drain) interface reporting state of LIN bus voltage |
| 6 | TXD | D I | TXD input interface to control state of LIN output |
| 7 | nRST | D O | Reset output (active low) |
| 8 | $V_{CC}$ | Supply Out | Output voltage from integrated LDO |

(1) HV - High Voltage, DI - Digital Input, DO - Digital Output, HV I/O - High Voltage Input/Output
(2) When the thermal pad is present, it must be soldered to ground plane.

ADVANCE INFORMATION

# 7 Specifications

## 7.1 ABSOLUTE MAXIMUM RATINGS

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{SUP}$ | Supply voltage range (ISO/DIS 17987) | –0.3 | 42 | V |
| $V_{LIN}$ | LIN Bus input voltage (ISO/DIS 17987) | –58 | 58 | V |
| $V_{CC50}$ | Regulated 5 V Output Supply | –0.3 | 6 | V |
| $V_{CC33}$ | Regulated 3.3 V Output Supply | –0.3 | 4.5 | V |
| $V_{nRST}$ | Reset output voltage | –0.3 | $V_{CC}$ + 0.3 | V |
| $V_{LOGIC\_INPUT}$ | Logic input voltage | –0.3 | 6 | V |
| $V_{LOGIC\_OUTPUT}$ | Logic output voltage | –0.3 | 6 | V |
| $I_{VCC}$ | $V_{CC}$ supply current | | 300 | mA |
| $I_O$ | Digital pin output current | –8 | 8 | mA |
| $I_{O(nRST)}$ | Reset output current | –5 | 5 | mA |
| $T_J$ | Junction temperature | –40 | 165 | °C |
| $T_{stg}$ | Storage temperature range | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 7.2 ESD RATINGS

| | | | | VALUE | UNIT |
|---|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM) classification level H2: $V_{SUP}$, LIN, and WAKE with respect to ground | | ±8000 | V |
| | | Human body model (HBM) classification level 3A: all other pins, per AEC Q100-002 (1) | | ±4000 | |
| | | Charged device model (CDM) classification level C5, per AEC Q100-011 | All pins | ±750 | |

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

## 7.3 ESD RATINGS, IEC SPECIFICATION

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge (1), LIN, $V_{SUP}$ terminal to GND (2) | IEC 61000-4-2 contact discharge | ±8000 | V |
| $V_{(ESD)}$ | Powered electrostatic discharge SAEJ2962-1 (3) | SAEJ2962-1 contact discharge | ±8000 | V |
| | | SAEJ2962-1 air discharge | ±15000 | |
| Transient | ISO7637-2 and IEC 62215-3 Transients according to IBEE LIN EMC test spec (4) | Pulse 1 | -100 | V |
| | | Pulse 2a | 75 | |
| | | Pulse 3a | -150 | |
| | | Pulse 3b | 100 | |
| Transient | ISO7637 Slow Transients Pulse | SAEJ2962-1 (5) test spec and IBEE Zwickau | 85 | V |

(1) IEC 61000-4-2 is a system-level ESD test. Results given here are specific to the IBEE LIN EMC Test specification conditions. Different system-level configurations may lead to different results
(2) Testing performed at 3rd party IBEE Zwickau test house, test report available upon request.
(3) SAEJ2962-1 Testing performed at 3rd party US3 approved EMC test facility, test report available upon request.
(4) ISO7637 is a system-level transient test. Results given here are specific to the IBEE LIN EMC Test specification conditions. Different system-level configurations may lead to different results.
(5) ISO7637 is a system-level transient test. Results given here are specific to the SAEJ2962-1 Test specification conditions. Different system-level configurations may lead to different results

## 7.4 RECOMMENDED OPERATING CONDITIONS

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{SUP}$ | Supply voltage | 5.5 | | 28 | V |
| $V_{LIN}$ | LIN bus input voltage | 0 | | 28 | V |
| $V_{LOGIC5}$ | Logic pin voltage | 0 | | 5.25 | V |

## RECOMMENDED OPERATING CONDITIONS (continued)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{LOGIC33}$ | Logic pin voltage | 0 | | 3.465 | V |
| $I_{OH(DO)}$ | Digital terminal HIGH level output current | -2 | | | mA |
| $I_{OL(DO)}$ | Digital terminal LOW level output current | | | 2 | mA |
| $C_{(VSUP)}$ | $V_{SUP}$ supply capacitor | 100 | | | nF |
| $C_{(VCC)}$ | $V_{CC}$ supply capacitor | 10 | | | µF |
| $ESR_{CO}$ | Output ESR requirements | 0.001 | | 2 | Ω |

## 7.5 THERMAL INFORMATION

| THERMAL METRIC[1] | | TLIN1028x | | | UNIT |
|---|---|---|---|---|---|
| | | D | DRB | DDA | |
| | | 8 PINS | 8 PINS | 8 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 119.4 | 45.7 | 40.9 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 51.5 | 49.2 | 60.5 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 64.9 | 18.9 | 15.6 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 9.6 | 0.7 | 4.0 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 63.7 | 18.8 | 15.8 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | n/a | 2.7 | 4.6 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 7.6 POWER SUPPLY CHARACTERISTICS

parameters valid over –40℃ ≤ $T_J$ ≤ 150 ℃ range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **SUPPLY VOLTAGE AND CURRENT** | | | | | | |
| $V_{SUP}$ | Operational supply voltage (ISO/DIS 17987 Param 10) | Device is operational beyond the LIN defined nominal supply voltage range. See Figure 1 and Figure 2 | 5.5 | | 36 | V |
| $V_{SUP}$ | Nominal supply voltage (ISO/DIS 17987 Param 10): | Normal and Standby Modes: Ramp VSUP while LIN signal is a 10 kHz square wave with 50 % duty cycle and swing between 5.5 V ≤ $V_{LIN}$ ≤ 28 V. See Figure 1 and Figure 2 | 5.5 | | 28 | V |
| | | Sleep Mode | 5.5 | | 28 | V |
| $UV_{SUPR}$ | Under voltage $V_{SUP}$ threshold | Ramp Up | | 3.5 | 4.2 | V |
| $UV_{SUPF}$ | Under voltage $V_{SUP}$ threshold | Ramp Down | 1.8 | 2.1 | 2.5 | V |
| $U_{VHYS}$ | Delta hysteresis voltage for $V_{SUP}$ under voltage threshold | | | 1.5 | | V |
| $I_{SUP}$ | Transceiver and LDO supply current (D Package) | Transceiver normal mode dominant plus LDO output | | | 80 | mA |
| $I_{SUP}$ | Transceiver and LDO supply current (DRB and DDA Packages) | Transceiver normal mode dominant plus LDO output | | | 135 | mA |
| $I_{SUPTRXDOM}$ | Supply current transceiver only | Normal Mode: EN = $V_{CC}$, bus dominant: total bus load where $R_{LIN}$ ≥ 500 Ω and $C_{LIN}$ ≤ 10 nF | | 1.2 | 7.5 | mA |
| | | Standby Mode: EN = 0 V, bus dominant: total bus load where $R_{LIN}$ ≥ 500 Ω and $C_{LIN}$ ≤ 10 nF | | 1 | 2.1 | mA |
| $I_{SUPTRXREC}$ | Supply current transceiver only | Normal Mode: EN = $V_{CC}$,<br>Bus recessive: LIN = $V_{SUP}$, | | 450 | 775 | µA |
| | | Standby Mode: EN = 0 V, LIN = recessive = $V_{SUP}$, $I_{OZH}$ from processor ≤ 1 µA | | 38 | 55 | µA |
| | | Added Standby Mode current through the RXD pull-up resistor with a value of 100 kΩ: EN = 0 V, LIN = recessive = VSUP, RXD = GND[1] | | | 55 | |

(1) RXD pin is an open drain output. In standby mode RXD is pulled low which has the device pulling current through $V_{SUP}$ through the pull-up resisitor to $V_{CC}$. The value of the pull-up resistor impacts the standby mode current. A 10 kΩ resistor value can add as much at 500 µA of current.

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## POWER SUPPLY CHARACTERISTICS (continued)

parameters valid over –40℃ ≤ $T_J$ ≤ 150 ℃ range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{SUPTRXSLP}$ | Sleep mode supply current transceiver only | 5.5 V < $V_{SUP}$ ≤ 28 V, LIN = $V_{SUP}$, EN = 0 V, TXD and RXD floating | | 11 | 27 | µA |
| **REGULATED OUTPUT $V_{CC}$** | | | | | | |
| $V_{CC}$ | Regulated output (D package) | $V_{SUP}$ = 5.5 to 28 V, $I_{CC}$ = 1 to 70 mA | –2 | | 2 | % |
| $V_{CC}$ | Regulated output (DRB and DDA package) | $V_{SUP}$ = 5.5 to 28 V, $I_{CC}$ = 1 to 125 mA | –2 | | 2 | % |
| $\Delta V_{CC(\Delta VSUP)}$ | Line regulation | $V_{SUP}$ = 5.5 to 28 V, $\Delta V_{CC}$, $I_{CC}$ = 10 mA | | | 50 | mV |
| $\Delta V_{CC(\Delta VSUPL)}$ | Load regulation (DRB and DDA package) | $I_{CC}$ = 1 to 125 mA, $V_{SUP}$ = 14 V, $\Delta V_{CC}$ | | | 50 | mV |
| $\Delta V_{CC(\Delta VSUPL)}$ | Load regulation (D package) | $I_{CC}$ = 1 to 70 mA, $V_{SUP}$ = 14 V, $\Delta V_{CC}$ | | | 50 | mV |
| $V_{DROP}$ | Dropout voltage (5 V LDO) (DRB and DDA package) | $V_{SUP}$ – $V_{CC}$, $I_{CC}$ = 125 mA; | | 300 | 600 | mV |
| $V_{DROP}$ | Dropout voltage (5 V LDO) (D package) | $V_{SUP}$ – $V_{CC}$, $I_{CC}$ = 70 mA; | | 300 | 600 | mV |
| $V_{DROP}$ | Dropout voltage (3.3 V LDO) (DRB and DDA package) | $V_{SUP}$ – $V_{CC}$, $I_{CC}$ = 125 mA; | | 350 | 700 | mV |
| $V_{DROP}$ | Dropout voltage (3.3 V LDO) (D package) | $V_{SUP}$ – $V_{CC}$, $I_{CC}$ = 70 mA; | | 350 | 700 | mV |
| $UV_{CC5R}$ | Under voltage 5 V $V_{CC}$ threshold | Ramp Up | | 4.7 | 4.86 | V |
| $UV_{CC5F}$ | Under voltage 5 V $V_{CC}$ threshold | Ramp Down | 4.2 | 4.45 | | V |
| $UV_{CC33R}$ | Under voltage 3.3 V $V_{CC}$ threshold | Ramp Up | | 2.9 | 3.1 | V |
| $UV_{CC33F}$ | Under voltage 3.3 V $V_{CC}$ threshold | Ramp Down | 2.5 | 2.75 | | V |
| $t_{DET(UVCC)}$ | VCC undervoltage deglitch time. An $UV_{CC}$ event will not be recognized unless it last longer than this. | $C_{nRST}$ = 20pF | 1 | | 15 | µs |
| $I_{CCOUT}$ | Output current (D Package) | $V_{CC}$ in regulation with 12 V $V_{SUP}$ | 0 | | 70 | mA |
| $I_{CCOUT}$ | Output current (DRB and DDA package) | $V_{CC}$ in regulation with 12 V $V_{SUP}$ | 0 | | 125 | mA |
| $I_{CCOUTL}$ | Output current limit | $V_{CC}$ short to ground | | | 275 | mA |
| PSRR | Power supply rejection ripple rejection | $V_{RIP}$ = 0.5 $V_{PP}$, Load = 10 mA, $f$ = 100 Hz, CO = 10 µF | | 60 | | dB |
| $T_{SDR}$ | Thermal shutdown temperature | Internal junction temperature - rising | 165 | | | °C |
| $T_{SDF}$ | Thermal shutdown temperature | Internal junction temperature - falling | | | 150 | °C |
| $T_{SDHYS}$ | Thermal shutdown hysteresis | | | 10 | | °C |

## 7.7 ELECTRICAL CHARACTERISTICS

parameters valid over –40℃ ≤ $T_J$ ≤ 150 ℃ range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **RXD OUTPUT TERMINAL (OPEN DRAIN)** | | | | | | |
| $V_{OL}$ | Output low voltage | Based upon a 2 kΩ to 10 kΩ external pull-up to $V_{CC}$ | | | 0.2 | $V_{CC}$ |
| $I_{OL}$ | Low level output current, open drain | LIN = 0 V, RXD = 0.4 V | 1.5 | | | mA |
| $I_{LKG}$ | Leakage current, high-level | LIN = $V_{SUP}$, RXD = $V_{CC}$ | –5 | 0 | 5 | µA |
| **TXD INPUT TERMINAL** | | | | | | |
| $V_{IL}$ | Low level input voltage | | –0.3 | | 0.8 | V |
| $V_{IH}$ | High level input voltage | | 2 | | 5.5 | V |
| $I_{IH}$ | High level input leakage current | TXD = high | –5 | 0 | 5 | µA |
| $R_{TXD}$ | Internal pull-up resistor value | | 125 | 350 | 800 | kΩ |
| **LIN TERMINAL (REFERENCED TO $V_{SUP}$)** | | | | | | |
| $V_{OH}$ | HIGH level output voltage | LIN recessive, TXD = high, $I_O$ = 0 mA, $V_{SUP}$ = 5.5 V to 36 V | 0.85 | | | $V_{SUP}$ |
| $V_{OL}$ | LOW level output voltage | LIN dominant, TXD = low, $V_{SUP}$ = 5.5 V to 36 V | | | 0.2 | $V_{SUP}$ |
| $V_{SUP\_NON\_OP}$ | $V_{SUP}$ where impact of recessive LIN bus < 5% (ISO/DIS 17987 Param 11) | TXD & RXD open, $V_{LIN}$ = 5.5 V to 42 V, Bus Load = 60 kΩ + diode and 1.1 kΩ + diode | –0.3 | | 42 | V |
| $I_{BUS\_LIM}$ | Limiting current (ISO/DIS 17987 Param 12) | TXD = 0 V, $V_{LIN}$ = 36 V, $R_{MEAS}$ = 440 Ω, $V_{SUP}$ = 36 V, $V_{BUSdom}$ < 4.518 V; Figure 6 | 40 | 90 | 200 | mA |

## ELECTRICAL CHARACTERISTICS (continued)

parameters valid over –40°C ≤ $T_J$ ≤ 150 °C range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{BUS\_PAS\_dom}$ | Receiver leakage current, dominant (ISO/DIS 17987 Param 13) | $V_{LIN}$ = 0 V, $V_{SUP}$ = 12 V Driver off/recessive, $R_{MEAS}$ = 499 Ω; Figure 7 | –1 | | | mA |
| $I_{BUS\_PAS\_rec1}$ | Receiver leakage current, recessive (ISO/DIS 17987 Param 14) | $V_{LIN}$ ≥ $V_{SUP}$, 5.5 V ≤ $V_{SUP}$ ≤ 36 V Driver off, $R_{MEAS}$ = 1 kΩ; Figure 8 | | | 20 | µA |
| $I_{BUS\_PAS\_rec2}$ | Receiver leakage current, recessive (ISO/DIS 17987 Param 14) | $V_{LIN}$ = $V_{SUP}$, Driver off, $R_{MEAS}$ = 1 kΩ; Figure 8 | –8 | | 8 | µA |
| $I_{BUS\_NO\_GND}$ | Leakage current, loss of ground (ISO/DIS 17987 Param 15) | GND = $V_{SUP}$, $V_{SUP}$ = 12 V, 0 V ≤ $V_{LIN}$ ≤ 28 V, $R_{MEAS}$ = 1 kΩ; Figure 9 | –1 | | 1 | mA |
| $I_{BUS\_NO\_BAT}$ | Leakage current, loss of supply (ISO/DIS 17987 Param 16) | 0 V ≤ $V_{LIN}$ ≤ 28 V, $V_{SUP}$ = GND, $R_{MEAS}$ = 10 kΩ; Figure 10 | | | 8 | µA |
| $V_{BUSdom}$ | Low level input voltage (ISO/DIS 17987 Param 17) | LIN dominant (including LIN dominant for wake up); Figure 3, Figure 4 | | | 0.4 | $V_{SUP}$ |
| $V_{BUSrec}$ | High level input voltage (ISO/DIS 17987 Param 18) | LIN recessive; Figure 3, Figure 4 | 0.6 | | | $V_{SUP}$ |
| $V_{BUS\_CNT}$ | Receiver center threshold (ISO/DIS 17987 Param 19) | $V_{BUS\_CNT}$ = ($V_{IL}$ + $V_{IH}$)/2; Figure 3, Figure 4 | 0.475 | 0.5 | 0.525 | $V_{SUP}$ |
| $V_{HYS}$ | Hysteresis voltage (ISO/DIS 17987 Param 20) | $V_{HYS}$ = ($V_{IL}$ - $V_{IH}$); Figure 3, Figure 4 | | | 0.175 | $V_{SUP}$ |
| $V_{SERIAL\_DIODE}$ | Serial diode LIN term pull-up path (ISO/DIS 17987 Param 21) | By design and characterization | 0.4 | 0.7 | 1.0 | V |
| $R_{SLAVE}$ | Pull-up resistor to $V_{SUP}$ (ISO/DIS 17987 Param 26) | Normal and Standby modes | 20 | 45 | 60 | kΩ |
| $I_{RSLEEP}$ | Pull-up current source to $V_{SUP}$ | Sleep mode, $V_{SUP}$ = 12 V, LIN = GND | –20 | | –2 | µA |
| $C_{LIN,PIN}$ | Capacitance of the LIN pin | | | | 55 | pF |
| **EN INPUT TERMINAL** | | | | | | |
| $V_{IH}$ | High level input voltage | | 2 | | 5.5 | V |
| $V_{IL}$ | Low level input voltage | | –0.3 | | 0.8 | V |
| $V_{HYS}$ | Hysteresis voltage | By design and characterization | 30 | | 500 | mV |
| $I_{IL}$ | Low level input current | EN = Low | –5 | 0 | 5 | µA |
| $R_{EN}$ | Internal pull-down resistor | | 125 | 350 | 800 | kΩ |
| **nRST TERMINAL (OPEN DRAIN OUTPUT)** | | | | | | |
| $I_{LKG}$ | Leakage current, high-level | LIN = $V_{SUP}$, nRST = $V_{CC}$ | –5 | | 5 | µA |
| $V_{OL}$ | Low-level output voltage | Based upon external pull up to $V_{CC}$ | | | 0.2 | $V_{CC}$ |
| $I_{OL}$ | Low-level output current, open drain | LIN = 0 V, nRST = 0.4 V | 1.5 | | | mA |
| **DUTY CYCLE CHARACTERISTICS** | | | | | | |
| $D1_{12V}$ | Duty Cycle 1 (ISO/DIS 17987 Param 27) | $TH_{REC(MAX)}$ = 0.744 x $V_{SUP}$, $TH_{DOM(MAX)}$ = 0.581 x $V_{SUP}$, $V_{SUP}$ = 5.5 V to 18 V, $t_{BIT}$ = 50 µs (20 kbps), D1 = $t_{BUS\_rec(min)}$/(2 x $t_{BIT}$) (See Figure 11, Figure 12) | 0.396 | | | |
| $D2_{12V}$ | Duty Cycle 2 (ISO/DIS 17987 Param 28) | $TH_{REC(MIN)}$ = 0.422 x $V_{SUP}$, $TH_{DOM(MIN)}$ = 0.284 x $V_{SUP}$, $V_{SUP}$ = 5.5 V to 18 V, $t_{BIT}$ = 50 µs (20 kbps), D2 = $t_{BUS\_rec(MAX)}$/(2 x $t_{BIT}$) (See Figure 11, Figure 12) | | | 0.581 | |
| $D3_{12V}$ | Duty Cycle 3 (ISO/DIS 17987 Param 29) | $TH_{REC(MAX)}$ = 0.778 x $V_{SUP}$, $TH_{DOM(MAX)}$ = 0.616 x $V_{SUP}$, $V_{SUP}$ = 5.5 V to 18 V, $t_{BIT}$ = 96 µs (10.4 kbps), D3 = $t_{BUS\_rec(min)}$/(2 x $t_{BIT}$) (See Figure 11, Figure 12) | 0.417 | | | |
| $D4_{12V}$ | Duty Cycle 4 (ISO/DIS 17987 Param 30) | $TH_{REC(MIN)}$ = 0.389 x $V_{SUP}$, $TH_{DOM(MIN)}$ = 0.251 x $V_{SUP}$, $V_{SUP}$ = 5.5 V to 18 V, $t_{BIT}$ = 96 µs (10.4 kbps), D4 = $t_{BUS\_rec(MAX)}$/(2 x $t_{BIT}$) (See Figure 11, Figure 12) | | | 0.59 | |

ADVANCE INFORMATION

## 7.8 AC SWITCHING CHARACTERISTICS

parameters valid over –40℃ ≤ $T_J$ ≤ 150 ℃ range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **DEVICE SWITCHING CHARACTERISTICS** | | | | | | |
| $t_{rx\_pdr}$<br>$t_{rx\_pdf}$ | Receiver rising/falling propagation delay time (ISO/DIS 17987 Param 31) | $R_{RXD}$ = 2.4 kΩ, $C_{RXD}$ = 20 pF (See Figure 13, Figure 14 and Figure 18) | | | 6 | µs |
| $t_{rs\_sym}$ | Symmetry of receiver propagation delay time Receiver rising propagation delay time (ISO/DIS 17987 Param 32) | Rising edge with respect to falling edge, ($t_{rx\_sym}$ = $t_{rx\_pdf}$ – $t_{rx\_pdr}$), $R_{RXD}$ = 2.4 kΩ, $C_{RXD}$ = 20 pF (Figure 13, Figure 14 and Figure 18) | –2 | | 2 | µs |
| $t_{LINBUS}$ | LIN wakeup time (minimum dominant time on LIN bus for wakeup) | See Figure 17, Figure 21 and Figure 22 | 25 | 100 | 150 | µs |
| $t_{CLEAR}$ | Time to clear false wakeup prevention logic if LIN bus had a bus stuck dominant fault (recessive time on LIN bus to clear bus stuck dominant fault) | See Figure 22 | 8 | 17 | 50 | µs |
| $t_{DST}$ | Dominant state time out | | 20 | 34 | 80 | ms |
| $t_{EN}$ | Enable pin deglitch time | Time enable pin state change before initiating mode change or sampling TXD pine: See Figure 15 | 3 | | 12 | µs |
| $t_{MODE\_CHANGE}$ | Mode change delay time sleep mode to normal mode | Time to change from normal mode to sleep or standby after TXD pin sampling after EN pin set low: See Figure 15 | | | 20 | µs |
| $t_{MODE\_CHANGE}$ | Mode change delay time sleep mode to normal mode | Time to change from sleep mode to normal mode through EN pin and not due to a wake event; RXD pulled up to $V_{CC}$: See Figure 15 | | | 800 | µs |
| $t_{NOMINT}$ | Normal mode initialization time | Time for normal mode to initialize and data on RXD pin to be valid after $t_{EN}$ See Figure 15 | | | 30 | µs |
| $t_{PWR}$ | Power up time | Upon power up time it takes for valid data on RXD | | | 1.5 | ms |

ADVANCE INFORMATION

# 8 Parameter Measurement Information

## 8.1 Test Circuit: Diagrams and Waveforms

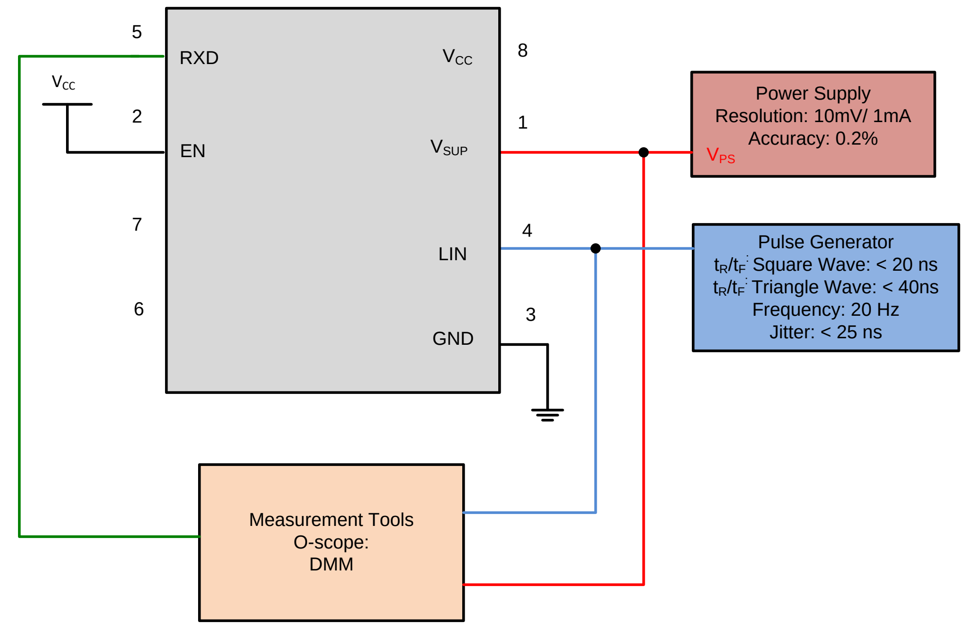


**Figure 1. Test System: Operating Voltage Range with RX and TX Access**

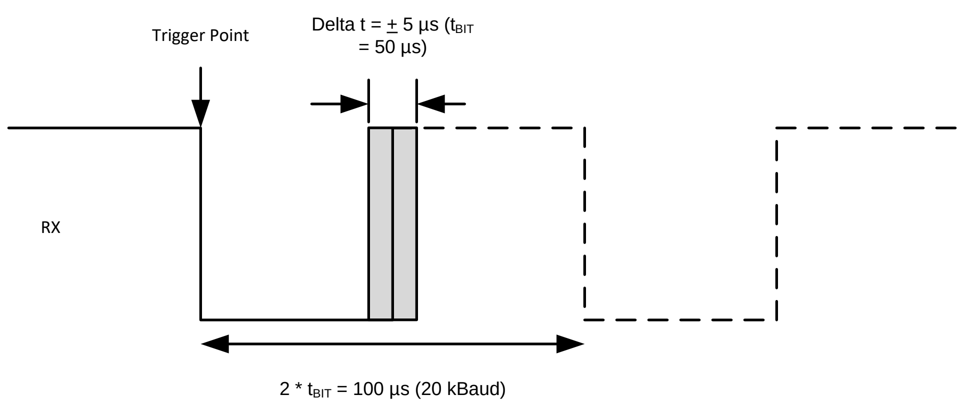


**Figure 2. RX Response: Operating Voltage Range**

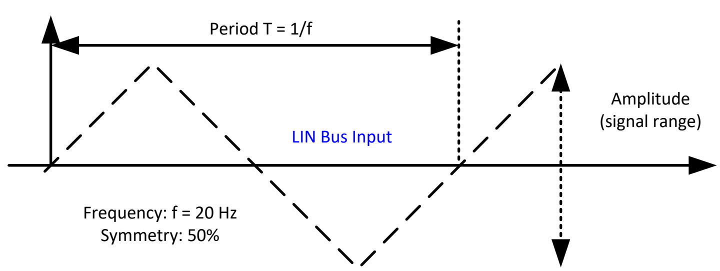


**Figure 3. LIN Bus Input Signal**

ADVANCE INFORMATION

## Test Circuit: Diagrams and Waveforms (continued)

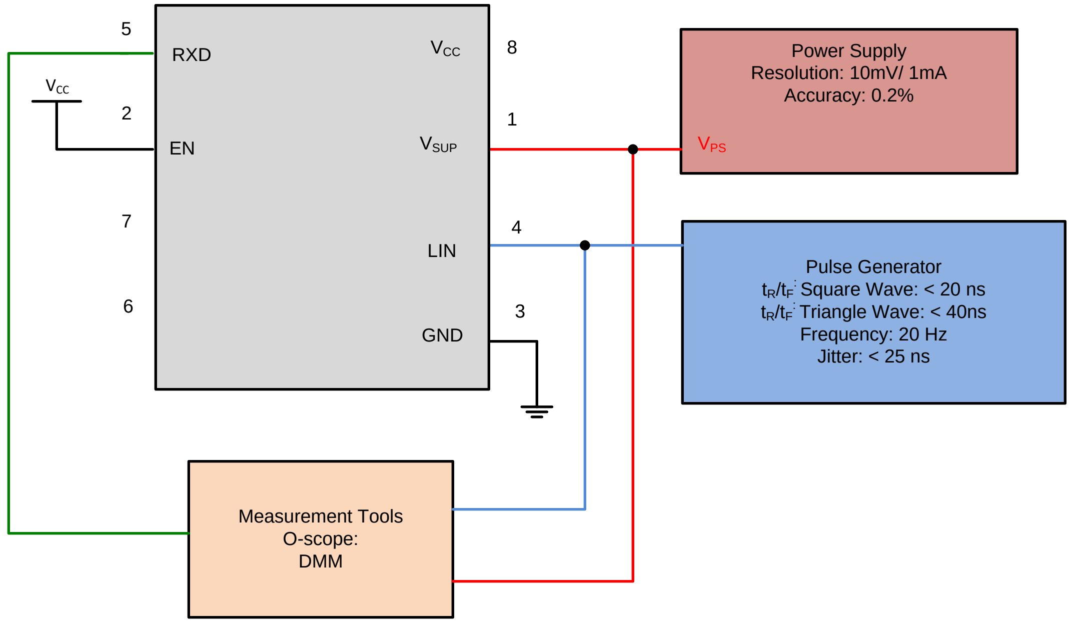


**Figure 4. LIN Receiver Test with RX access**

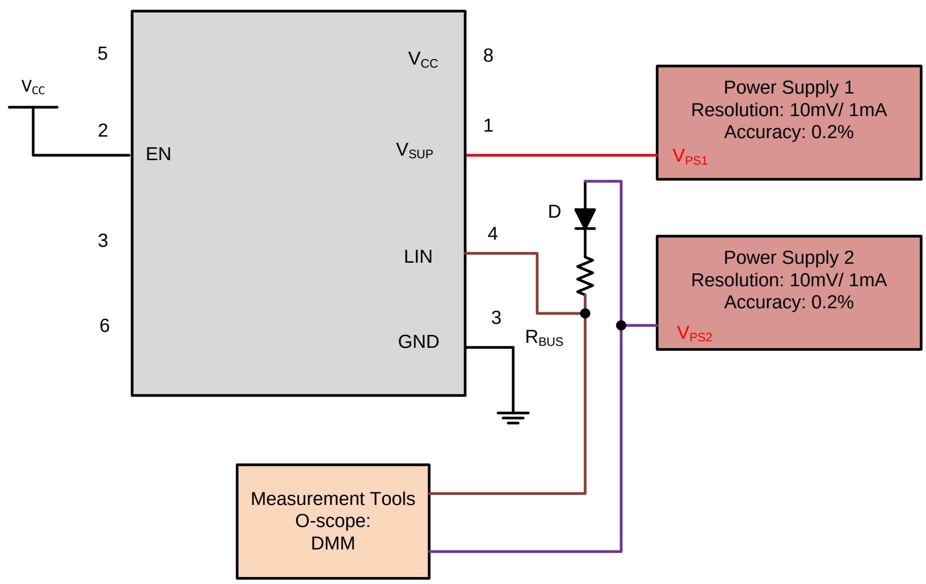


**Figure 5. $V_{SUP\_NON\_OP}$ Test Circuit**





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## Test Circuit: Diagrams and Waveforms (continued)

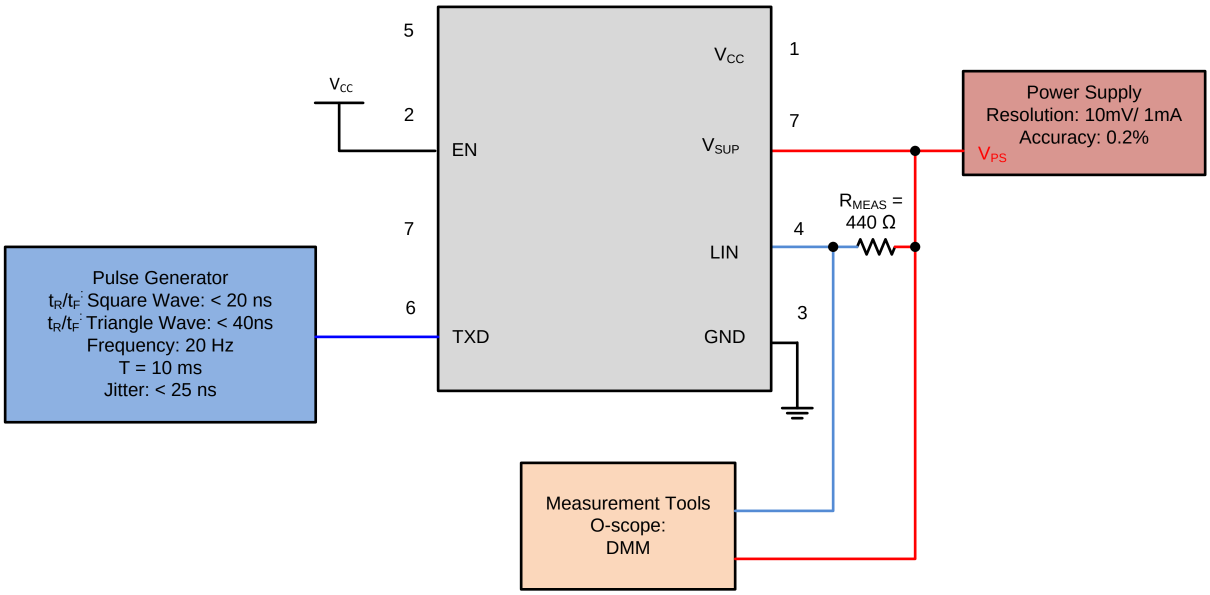


**Figure 6. Test Circuit for $I_{BUS\_LIM}$ at Dominant State (Driver on)**

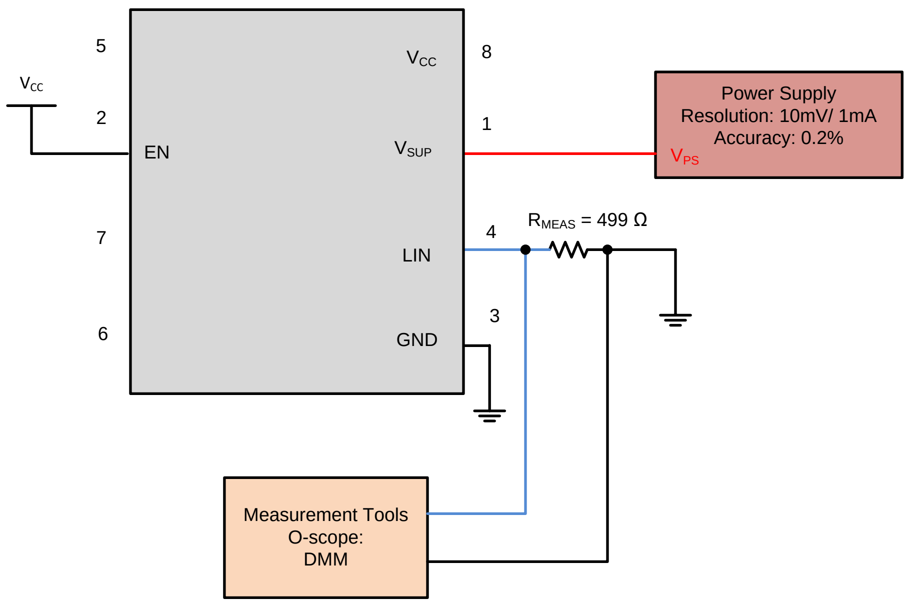


**Figure 7. Test Circuit for $I_{BUS\_PAS\_dom}$; TXD = Recessive State $V_{BUS}$ = 0 V**

ADVANCE INFORMATION

## Test Circuit: Diagrams and Waveforms (continued)

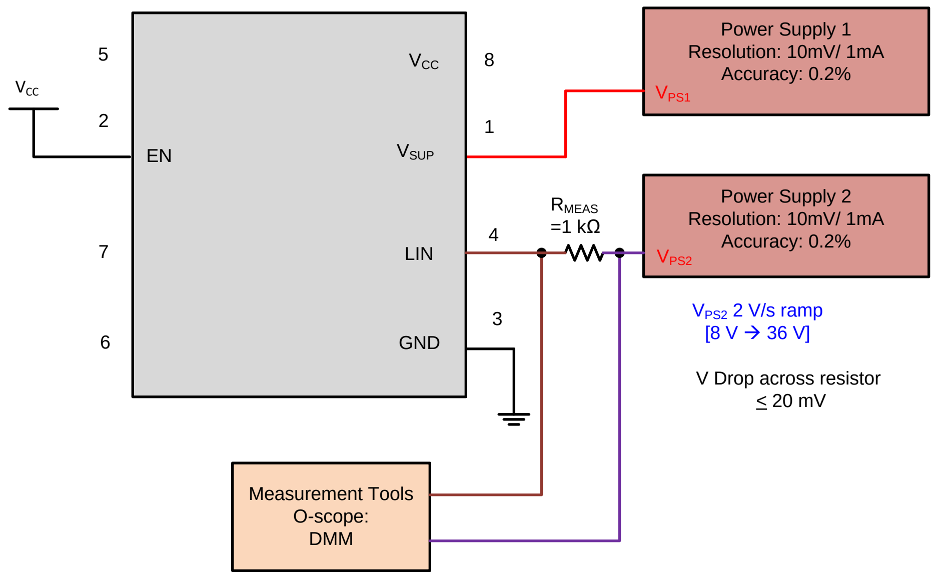


**Figure 8. Test Circuit for $I_{BUS\_PAS\_rec}$**

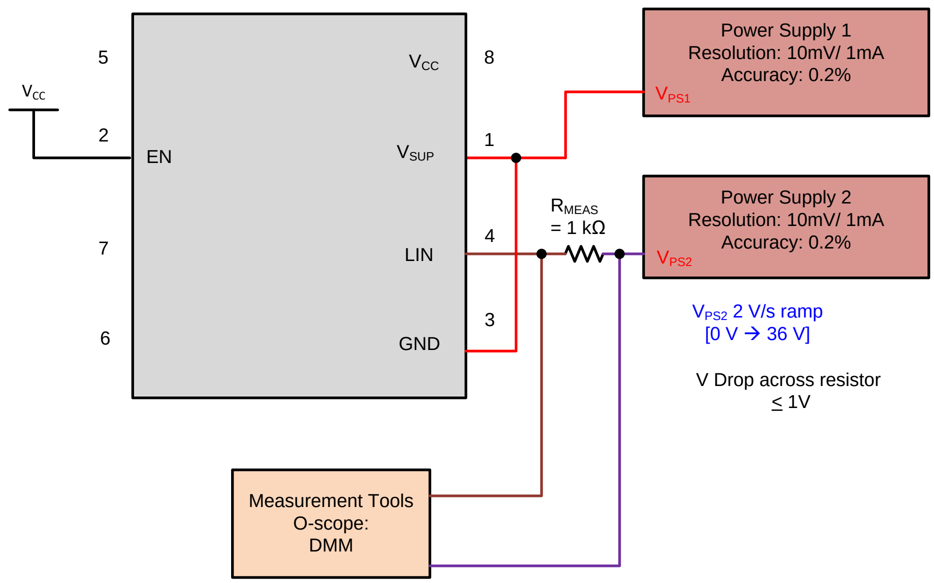


**Figure 9. Test Circuit for $I_{BUS\_NO\_GND}$ Loss of GND**

## Test Circuit: Diagrams and Waveforms (continued)

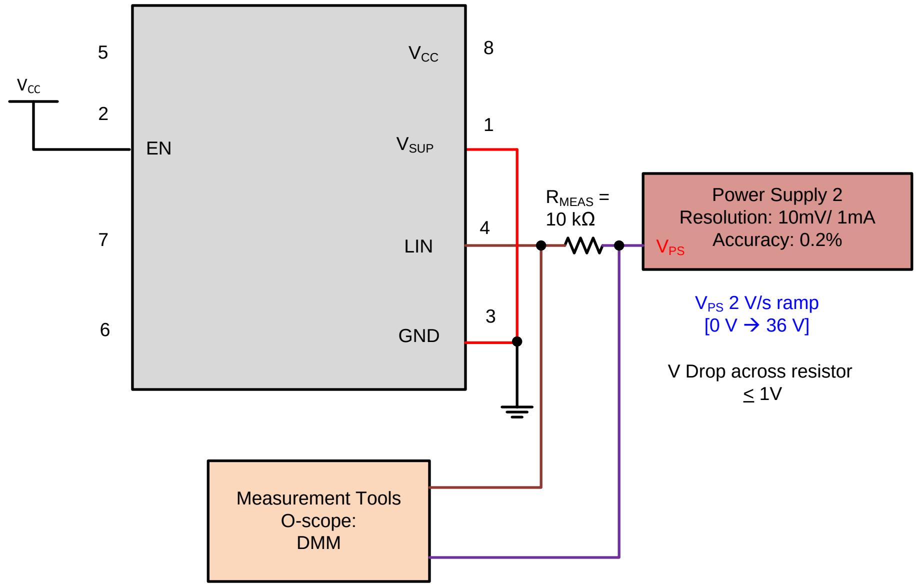


**Figure 10. Test Circuit for $I_{BUS\_NO\_BAT}$ Loss of Battery**

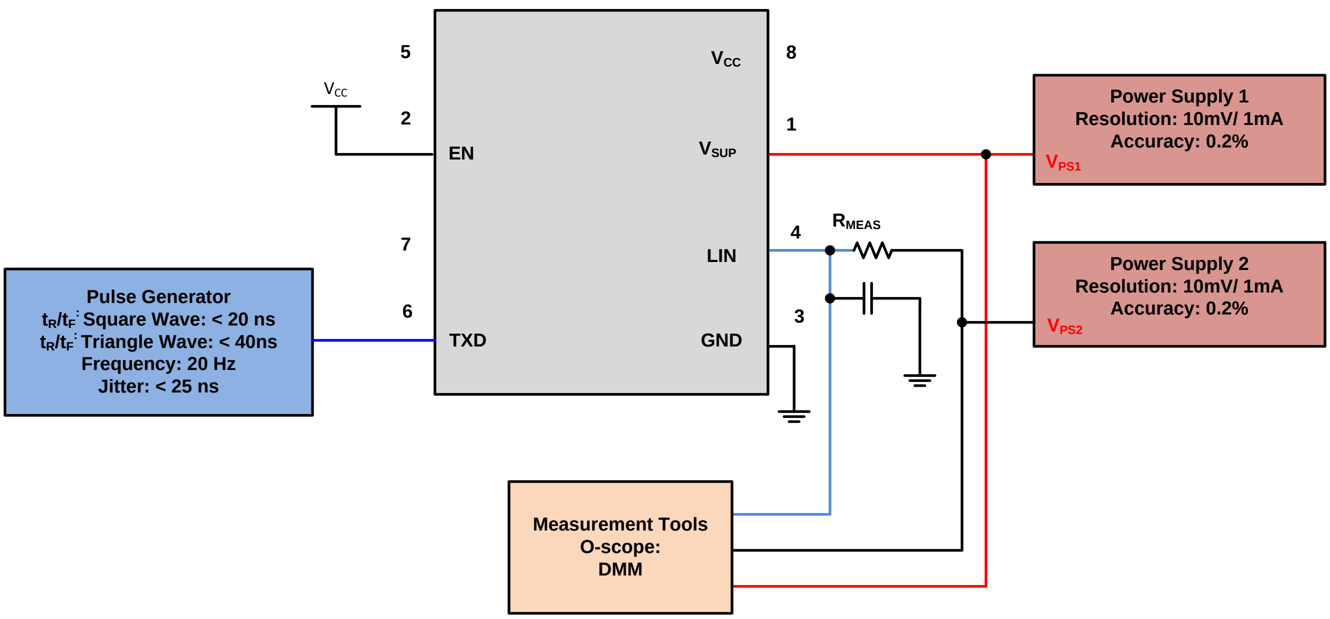


**Figure 11. Test Circuit Slope Control and Duty Cycle**

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## Test Circuit: Diagrams and Waveforms (continued)

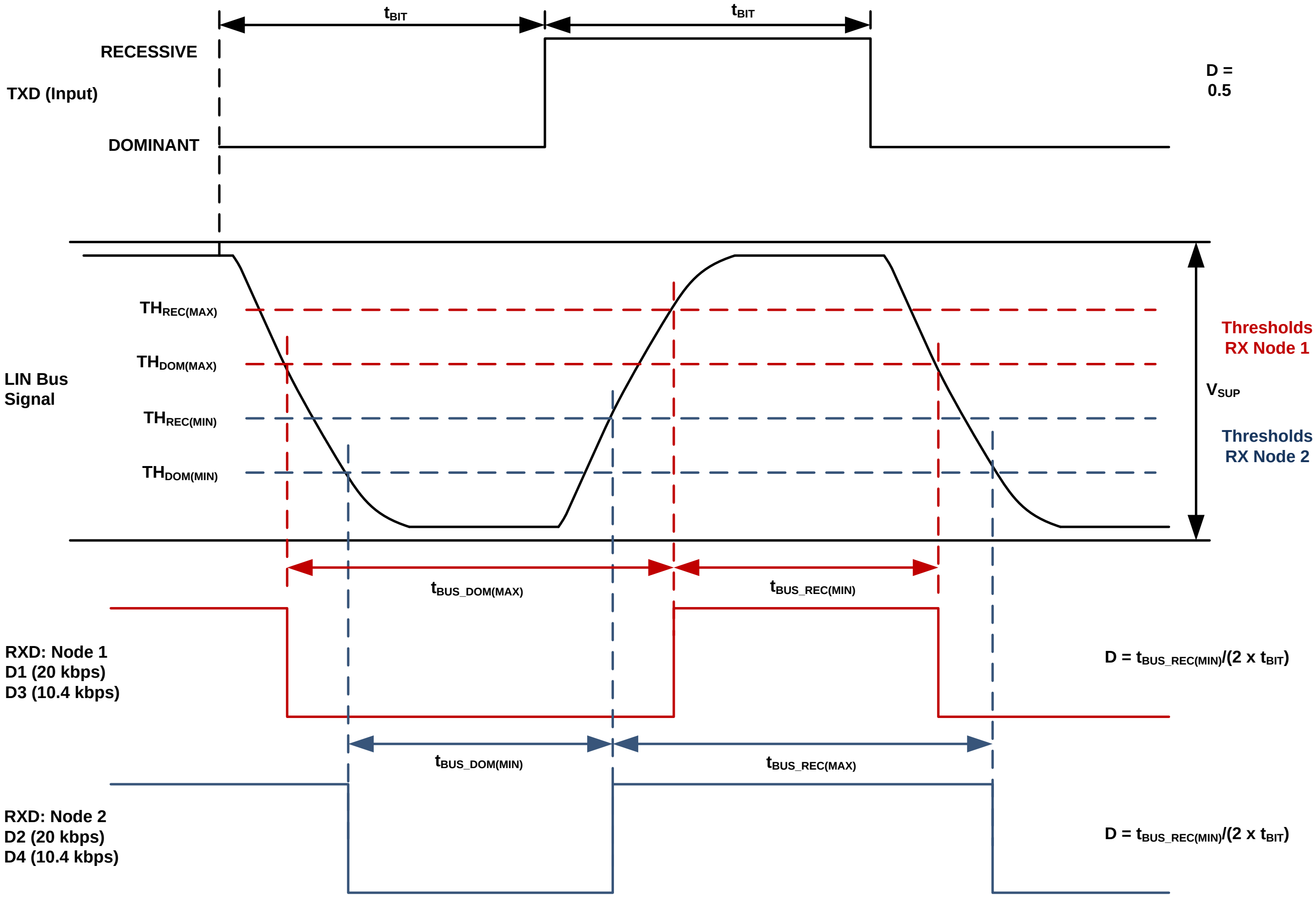


**Figure 12. Definition of Bus Timing**

## Test Circuit: Diagrams and Waveforms (continued)

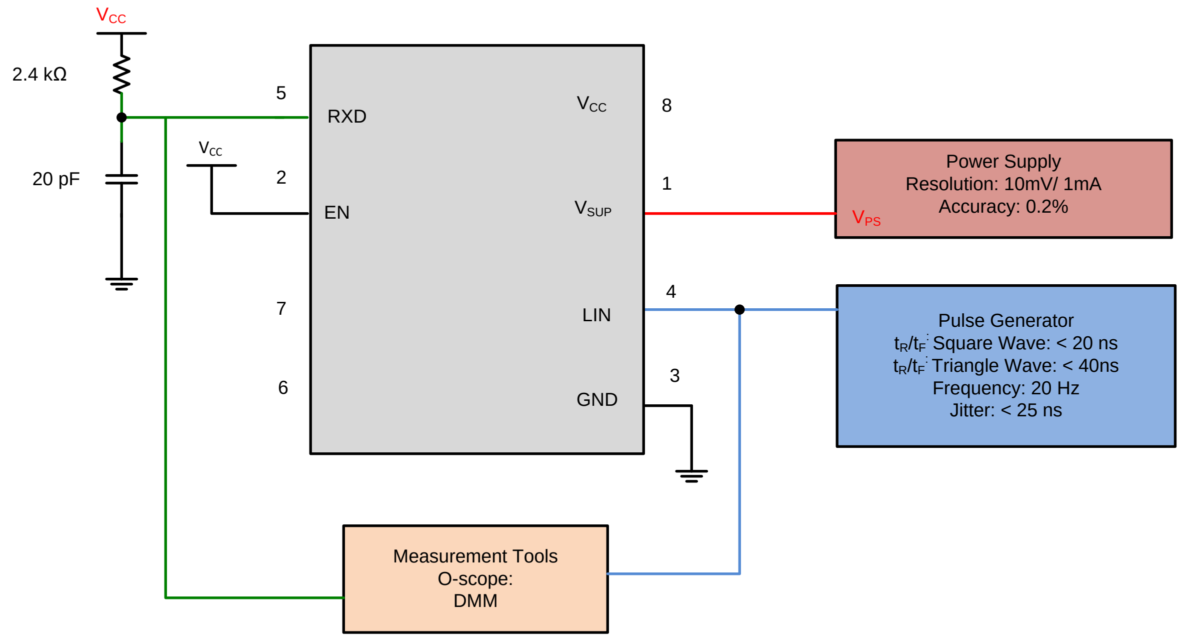


**Figure 13. Propagation Delay Test Circuit**

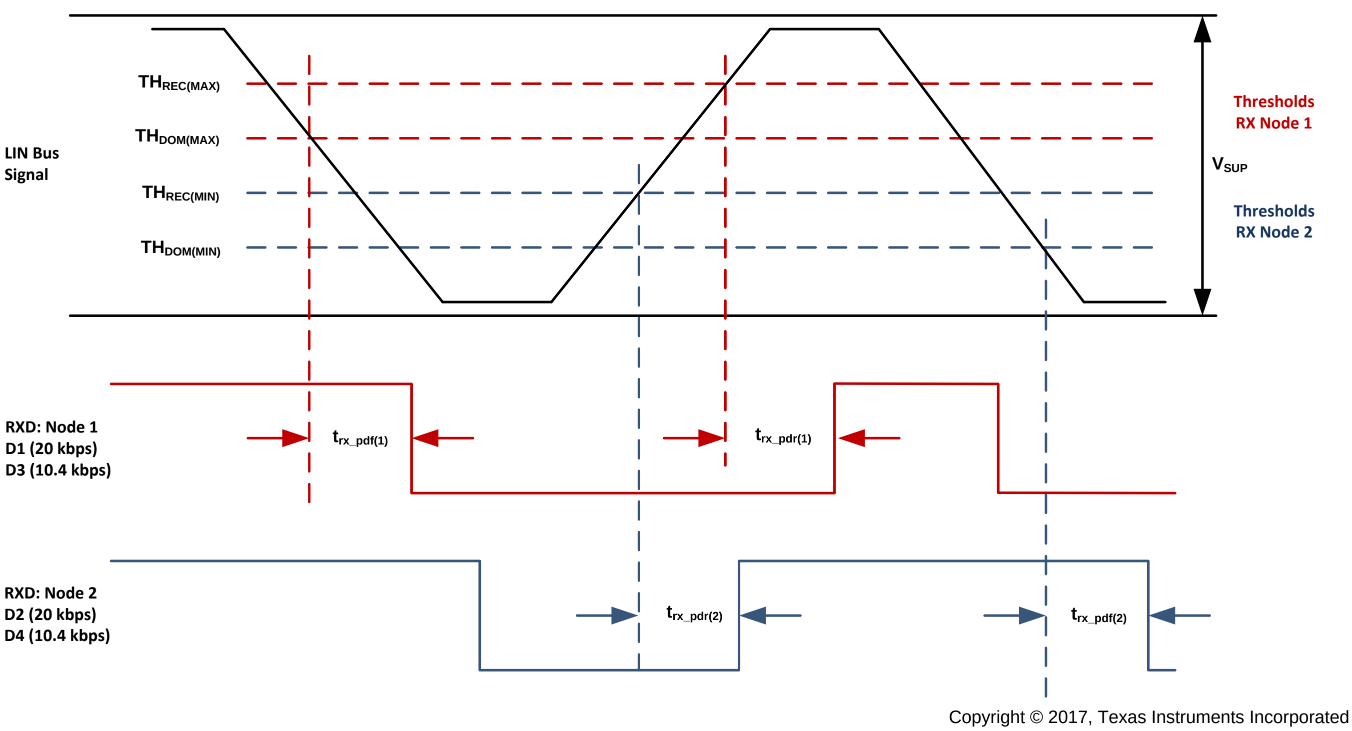


**Figure 14. Propagation Delay**

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## Test Circuit: Diagrams and Waveforms (continued)

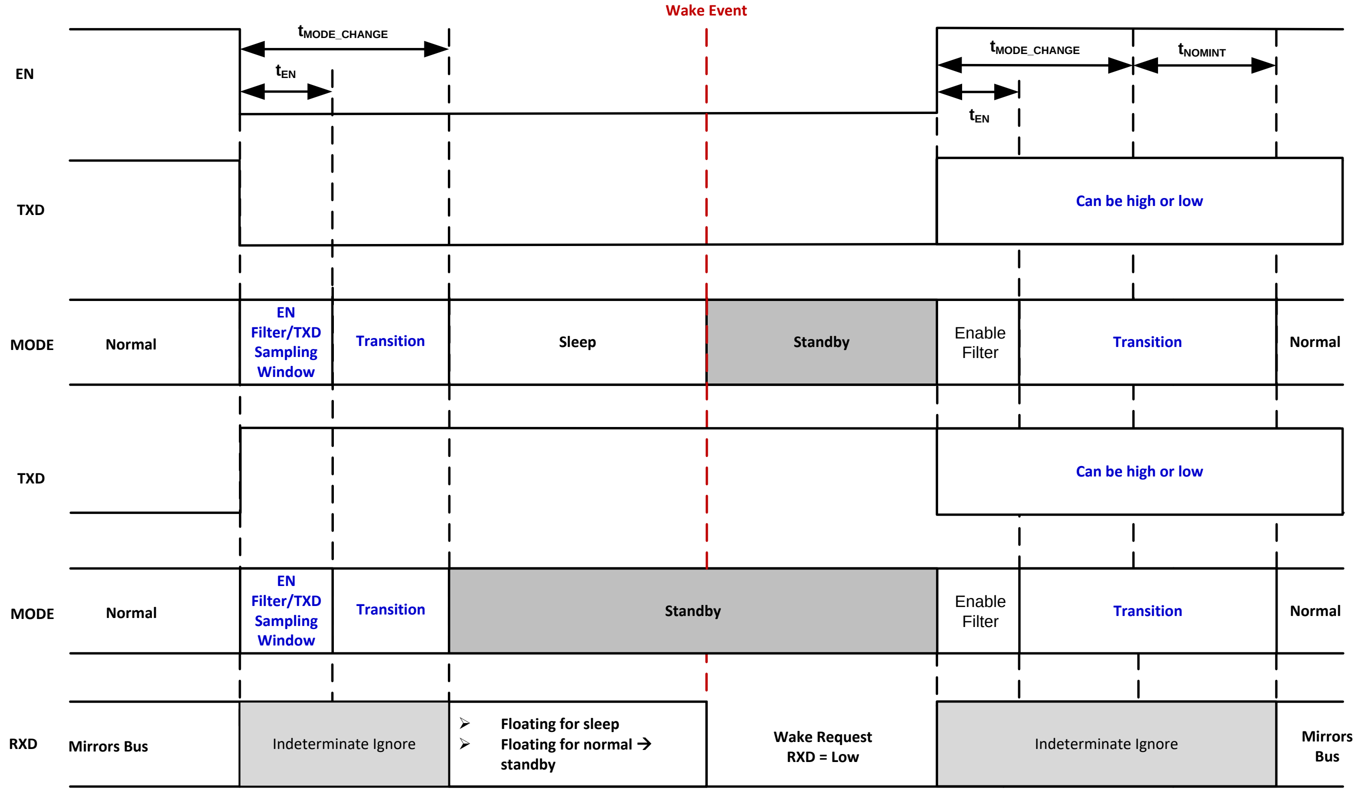


**Figure 15. Mode Transitions**

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## Test Circuit: Diagrams and Waveforms (continued)

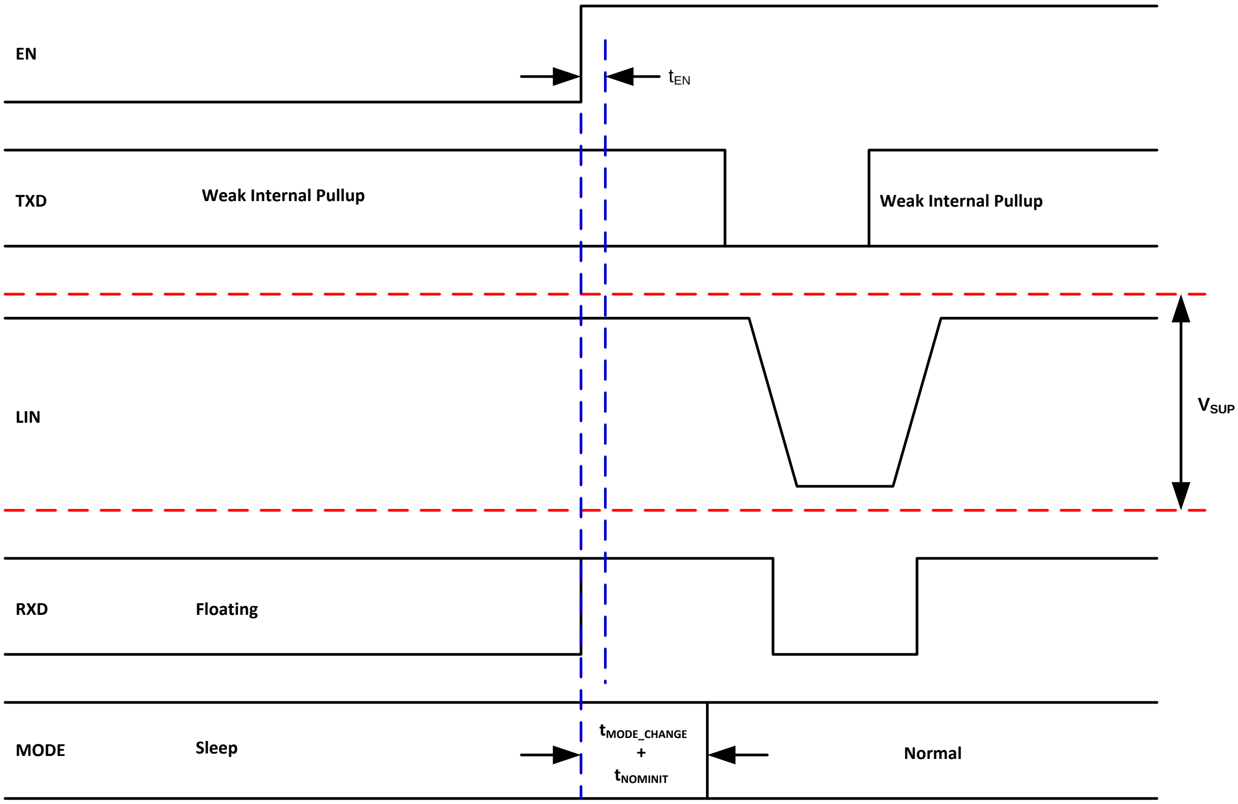


Figure 16. Wakeup Through EN

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ADVANCE INFORMATION

## Test Circuit: Diagrams and Waveforms (continued)

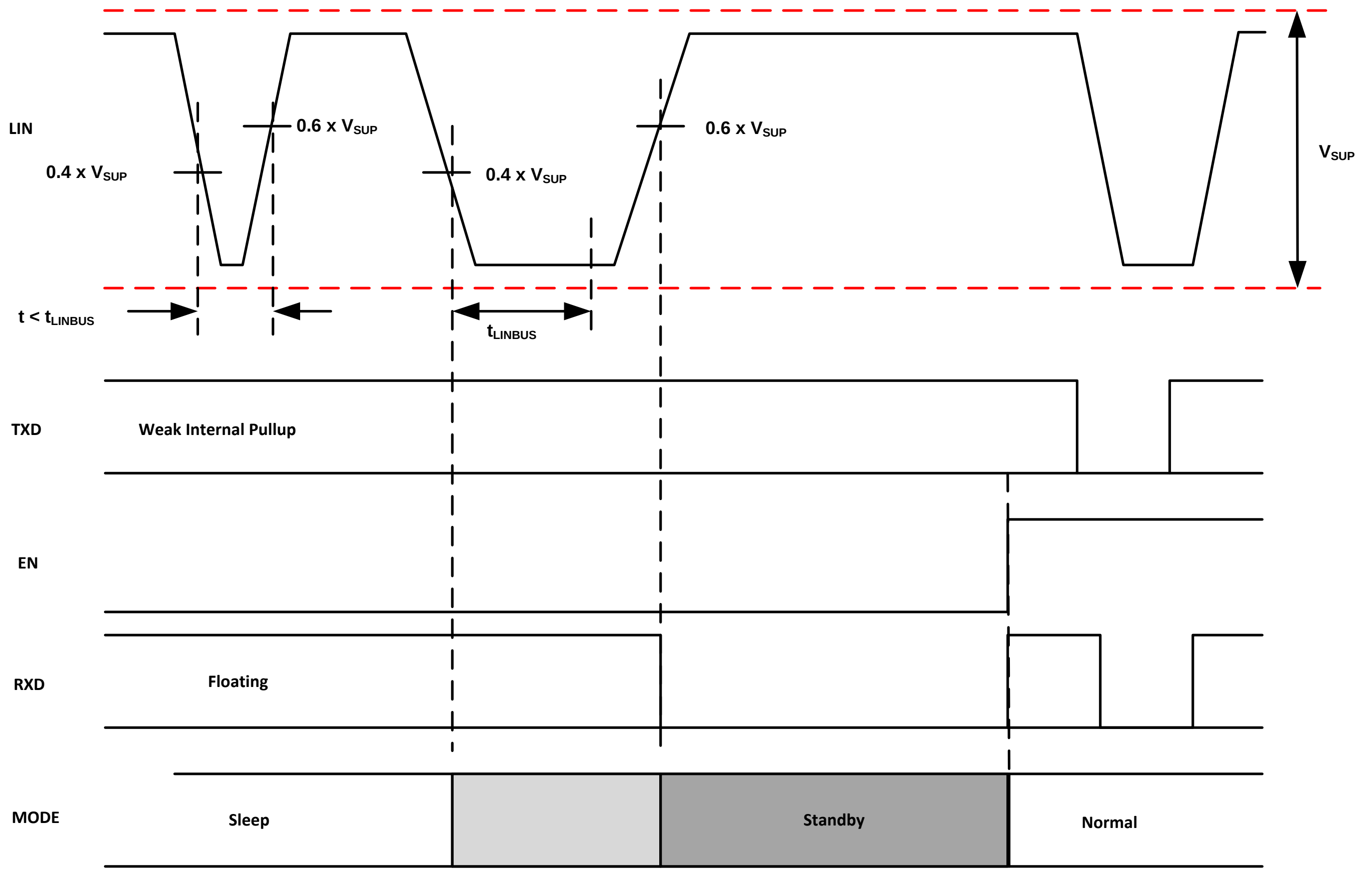


Figure 17. Wakeup through LIN

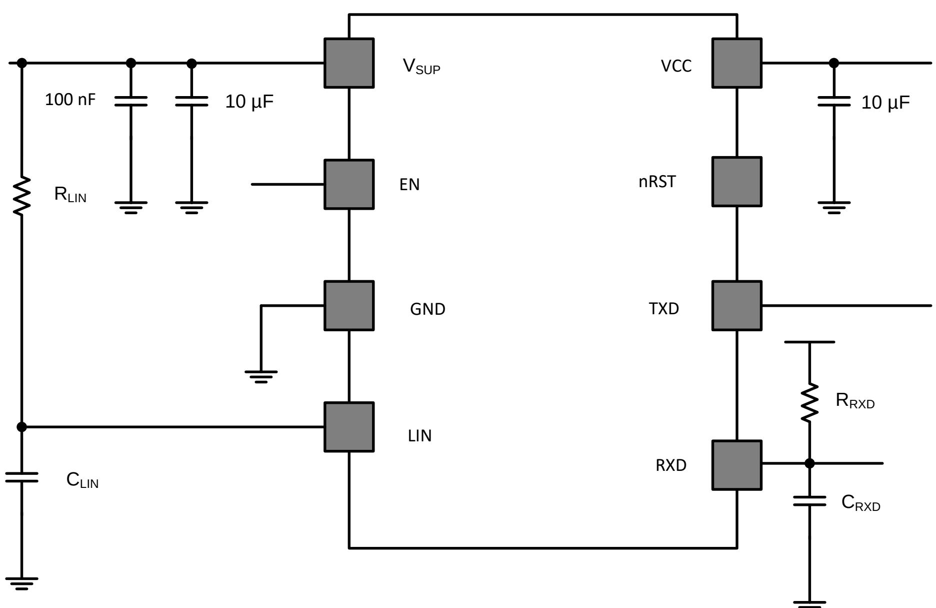


Figure 18. Test Circuit for AC Characteristics

# 9 Detailed Description

## 9.1 Overview

The TLIN1028-Q1 LIN transceiver is a Local Interconnect Network (LIN) physical layer transceiver, compliant to LIN 2.0, LIN 2.1, LIN 2.2, LIN 2.2A and ISO/DIS 17987–4.2 with integrated wake-up and protection features. The LIN bus is a single-wire, bidirectional bus that typically is used in low speed in-vehicle networks with data rates that range up to 20 kbps. The LIN receiver works up to 100 kbps supporting in-line programming. The device converts the LIN protocol data stream on the TXD input into a LIN bus signal using a current-limited wave-shaping driver which reduces electromagnetic emissions (EME). The receiver converts the data stream to logic level signals that are sent to the microprocessor through the open-drain RXD pin. The LIN bus has two states: dominant state (voltage near ground) and recessive state (voltage near battery). In the recessive state, the LIN bus is pulled high by the internal pull-up resistor (45 kΩ) and a series diode.

Ultra-low current consumption is possible using the sleep mode. The TLIN1028 provides two methods to wake up from sleep mode: EN pin and LIN bus. The device integrates a low dropout voltage regulator with a wide input from $V_{SUP}$ providing 5 V ±2% or 3.3 V ±2% with up to 125 mA of current depending upon system implementation. nRST is asserted high when $V_{CC}$ increases above $UV_{CC}$ and stays high as long as $V_{CC}$ is above this threshold.

## 9.2 Functional Block Diagram

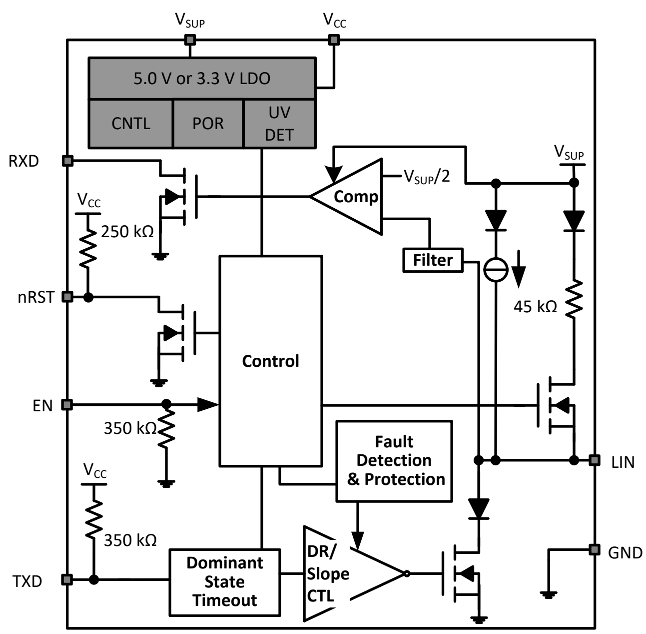


**Figure 19. Functional Block Diagram**

## 9.3 Feature Description

### 9.3.1 LIN (Local Interconnect Network) Bus

This high voltage input or output pin is a single wire LIN bus transmitter and receiver. The LIN pin can survive transient voltages up to 58 V. Reverse currents from the LIN to supply ($V_{SUP}$) are minimized with blocking diodes, even in the event of a ground shift or loss of supply ($V_{SUP}$).

#### *9.3.1.1 LIN Transmitter Characteristics*

The transmitter meets thresholds and AC parameters according to the LIN specification. The transmitter is a low side transistor with internal current limitation and thermal shutdown. During a thermal shutdown condition, the transmitter is disabled to protect the device. There is an internal pull-up resistor with a serial diode structure to $V_{SUP}$, so no external pull-up components are required for the LIN slave mode applications. An external pull-up resistor and series diode to $V_{SUP}$ must be added when the device is used for a master node application.



ADVANCE INFORMATION

## Feature Description (continued)

#### *9.3.1.2 LIN Receiver Characteristics*

The receiver characteristic thresholds are ratio-metric with the device supply pin according to the LIN specification.

The receiver is capable of receiving higher data rates (> 100 kbps) than supported by LIN or SAEJ2602 specifications. This allows the TLIN1028-Q1 to be used for high speed downloads at the end-of-line production or other applications. The actual data rate achievable depends on system time constants (bus capacitance and pull-up resistance) and driver characteristics used in the system.

##### 9.3.1.2.1 Termination

There is an internal pull-up resistor with a serial diode structure to $V_{SUP}$, so no external pull-up components are required for the LIN slave mode applications. An external pull-up resistor (1 kΩ) and a series diode to $V_{SUP}$ must be added when the device is used for master node applications as per the LIN specification.

Figure 20 shows a master node configuration and how the voltage levels are defined

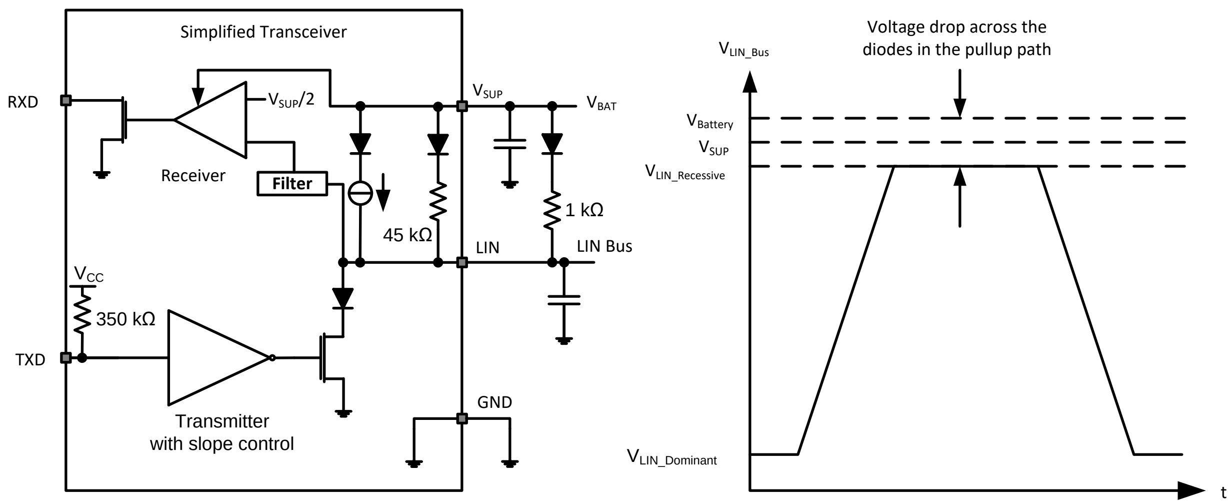


**Figure 20. Master Node Configuration with Voltage Levels**

### 9.3.2 TXD (Transmit Input and Output)

TXD is the interface to the node processors's LIN protocol controller that is used to control the state of the LIN output. When TXD is low, the LIN output is dominant (near ground). When TXD is high, the LIN output is recessive (near $V_{SUP}$). See Figure 20. The TXD input structure is compatible with processors with 3.3 V and 5 $V_I$ and $V_O$. TXD has an internal pull-up resistor. The LIN bus is protected from being stuck dominant through a system failure driving TXD low through the dominant state time-out timer.

### 9.3.3 RXD (Receive Output)

RXD is the interface to the processors LIN protocol controller, which reports the state of the LIN bus voltage. LIN recessive (near $V_{SUP}$) is represented by a high level on the RXD and LIN dominant (near ground) is represented by a low level on the RXD pin. The RXD output structure is an open-drain output stage. This allows the device to be used with 3.3 V and 5 $V_{I/O}$ processors. If the processors RXD pin does not have an integrated pull-up, an external pull-up resistor to the processors I and O supply voltage is required. In standby mode, the RXD pin is driven low to indicate a wake up request from the LIN bus. When going from normal mode to standby mode the RXD pin is released and pulled up to the voltage rail the external pull-up resistor is connected. It is pulled low if a wake event takes place.

### 9.3.4 $V_{SUP}$ (Supply Voltage)

$V_{SUP}$ is the power supply pin. $V_{SUP}$ is connected to the battery through an external reverse battery-blocking diode.

## Feature Description (continued)

The $V_{SUP}$ pin is a high-voltage-tolerant pin. Decoupling capacitor with a value of 100 nF is recommended to be connected close to this pin to better the transient performance. If there is a loss of power at the ECU level, the device has extremely low leakage from the LIN pin, which does not load the bus down. This is optimal for LIN systems in which some of the nodes are unpowered (ignition supplied) while the rest of the network remains powered (battery supplied). When $V_{SUP}$ drops low enough the regulated output drops out of regulation. The LIN bus works with a $V_{SUP}$ as low as 5.5 V, but at a lower voltage, the performance is indeterminate and not ensured. If $V_{SUP}$ voltage level drops enough, it triggers the $UV_{SUP}$, and if it keeps dropping, at some point it passes the POR threshold.

### 9.3.5 GND (Ground)

GND is the device ground connection. The device can operate with a ground shift as long as the ground shift does not reduce the $V_{SUP}$ below the minimum operating voltage. If there is a loss of ground at the ECU level, the device has extremely low leakage from the LIN pin, which does not load the bus down. This is optimal for LIN systems in which some of the nodes are unpowered (ignition supplied) while the rest of the network remains powered (battery supplied).

### 9.3.6 EN (Enable Input)

EN controls the operational modes of the device. When EN is high, the device is in normal operating mode allowing a transmission path from TXD to LIN and from LIN to RXD. When EN is low, the device is put into sleep mode and there are no transmission paths available. EN has an internal pull-down resistor to ensure the device remains in low power mode even if EN is left floating. EN should be held low until $V_{SUP}$ reaches the expected system voltage level.

### 9.3.7 nRST (Reset Output)

The $V_{CC}$ pin is monitored for under voltage events. This pin is internally pulled up to $V_{CC}$ and when an undervoltage event takes place, this pin is pulled low. The pin returns to $V_{CC}$ once the voltage on $V_{CC}$ exceeds the under voltage threshold. nRST is only dependent upon $UV_{CC}$ and not dependent upon the operational mode. If $UV_{CC}$ takes place for longer than $t_{DET(UVCC)}$ nRST is pulled low. If a thermal shutdown event takes place, this pin is pulled to ground.

### 9.3.8 $V_{CC}$ (Supply Output)

The $V_{CC}$ terminal can provide 5 V or 3.3 V with up to 125 mA to power up external devices when using high-k boards and thermal management best practices in order to keep the virtual junction temperature below 150 °C.

### 9.3.9 Protection Features

The device has several protection features that are described as follows.

#### *9.3.9.1 TXD Dominant Time Out (DTO)*

During normal mode, if TXD is inadvertently driven permanently low by a hardware or software application failure, the LIN bus is protected by the dominant state time-out timer. This timer is triggered by a falling edge on the TXD pin. If the low signal remains on TXD for longer than $t_{DST}$, the transmitter is disabled, thus allowing the LIN bus to return to recessive state and communication to resume on the bus. The protection is cleared and the $t_{DST}$ timer is reset by a rising edge on TXD. The TXD pin has an internal pull-up to ensure the device fails to a known recessive state if TXD is disconnected. During this fault, the transceiver remains in normal mode (assuming no change of stated request on EN), the RXD pin reflects the LIN bus and the LIN bus pull-up termination remains on.

#### *9.3.9.2 Bus Stuck Dominant System Fault: False Wake Up Lockout*

The device contains logic to detect bus stuck dominant system faults and prevents the device from waking up falsely during the system fault. Upon entering sleep mode, the device detects the state of the LIN bus. If the bus is dominant, the wake up logic is locked out until a valid recessive on the bus “clears” the bus stuck dominant, preventing excessive current use. Figure 21 and Figure 22 show the behavior of this protection.

ADVANCE INFORMATION

## Feature Description (continued)

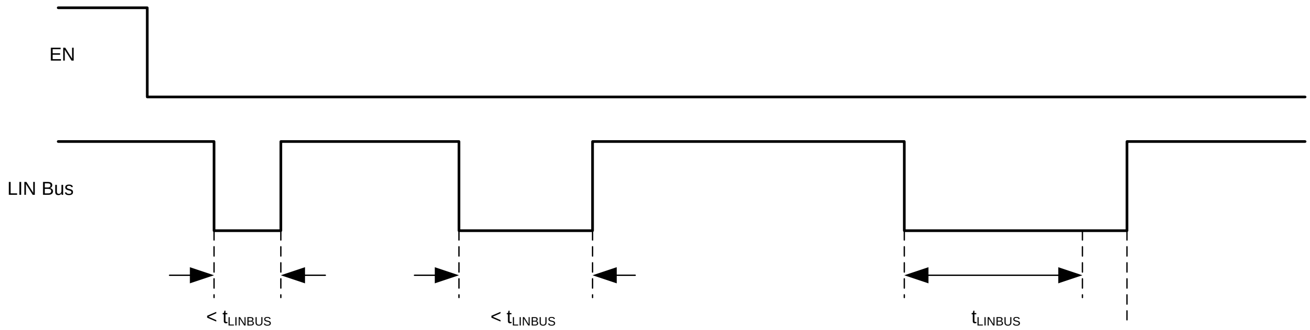


**Figure 21. No Bus Fault: Entering Sleep Mode with Bus Recessive Condition and Wakeup**

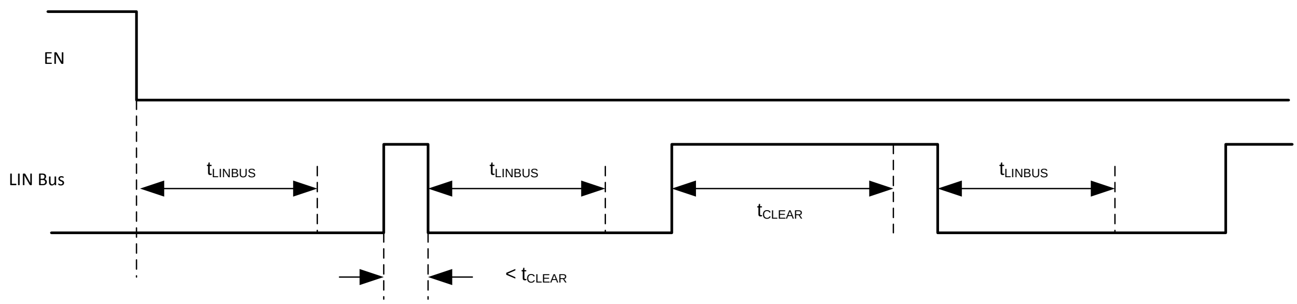


**Figure 22. Bus Fault: Entering Sleep Mode with Bus Stuck Dominant Fault, Clearing, and Wakeup**

#### *9.3.9.3 Thermal Shutdown*

The LIN transmitter is protected by current limiting circuit; however, if the junction temperature of the device exceeds the thermal shutdown threshold, the device puts the LIN transmitter into the recessive state and turns off the $V_{CC}$ regulator. The nRST pin is pulled to ground during a TSD event. Once the over-temperature fault condition has been removed and the virtual junction temperature has cooled beyond the hysteresis temperature, the transmitter is re-enabled. During this fault the device enters a TSD off mode. Once the junction temperature cools, the device enters standby mode as per the state diagram.

#### *9.3.9.4 Under Voltage on $V_{SUP}$*

The device contains a power-on reset circuit to avoid false bus messages during under voltage conditions when $V_{SUP}$ is less than $UV_{SUP}$.

#### *9.3.9.5 Unpowered Device and LIN Bus*

In automotive applications, some LIN nodes in a system can be unpowered (ignition supplied) while others in the network remain powered by the battery. The device has extremely low unpowered leakage current from the bus, so an unpowered node does not affect the network or load it down.

### 9.4 Device Functional Modes

The TLIN1028-Q1 has three functional modes of operation, normal, sleep, and standby. The next sections describes these modes as well as how the device moves between the different modes. Figure 23 graphically shows the relationship while Table 1 shows the state of pins.

**Table 1. Operating Modes**

| Mode | EN | RXD | LIN BUS Termination | Transmitter | nRST | Comment |
|---|---|---|---|---|---|---|
| Sleep | Low | Floating | Weak Current pull-up | Off | Ground | nRST is internally connected to the LDO output which in sleep mode is pulled to ground |

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## Device Functional Modes (continued)

**Table 1. Operating Modes (continued)**

| Mode | EN | RXD | LIN BUS Termination | Transmitter | nRST | Comment |
|---|---|---|---|---|---|---|
| Standby Init | Low | Floating | 45 kΩ (typical) | Off | Ramping | nRST is internally connected to the LDO output which in standby init mode is pulled low until VCC raises beyond $UV_{CC}$ threshold. |
| Standby from SLP | Low | Low | 45 kΩ (typical) | Off | $V_{CC}$ | Wake up event detected, waiting on processors to set EN<br>nRST comes on to $V_{CC}$ once thresholds are met. |
| Standby from Norm | Low | Floating | 45 kΩ (typical) | Off | $V_{CC}$ | LDO is on and RXD is floating. If a wake event takes place RXD is pulled low. |
| Normal | High | LIN Bus Data | 45 kΩ (typical) | On | $V_{CC}$ | LIN transmission up to 20 kbps |
| TSD Off | NA | Floating | 45 kΩ (typical) | Off | Ground | nRST is pulled low as the LDO is turned off which means $UV_{CC}$ threshold has been met. |

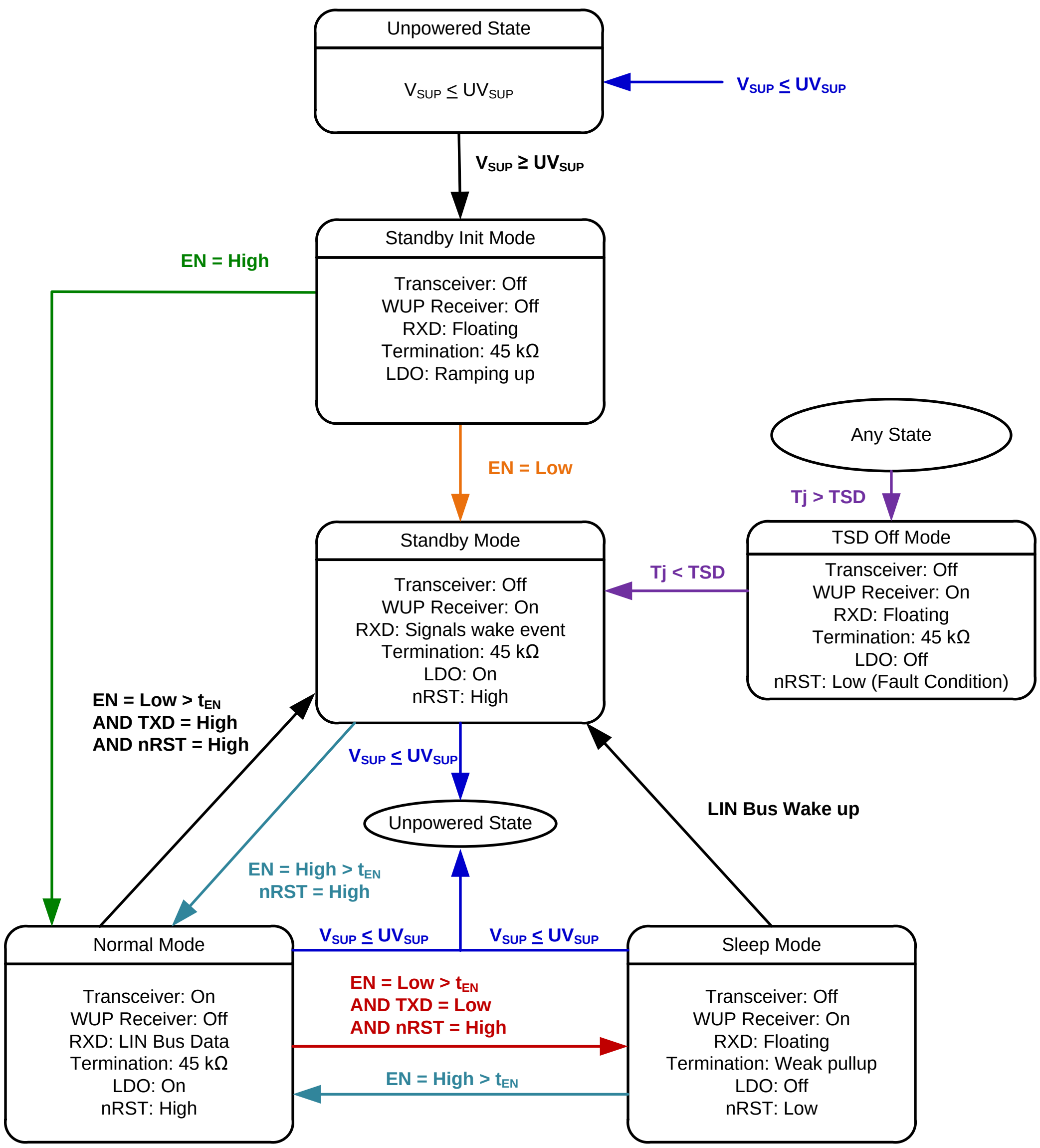



**Figure 23. Operating State Diagram**

### 9.4.1 Normal Mode

If the EN pin is high after the device enters standby init mode it enters normal mode. If EN is low, it enters standby mode. In normal operational mode, the receiver and transmitter are active and the LIN transmission up to the LIN specified maximum of 20 kbps is supported. The receiver detects the data stream on the LIN bus and outputs it on RXD for the LIN controller. A recessive signal on the LIN bus is a digital high and a dominant signal on the LIN bus is a digital low. The driver transmits input data from TXD to the LIN bus. Normal mode is entered as EN transitions high while the device is in sleep or standby mode for > $t_{EN}$. Once EN has been high for $t_{EN}$ the device enters normal mode after $t_{MODE\_CHANGE}$ and $t_{NOMINIT}$ times.

### 9.4.2 Sleep Mode

Sleep Mode is the power saving mode for the TLIN1028-Q1. Even with extremely low current consumption in this mode, the device can still wake up from the LIN bus through a wake-up signal or if EN is set high for > $t_{EN}$. The wake-up events must be active for the respective time periods ($t_{LINBUS}$).

While the device is in sleep mode, the following conditions exist:

- The LIN bus driver is disabled and the internal LIN bus termination is switched off (to minimize power loss if LIN is short circuited to ground). However, the weak current pull-up is active to prevent false wake up events in case an external connection to the LIN bus is lost.
- The normal receiver is disabled.
- EN input and LIN wake up receiver are active.

### 9.4.3 Standby Mode

Standby mode is entered either by a wake up event through LIN bus while the device is in sleep mode or by the EN pin while in normal mode. From normal mode EN must be low for > $t_{EN}$ and TXD and nRST are high. RXD pin in standby mode is dependent upon how standby mode was entered. If entered from normal mode or power up, RXD floats until a wake event takes place at which time it is pulled low. If entered from sleep mode, RXD is pulled low to indicate a wake event. See *Standby Mode Application Note* for more application information.

During power up, if EN is low the device goes into standby mode, and if EN is high, the device goes into normal mode. EN has an internal pull-down resistor ensuring EN is pulled low if the pin is left floating in the system.

### 9.4.4 Wake Up Events

There are two ways to wake up from sleep mode:

- Remote wake up initiated by the falling edge of a recessive (high) to dominant (low) state transition on the LIN bus where the dominant state is held for the $t_{LINBUS}$ filter time. After this $t_{LINBUS}$ filter time has been met and a rising edge on the LIN bus going from dominant state to recessive state initiates a remote wake up event eliminating false wake ups from disturbances on the LIN bus or if the bus is shorted to ground.
- Local wake up through EN being set high for longer than $t_{EN}$.

#### *9.4.4.1 Wake Up Request (RXD)*

When the TLIN1028-Q1 encounters a wake up event from the LIN bus, RXD goes low and the device transitions to standby mode until EN is reasserted high and the device enters normal mode. Once the device enters normal mode, the RXD pin releases the wake up request signal and the RXD pin then reflects the receiver output from the LIN bus.

### 9.4.5 Mode Transitions

When the device is transitioning between modes, the device needs the time $t_{MODE\_CHANGE}$ and $t_{NOMINT}$ to allow the change to fully propagate from the EN pin through the device into the new state.

### 9.4.6 Voltage Regulator

The device has an integrated high-voltage LDO that operates over a 5.5 V to 28 V input voltage range for both 3.3 V and 5 V $V_{CC}$. The device has an output current capability of 125 mA and support fixed output voltages of 3.3 V (TLIN10283-Q1) or 5 V (TLIN10285-Q1). It features thermal shutdown and short-circuit protection to prevent damage during over-temperature and over-current conditions

#### 9.4.6.1 $V_{CC}$

The $V_{CC}$ pin is the regulated output based on the required voltage. The regulated voltage accuracy is ± 2%. The output is current limited. In the event that the regulator drops out of regulation, the output tracks the input minus a drop based on the load current. When the input voltage drops below the $UV_{SUP}$ threshold, the regulator shuts down until the input voltage returns above the $UV_{SUPR}$ level. The device monitors situations where $V_{CC}$ may drop below the $UV_{CC}$ level thus causing the nRST pin to be pulled low.

#### 9.4.6.2 Output Capacitance Selection

For stable operation over the full temperature range and with load currents up to 125 mA on $V_{CC}$ a certain capacitance is expected and depends upon the minimum load current. To support no load to full load a value of 10 µF and ESR smaller than 2 Ω is needed. For 500 µA to full load an 1 µF capacitance can be used. The low ESR recommendation is to improve the load transient performance.

#### 9.4.6.3 Low-Voltage Tracking

At low input voltages, the regulator drops out of regulation and the output voltage tracks input minus a voltage based on the load current (IL) and switch resistor. This tracking allows for a smaller input capacitance and can possibly eliminate the need for a boost converter during cold-crank conditions.

#### 9.4.6.4 Power Supply Recommendation

The device is designed to operate from an input-voltage supply range between 5.5 V and 28 V. This input supply must be well regulated. If the input supply is located more than a few inches from the device. The recommended minimum capacitance at the pin is 100 nF . The max voltage range is for the LIN functionality. Exceeding 24V for the LDO reduces the effective current sourcing capability due to thermal considerations.

# 10 Application and Implementation

**NOTE**

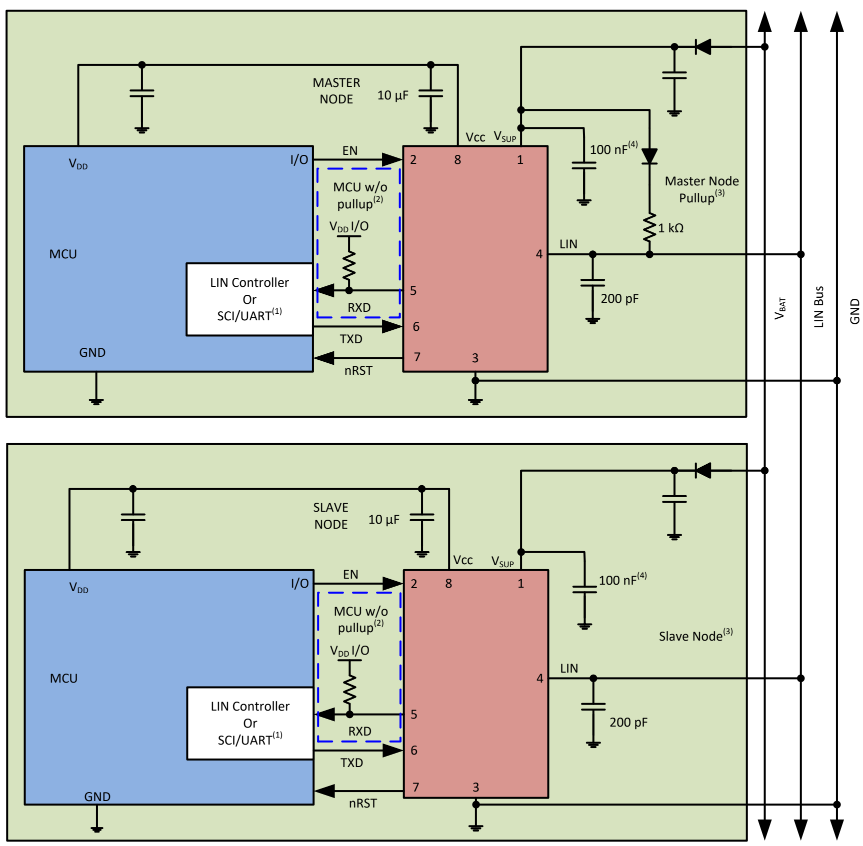
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 10.1 Application Information

The TLIN1028-Q1 can be used as both a slave device and a master device in a LIN network. The device comes with the ability to support remote wake up request. It can provide the power to the local processor.

## 10.2 Typical Application

The device comes with an integrated 45 kΩ pull-up resistor and series diode for slave applications. For master applications an external 1 kΩ pull-up resistor with series blocking diode can be used. Figure 24 shows the device being used in both master and slave applications.




(1) If RXD on MCU or LIN slave has internal pullup; no external pullup resistor is needed.
(2) If RXD on MCU or LIN slave does not have an internal pullup requires external pullup resistor.
(3) Master node applications require and external 1 kΩ pullup resistor and serial diode.
(4) Decoupling capacitor values are system dependent but usually have 100 nF, 1 µF and ≥10 µF

**Figure 24. Typical LIN Bus**

## Typical Application (continued)

### 10.2.1 Design Requirements

#### *10.2.1.1 Normal Mode Application Note*

When using the TLIN1028-Q1 in systems which are monitoring the RXD pin for a wake up request, special care should be taken during the mode transitions. The output of the RXD pin is indeterminate for the transition period between states as the receivers are switched. The application software should not look for an edge on the RXD pin indicating a wake up request until $t_{MODE\_CHANGE}$. This is shown in When transitioning to normal mode there is an initialization period shown as $t_{NOMINIT}$.

#### *10.2.1.2 Standby Mode Application Note*

If the TLIN1028-Q1 detects an under voltage on $V_{SUP}$, the RXD pin transitions low and would signal to the software that the device is in standby mode and should be returned to sleep mode for the lowest power state.

#### *10.2.1.3 TXD Dominant State Timeout Application Note*

The maximum dominant TXD time allowed by the TXD dominant state time out limits the minimum possible data rate of the device. The LIN protocol has different constraints for master and slave applications; thus, there are different maximum consecutive dominant bits for each application case and thus different minimum data rates.

### 10.2.2 Detailed Design Procedures

RXD on processors or LIN slave has internal pull-up; no external pull-up resistor is need. RXD on processors or LIN slave without internal pull-up requires external pull-up resistor. Master node applications require and external 1 kΩ pull-up resistor and serial diode.

## 11 Power Supply Recommendations

The TLIN1028-Q1 was designed to operate directly off a car battery, or any other DC supply ranging from 5.5 V to 28 V . A 100 nF decoupling capacitor should be placed as close to the $V_{SUP}$ pin of the device as possible.

# 12 Layout

PCB design should start with design of the protection and filtering circuitry because ESD and EFT have a wide frequency bandwidth from approximately 3 MHz to 3 GHz, high frequency layout techniques must be applied during PCB design. Placement at the connector also prevents these noisy events from propagating further into the PCB and system.

## 12.1 Layout Guidelines

- **Pin 1 ($V_{SUP}$):** This is the supply pin for the device. A 100 nF decoupling capacitor should be placed as close to the device as possible.
- **Pin 2 (EN):** EN is an input pin that is used to place the device in a low power sleep mode. If this feature is not used, the pin should be pulled high to the regulated voltage supply of the microprocessor through a series resistor, values between 1 kΩ and 10 kΩ. Additionally, a series resistor may be placed on the pin to limit current on the digital lines in the event of an over voltage fault.
- **Pin 3 (GND):** This is the ground connection for the device. This pin should be tied to the ground plane through a short trace with the use of two vias to limit total return inductance.
- **Pin 4 (LIN):** This pin connects to the LIN bus. For slave applications, a 200 pF capacitor to ground is implemented. For master applications, an additional series resistor and blocking diode should be placed between the LIN pin and the $V_{SUP}$ pin. See Figure 24
- **Pin 5 (RXD):** The pin is an open drain output and requires and external pull-up resistor in the range of 1 kΩ to 10 kΩ to function properly. If the microprocessor paired with the transceiver does not have an integrated pull-up, an external pull-up resistor should be placed on RXD. If RXD is connected to the $V_{CC}$ pin a higher pull-up resistor value can be used to reduce standby current.
- **Pin 6 (TXD):** The TXD pin is the transmit input signal to the device from the processors. A series resistor can be placed to limit the input current to the device in the event of an over voltage on this pin. A capacitor to ground can be placed close to the input pin of the device to filter noise.
- **Pin 7 (nRST):** This pin connects to the processors as a reset out.
- **Pin 8 ($V_{CC}$):** Output source, either 3.3 V or 5 V depending upon the version of the device.

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**NOTE**

All ground and power connections should be made as short as possible and use at least two vias to minimize the total loop inductance.

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ADVANCE INFORMATION

## 12.2 Layout Example

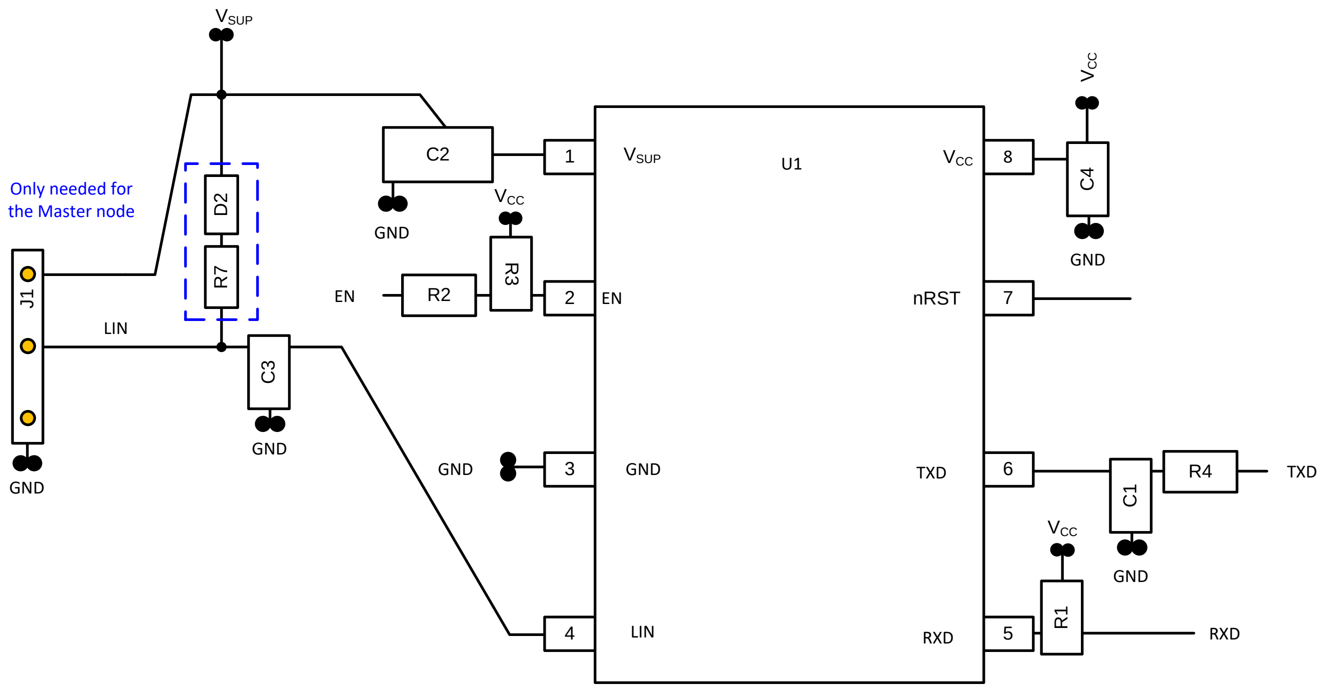


Figure 25. Layout Example

ADVANCE INFORMATION

# 13 Device and Documentation Support

## 13.1 Documentation Support

### 13.1.1 Related Documentation

For related documentation see the following:

LIN Standards:

- ISO/DIS 17987-1.2: Road vehicles -- Local Interconnect Network (LIN) -- Part 1: General information and use case definition
- ISO/DIS 17987-4.2: Road vehicles -- Local Interconnect Network (LIN) -- Part 4: Electrical Physical Layer (EPL) specification 12V/24V
- SAEJ2602-1: LIN Network for Vehicle Applications
- LIN2.0, LIN2.1, LIN2.2 and LIN2.2A specification

EMC requirements:

- SAEJ2962-2: TBD
- HW Requirements for CAN, LIN, FR V1.3: German OEM requirements for LIN
- ISO 10605: Road vehicles - Test methods for electrical disturbances from electrostatic discharge
- ISO 11452-4:2011: Road vehicles - Component test methods for electrical disturbances from narrowband radiated electromagnetic energy - Part 4: Harness excitation methods
- ISO 7637-1:2015: Road vehicles - Electrical disturbances from conduction and coupling - Part 1: Definitions and general considerations
- ISO 7637-3: Road vehicles - Electrical disturbances from conduction and coupling - Part 3: Electrical transient transmission by capacitive and inductive coupling via lines other than supply lines
- IEC 62132-4:2006: Integrated circuits - Measurement of electromagnetic immunity 150 kHz to 1 GHz - Part 4: Direct RF power injection method
- IEC 61000-4-2
- IEC 61967-4
- CISPR25

Conformance Test requirements:

- ISO/DIS 17987-7.2: Road vehicles -- Local Interconnect Network (LIN) -- Part 7: Electrical Physical Layer (EPL) conformance test specification
- SAEJ2602-2: LIN Network for Vehicle Applications Conformance Test

*TLINx441 LDO Performance*, SLLA427

## 13.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

## 13.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

ADVANCE INFORMATION

### 13.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 13.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

### 13.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 13.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PTLIN10285DRBRQ1 | ACTIVE | SON | DRB | 8 | 3000 | TBD | Call TI | Call TI | -40 to 125 | | Samples |
| TLIN10283DDARQ1 | PREVIEW | SO PowerPAD | DDA | 8 | 2500 | TBD | Call TI | Call TI | -40 to 125 | | |
| TLIN10283DRBRQ1 | PREVIEW | SON | DRB | 8 | 3000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | TLN83 | |
| TLIN10283DRQ1 | PREVIEW | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TL083 | |
| TLIN10285DDARQ1 | PREVIEW | SO PowerPAD | DDA | 8 | 2500 | TBD | Call TI | Call TI | -40 to 125 | | |
| TLIN10285DRBRQ1 | PREVIEW | SON | DRB | 8 | 3000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | TLN85 | |
| TLIN10285DRQ1 | PREVIEW | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TL085 | |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.