



Low-Power, High-Speed CMOS Analog Switches

FEATURES

- 44-V Supply Max Rating
- ± 15 -V Analog Signal Range
- On-Resistance— $r_{DS(on)}$: 23 Ω
- Low Leakage— $I_{D(on)}$: 40 pA
- Fast Switching— t_{ON} : 100 ns
- Upgrade to DG401/403/405
- TTL, CMOS Compatible
- Single Supply Capability

BENEFITS

- Wide Dynamic Range
- Break-Before-Make Switching Action (DG403B only)
- Simple Interfacing

APPLICATIONS

- Audio and Video Switching
- Sample-and-Hold Circuits
- Test Equipment
- PBX, PABX

DESCRIPTION

The DG401B/403B/405B monolithic analog switches are replacements for the popular DG401/403/405 analog switches and provide improved performance, combining high speed (t_{ON} : 100 ns, typ) with low power consumption make the DG401B series ideal for portable and battery powered applications.

Built on the Vishay Siliconix proprietary high-voltage silicon-gate process to achieve high voltage rating and superior switch on/off performance, break-before-make is guaranteed for the SPDT configurations.

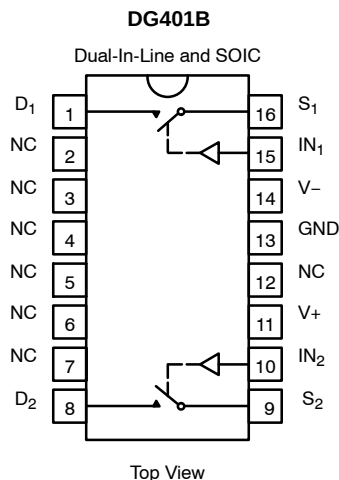
Each switch conducts equally well in both directions when on, and blocks up to 30 V peak-to-peak when off. On-resistance is very flat over the full ± 15 -V analog range. The DG401B has

two independent SPST switches. The DG403B has four SPST switches in NO/NC combinations. The DG405B has four switches in two SPST pairs. (See Functional Block Diagrams and Pin Configurations on pages 1 and 2.)

The DG401B/403B/405B is available in both 16-pin plastic dip and 16-pin SOIC packages.

As a committed partner to the community and the environment, Vishay Siliconix manufactures this product with the lead (Pb)-free device terminations. For analog switching products manufactured with 100% matte tin device terminations, the lead (Pb)-free “—E3” suffix is being used as a designator.

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



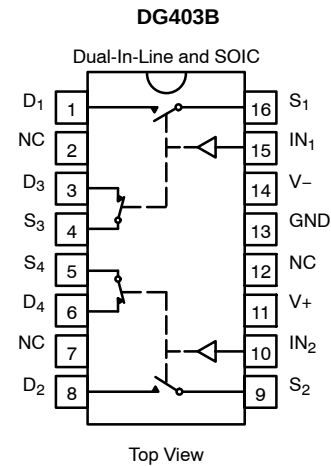
Two SPST Switches per Package

TRUTH TABLE	
Logic	Switch
0	OFF
1	ON

Logic “0” ≤ 0.8 V
Logic “1” ≥ 2.4 V



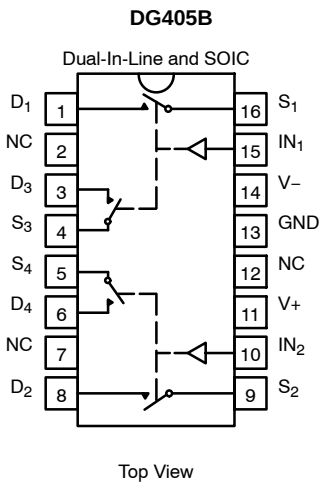
FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



Four SPST Switches in Two Pairs per Package

TRUTH TABLE		
Logic	SW ₁ , SW ₂	SW ₃ , SW ₄
0	OFF	ON
1	ON	OFF

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V



Four SPST Switches in Two Pairs per Package

TRUTH TABLE	
Logic	Switch
0	OFF
1	ON

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V

ORDERING INFORMATION			
Standard Commercial Part Number	Lead (Pb)-Free Commercial Part Number	Package	Temperature Range
DG401BDJ	DG401BDJ—E3	16-Pin Plastic Dip	-40 to 85°C
DG403BDJ	DG403BDJ—E3		
DG405BDJ	DG405BDJ—E3		
DG401BDY	DG401BDY—E3	16-Pin Narrow SOIC	
DG403BDY	DG403BDY—E3		
DG405BDY	DG405BDY—E3		
DG401BDY-T1	DG401BDY-T1—E3	16-Pin Narrow SOIC With Tape and Reel	
DG403BDY-T1	DG403BDY-T1—E3		
DG405BDY-T1	DG405BDY-T1—E3		



ABSOLUTE MAXIMUM RATINGS

V_+ to V_-	44 V
GND to V_-	25 V
Digital Inputs ^a V_S , V_D	(V_-) – 0.3 V to (V_+) +0.3 V or 30 mA, whichever occurs first
Current (Any Terminal) Continuous	30 mA
Current, S or D (Pulsed 1 ms 10% duty)	100 mA
Storage Temperature (DJ, DY Suffix)	–65 to 125°C

Power Dissipation (Package)^b

16-Pin Plastic DIP ^c	450 mW
16-Pin SOIC ^d	600 mW

Notes:

- Signals on S_X , D_X , or IN_X exceeding V_+ or V_- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- All leads welded or soldered to PC Board.
- Derate 6 mW/°C above 75°C
- Derate 7.6 mW/°C above 75°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

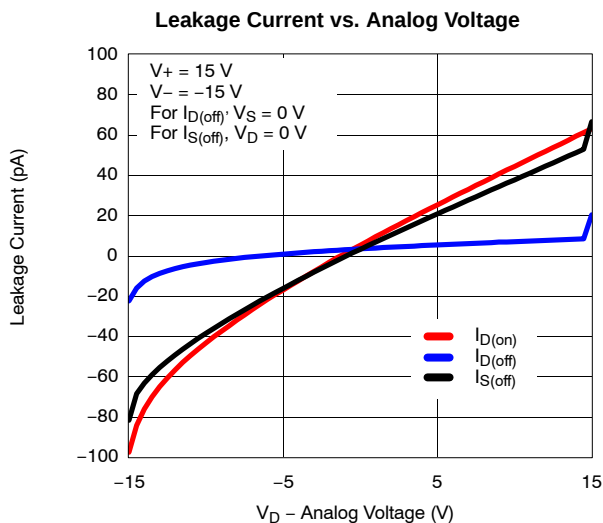
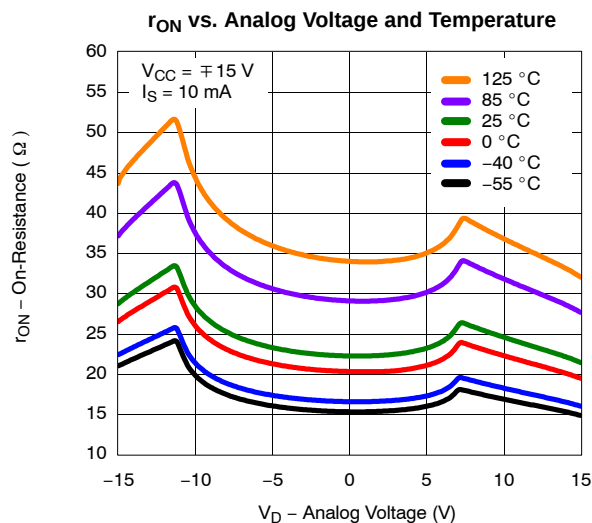
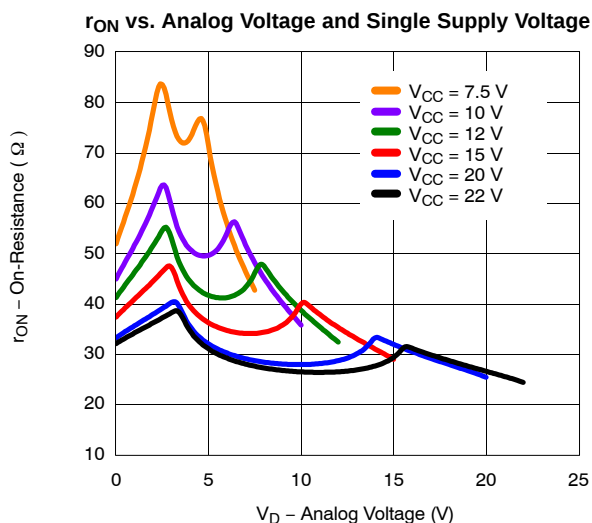
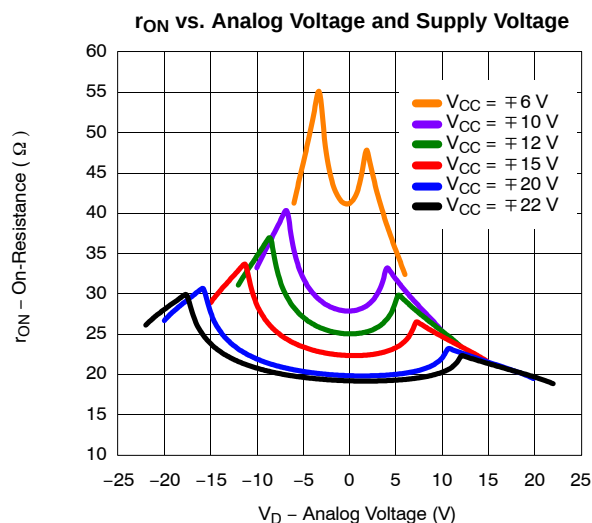
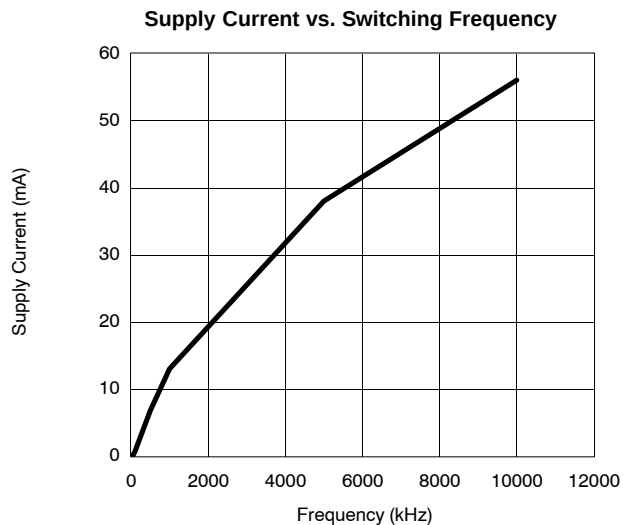
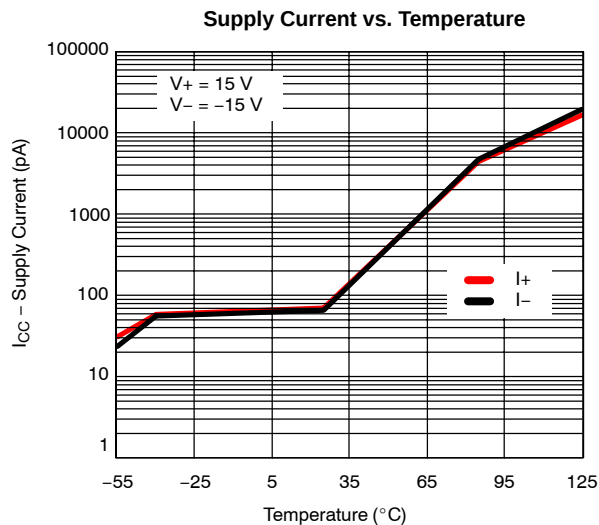
SPECIFICATIONS^a

Parameter	Symbol	Test Conditions Unless Specified V+ = 15 V, V- = -15 V, VIN = 2.4 V, 0.8 V ^f	Temp ^b	Limits -40 to 85°C			Unit
				Min ^d	Typ ^c	Max ^d	
Analog Switch							
Analog Signal Range ^e	VANALOG		Full	-15		15	V
Drain-Source On-Resistance	rDS(on)	IS = -10 mA, VD = ±10 V V+ = 13.5 V, V- = -13.5 V	Room Full		23	45 55	Ω
Δ Drain-Source On-Resistance	ΔrDS(on)	IS = -10 mA, VD = ±5 V, 0 V V+ = 16.5 V, V- = -16.5 V	Room Full		0.72	3 5	
Switch Off Leakage Current	IS(off)	V+ = 16.5, V- = -16.5 V VD = ±15.5 V, VS = ∓15.5 V	Room Hot	-0.5 -5	-0.01	0.5 5	nA
	ID(off)		Room Hot	-0.5 -5	-0.01	0.5 5	
Channel On Leakage Current	ID(on)	V+ = 16.5 V, V- = -16.5 V VS = VD = ±15.5 V	Room Hot	-1 -10	-0.04	1 10	
Digital Control							
Input Current VIN Low	IL	VIN under test = 0.8 V, All Other = 2.4 V	Full	-1	0.005	1	μA
Input Current VIN High	IH	VIN under test = 2.4 V, All Other = 0.8 V	Full	-1	0.005	1	
Dynamic Characteristics							
Turn-On Time	tON	RL = 300 Ω , CL = 35 pF See Figure 2	Room		100	150	ns
Turn-Off Time	tOFF		Room		60	100	
Break-Before-Make Time Delay (DG403B)	tD	RL = 300 Ω , CL = 35 pF	Room	5	12		
Charge Injection	Q	CL = 10,000 pF, Vgen = 0 V, Rgen = 0 Ω	Room		60		pC
Off Isolation Reject Ratio	OIRR	RL = 100 Ω , CL = 5 pF f = 1 MHz	Room		-81.7		dB
Channel-to-Channel Crosstalk	XTALK		Room		-94.8		
Source Off Capacitance	CS(off)	f = 1 MHz, VS = 0 V	Room		12		pF
Drain Off Capacitance	CD(off)		Room		12		
Channel On Capacitance	CD, CS(on)		Room		39		
Power Supplies							
Positive Supply Current	I+	V+ = 16.5 V, V- = -16.5 V VIN = 0 or 5 V	Room Full		0.250	0.5 1	mA
Negative Supply Current	I-		Room Full	-0.5 -1	0.25		
Ground Current	IGND		Room Full	-0.5 -1	0.25		

Notes:

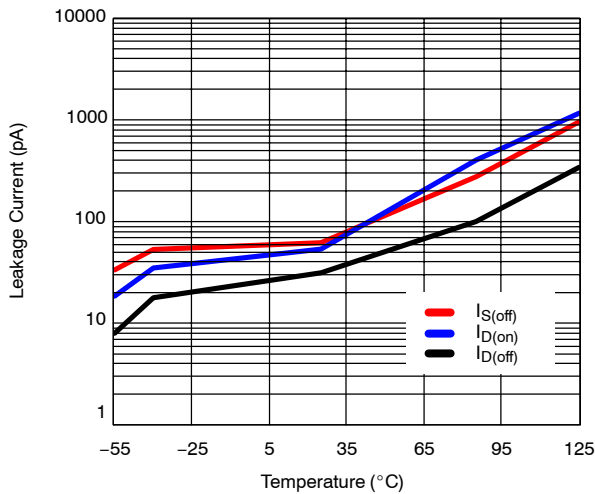
- Refer to PROCESS OPTION FLOWCHART.
- Room = 25°C, Full = as determined by the operating temperature suffix.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Guaranteed by design, not subject to production test.
- V_{IN} = input voltage to perform proper function.

TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)

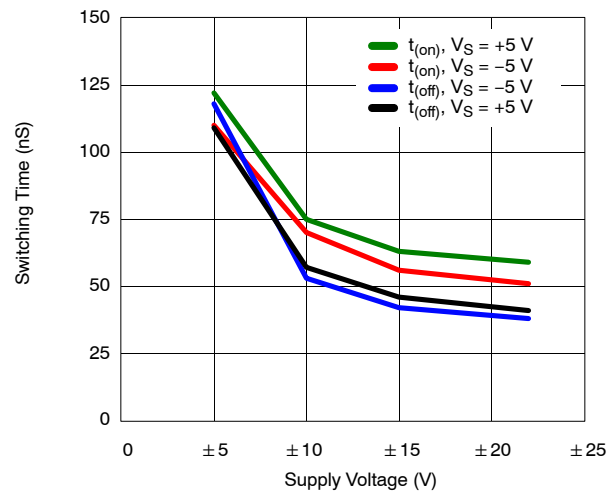


**TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)**

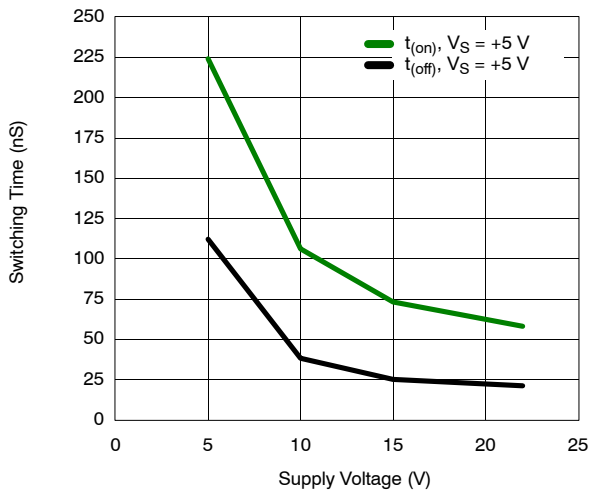
Leakage Current vs. Temperature



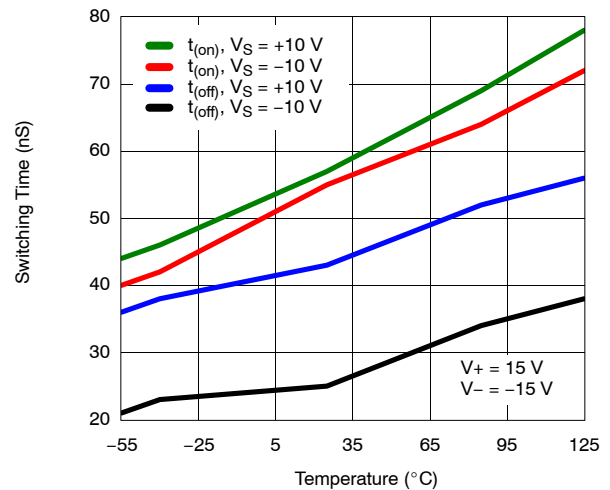
Switching Time vs. Supply Voltage



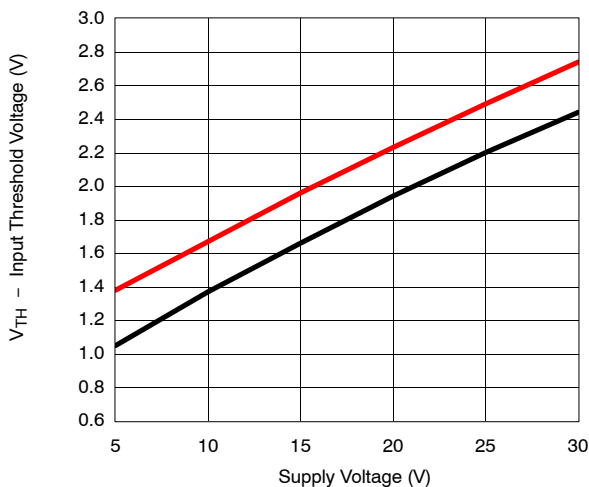
Switching Time vs. Single Supply Voltage



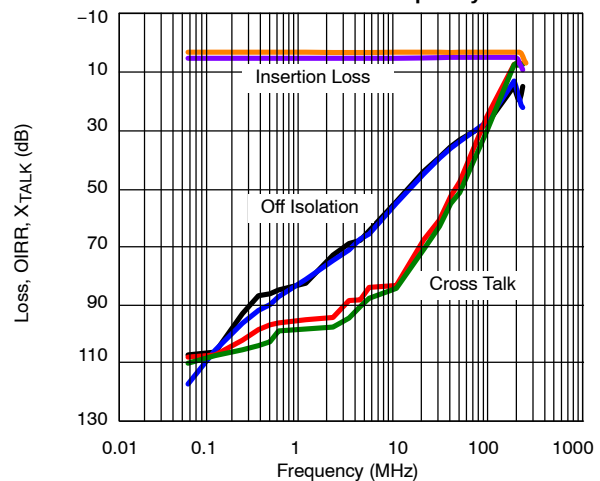
Switching Time vs. Temperature



Input Switching Threshold vs. Supply Voltage



Insertion Loss, Off-Isolation Crosstalk vs. Frequency





SCHEMATIC DIAGRAM (TYPICAL CHANNEL)

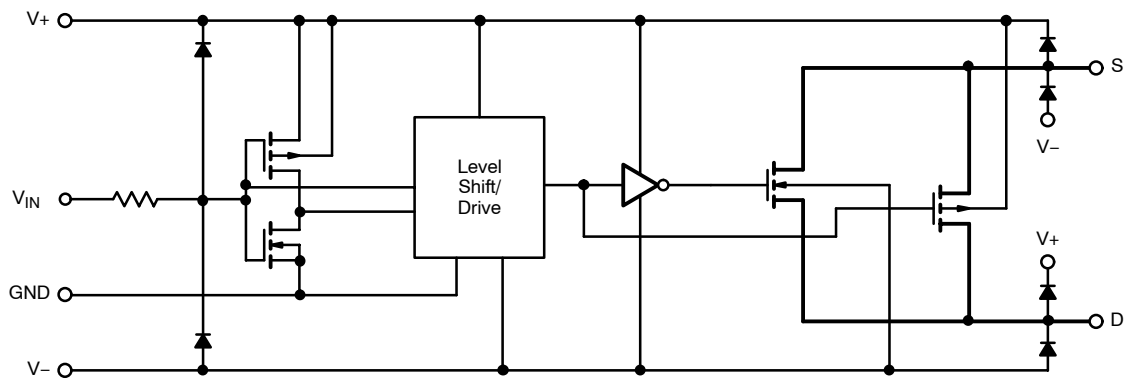
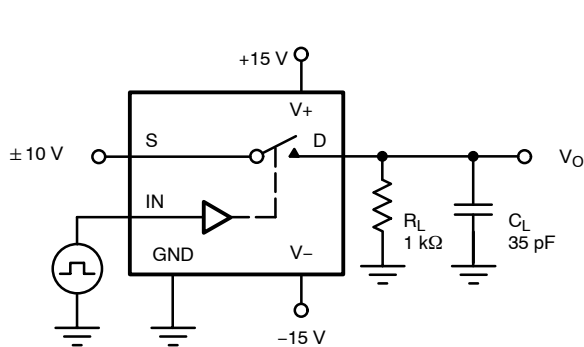


FIGURE 1.

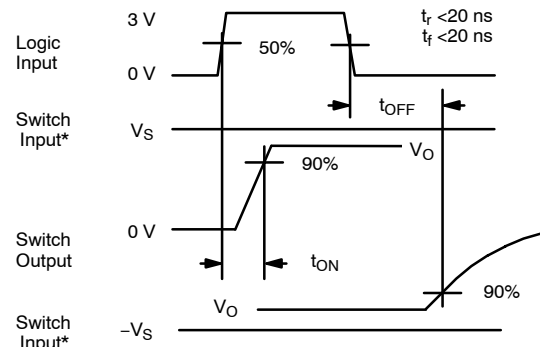
TEST CIRCUITS

V_O is the steady state output with the switch on. Feedthrough via switch capacitance may result in spikes at the leading and trailing edge of the output waveform.



C_L (includes fixture and stray capacitance)

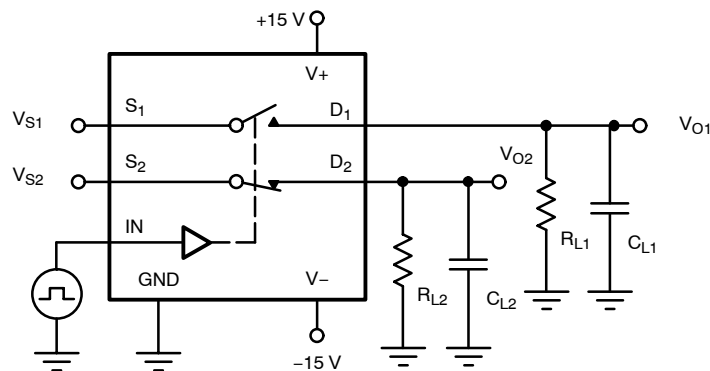
$$V_O = V_S \frac{R_L}{R_L + r_{DS(on)}}$$



*V_S = 10 V for t_{ON}, V_S = -10 V for t_{OFF}

Note: Logic input waveform is inverted for switches that have the opposite logic sense control

FIGURE 2. Switching Time



C_L (includes fixture and stray capacitance)

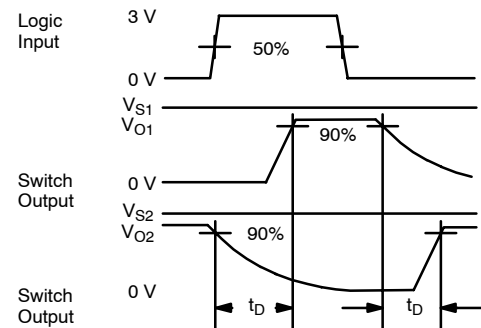


FIGURE 3. Break-Before-Make

TEST CIRCUITS

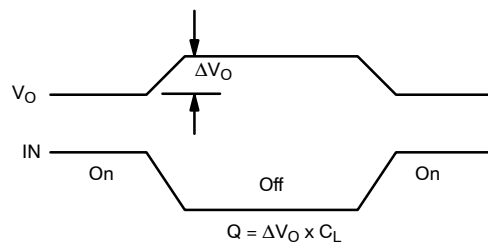
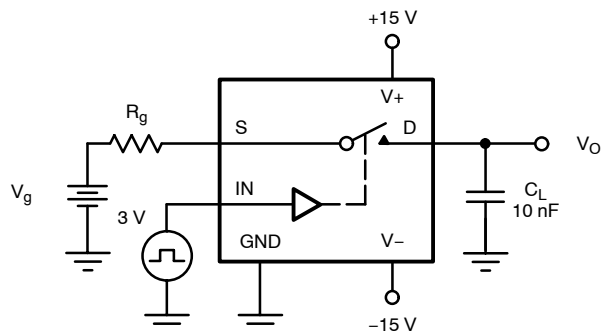


FIGURE 4. Charge Injection

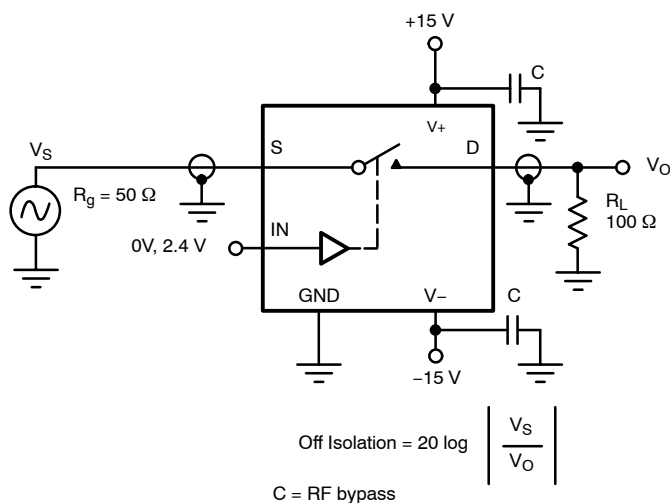


FIGURE 5. Off Isolation

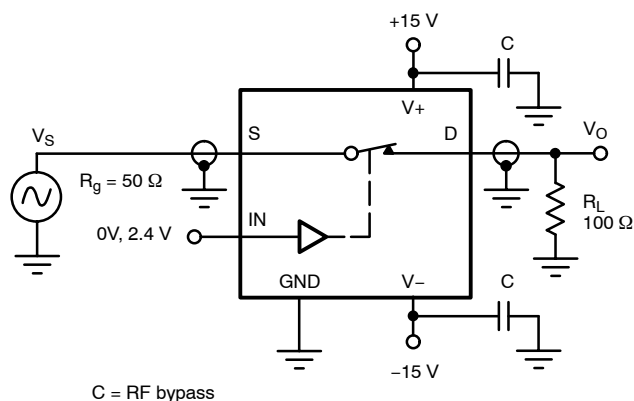


FIGURE 6. Insertion Loss

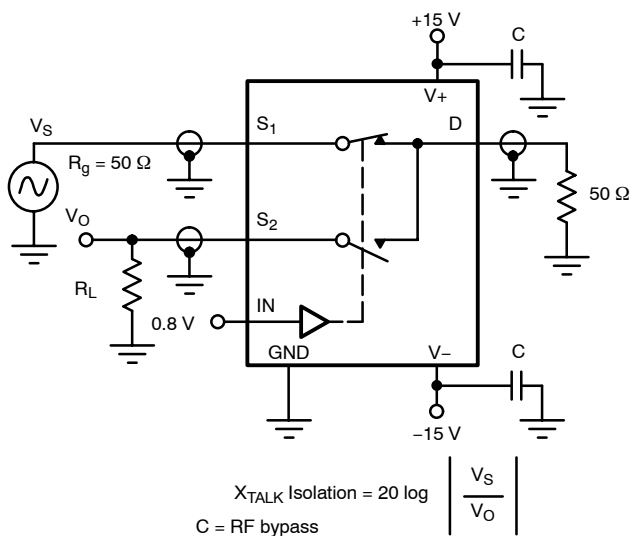


FIGURE 7. Crosstalk

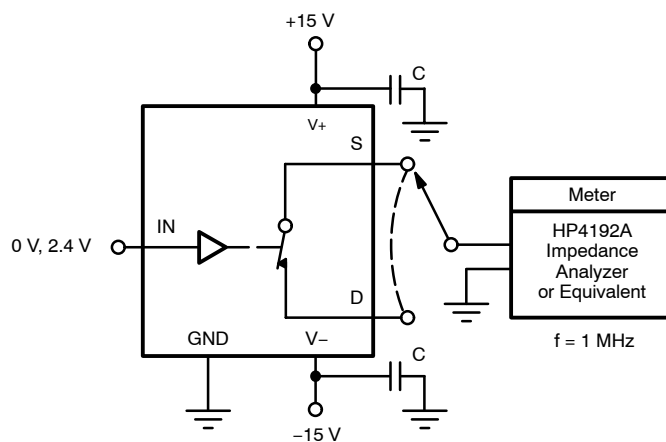


FIGURE 8. Capacitances

APPLICATIONS

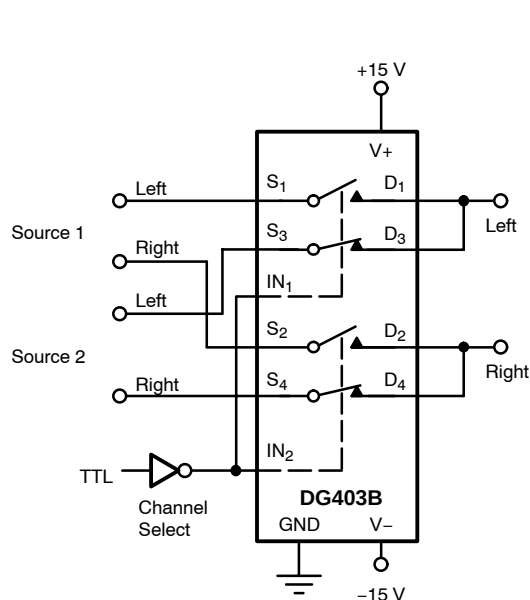


FIGURE 9. Stereo Source Selector

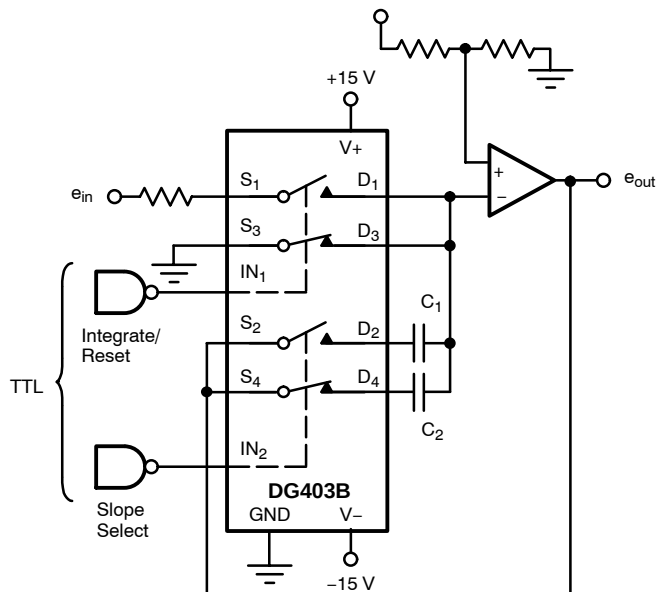


FIGURE 10. Dual Slope Integrator

Dual Slope Integrators

The DG403B is well suited to configure a selectable slope integrator. One control signal selects the timing capacitor C_1 or C_2 . Another one selects e_{in} or discharges the capacitor in preparation for the next integration cycle.

Band-Pass Switched Capacitor Filter

Single-pole double-throw switches are a common element for switched capacitor networks and filters. The fast switching times and low leakage of the DG403B allow for higher clock rates and consequently higher filter operating frequencies.

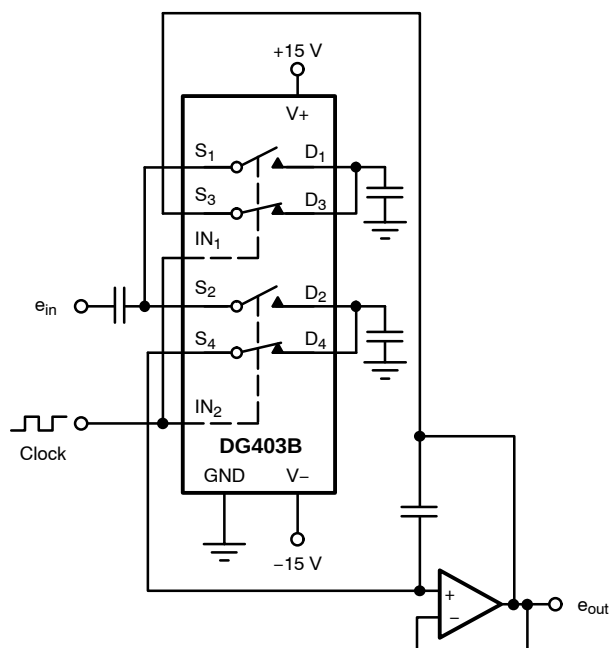


FIGURE 11. Band-Pass Switched Capacitor Filter

APPLICATIONS

Peak Detector

A_3 acting as a comparator provides the logic drive for operating SW_1 . The output of A_2 is fed back to A_3 and compared to the analog input e_{in} . If $e_{in} > e_{out}$ the output of A_3 is high keeping SW_1 closed. This allows C_1 to charge up to the

analog input voltage. When e_{in} goes below e_{out} A_3 goes negative, turning SW_1 off. The system will therefore store the most positive analog input experienced.

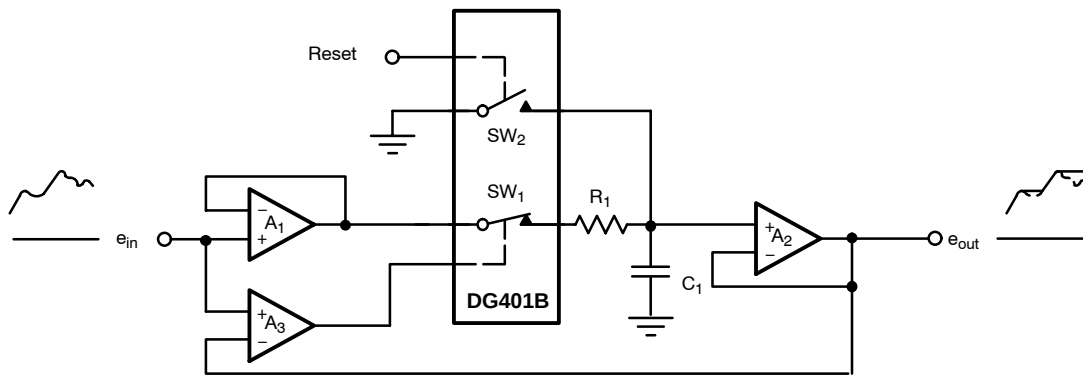


FIGURE 12. Positive Peak Detector



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