



ALPHA & OMEGA
SEMICONDUCTOR

AONR36326C

30V N-Channel MOSFET

General Description

- Trench Power MOSFET technology
- Very Low $R_{DS(ON)}$ at 4.5V V_{GS}
- Low Gate Charge
- High Current Capability
- RoHS and Halogen-Free Compliant

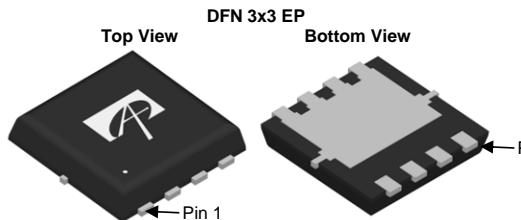
Product Summary

V_{DS}	30V
I_D (at $V_{GS}=10V$)	12A
$R_{DS(ON)}$ (at $V_{GS}=10V$)	< 9.8mΩ
$R_{DS(ON)}$ (at $V_{GS}=4.5V$)	< 15.9mΩ

Applications

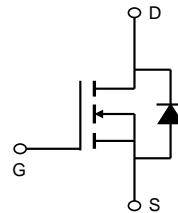
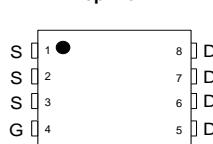
- DC/DC Converters in Computing, Servers, and POL
- Isolated DC/DC Converters in Telecom and Industrial
- See Note I

100% UIS Tested
100% R_g Tested



Top View

Bottom View



Orderable Part Number	Package Type	Form	Minimum Order Quantity
AONR36326C	DFN 3X3 EP	Tape & Reel	5000

Absolute Maximum Ratings $T_A=25^\circ C$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ^G	I_D	12	A
		12	
Pulsed Drain Current ^C	I_{DM}	48	
Continuous Drain Current ^G	I_{DSM}	12	A
		11	
Avalanche Current ^C	I_{AS}	20	A
Avalanche energy ^C	E_{AS}	10	mJ
Power Dissipation ^B	P_D	20.5	W
		8	
Power Dissipation ^A	P_{DSM}	3.1	W
		2	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	°C

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	30	40	°C/W
		60	70	°C/W
Maximum Junction-to-Case	$R_{\theta JC}$	5	6	°C/W

Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D=250\mu\text{A}, V_{GS}=0\text{V}$	30			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=30\text{V}, V_{GS}=0\text{V}$ $T_J=55^\circ\text{C}$		1	5	μA
I_{GSS}	Gate-Body leakage current	$V_{DS}=0\text{V}, V_{GS}=\pm20\text{V}$			±100	nA
$V_{GS(\text{th})}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	1.3	1.8	2.3	V
$R_{DS(\text{ON})}$	Static Drain-Source On-Resistance	$V_{GS}=10\text{V}, I_D=12\text{A}$ $T_J=125^\circ\text{C}$		8	9.8	$\text{m}\Omega$
		$V_{GS}=4.5\text{V}, I_D=10\text{A}$		11	13.5	$\text{m}\Omega$
g_{FS}	Forward Transconductance	$V_{DS}=5\text{V}, I_D=12\text{A}$		45		S
V_{SD}	Diode Forward Voltage	$I_S=1\text{A}, V_{GS}=0\text{V}$		0.73	1	V
I_S	Maximum Body-Diode Continuous Current ^G				12	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	$V_{GS}=0\text{V}, V_{DS}=15\text{V}, f=1\text{MHz}$		540		pF
C_{oss}	Output Capacitance			230		pF
C_{rss}	Reverse Transfer Capacitance			30		pF
R_g	Gate resistance	$f=1\text{MHz}$	1	2	3	Ω
SWITCHING PARAMETERS						
$Q_g(10\text{V})$	Total Gate Charge	$V_{GS}=10\text{V}, V_{DS}=15\text{V}, I_D=12\text{A}$		9	15	nC
$Q_g(4.5\text{V})$	Total Gate Charge			4.3	7	nC
Q_{gs}	Gate Source Charge			2.2		nC
Q_{gd}	Gate Drain Charge			1.7		nC
$t_{D(\text{on})}$	Turn-On DelayTime	$V_{GS}=10\text{V}, V_{DS}=15\text{V}, R_L=1.25\Omega, R_{\text{GEN}}=3\Omega$		4		ns
t_r	Turn-On Rise Time			3.5		ns
$t_{D(\text{off})}$	Turn-Off DelayTime			18		ns
t_f	Turn-Off Fall Time			3		ns
t_{rr}	Body Diode Reverse Recovery Time	$I_F=12\text{A}, \text{di}/\text{dt}=500\text{A}/\mu\text{s}$		9.7		ns
Q_{rr}	Body Diode Reverse Recovery Charge	$I_F=12\text{A}, \text{di}/\text{dt}=500\text{A}/\mu\text{s}$		11.5		nC

A. The value of R_{JJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$. The Power dissipation P_{DSM} is based on $R_{\text{JJA}} \leq 10\text{s}$ and the maximum allowed junction temperature of 150°C . The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on $T_{J(\text{MAX})}=150^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Single pulse width limited by junction temperature $T_{J(\text{MAX})}=150^\circ\text{C}$.

D. The R_{JJA} is the sum of the thermal impedance from junction to case R_{JJC} and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(\text{MAX})}=150^\circ\text{C}$. The SOA curve provides a single pulse rating.

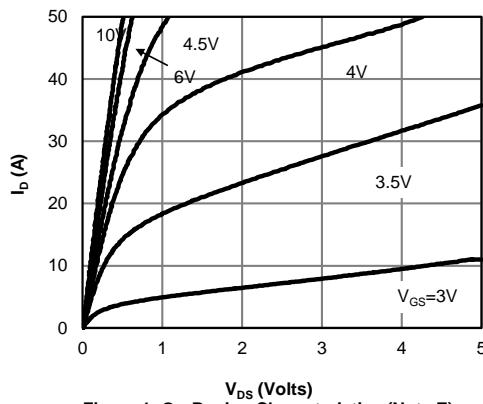
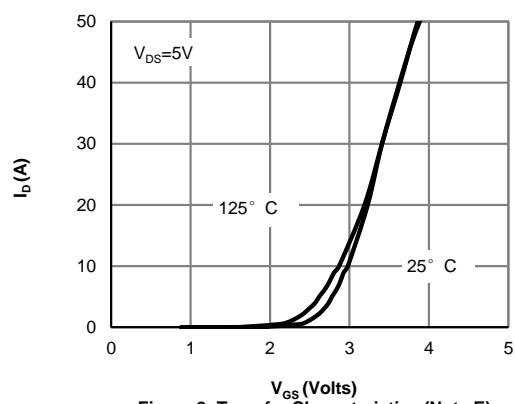
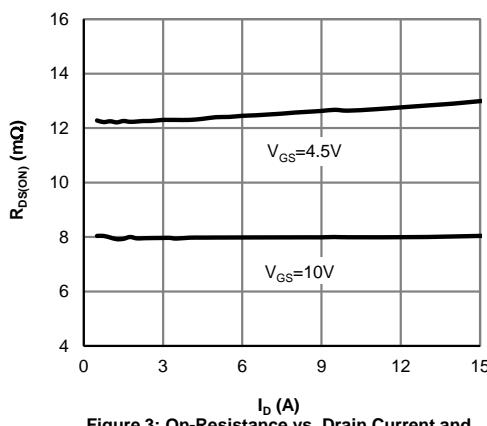
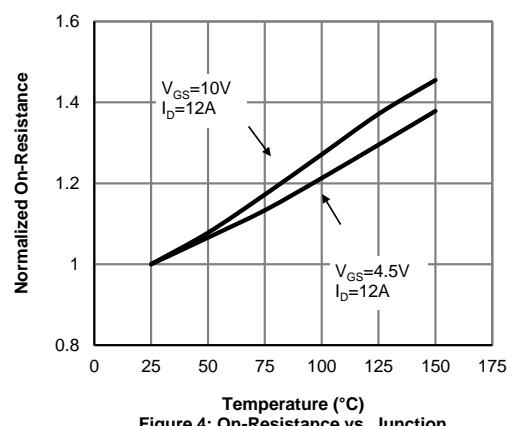
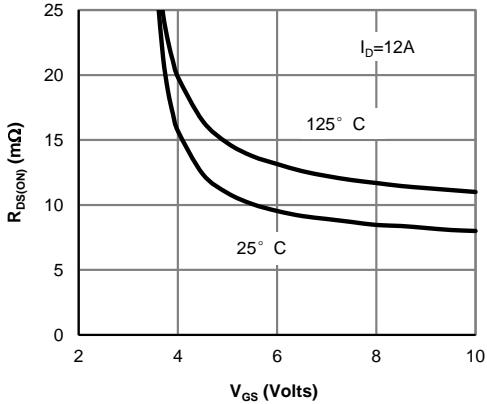
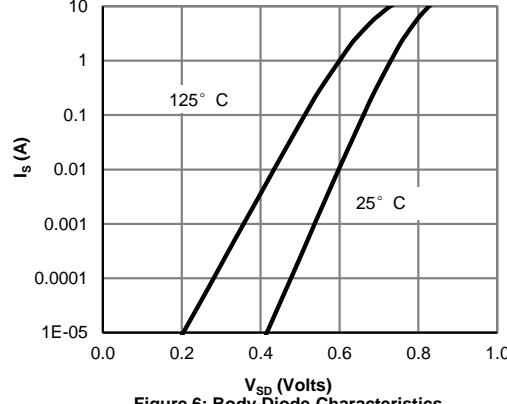
G. The maximum current rating is package limited.

H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$.

I. For application requiring slow >1ms turn-on/turn-off, please consult AOS FAE for proper product selection.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

Figure 1: On-Region Characteristics (Note E)

Figure 2: Transfer Characteristics (Note E)

Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

Figure 4: On-Resistance vs. Junction Temperature (Note E)

Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

Figure 6: Body-Diode Characteristics (Note E)

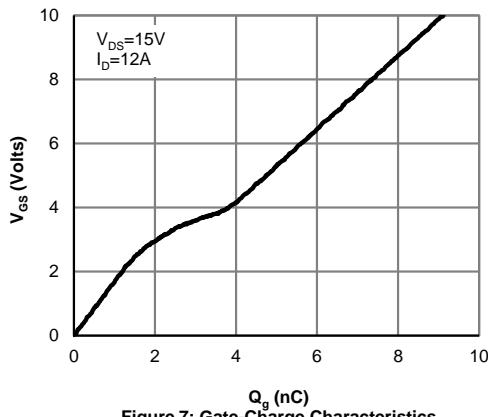
TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS


Figure 7: Gate-Charge Characteristics

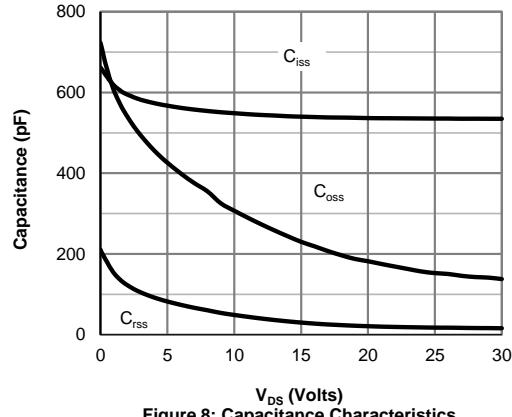


Figure 8: Capacitance Characteristics

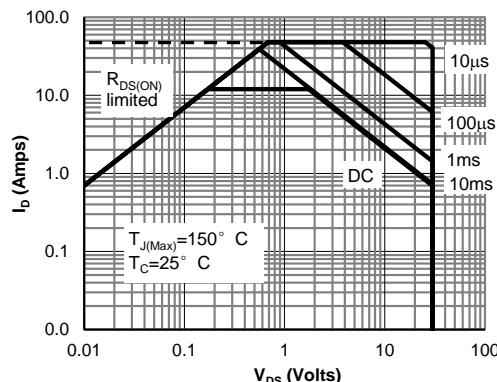


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

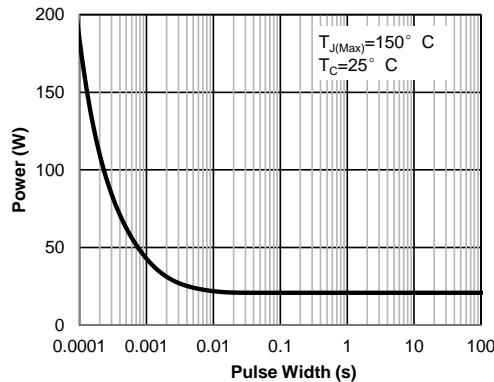


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

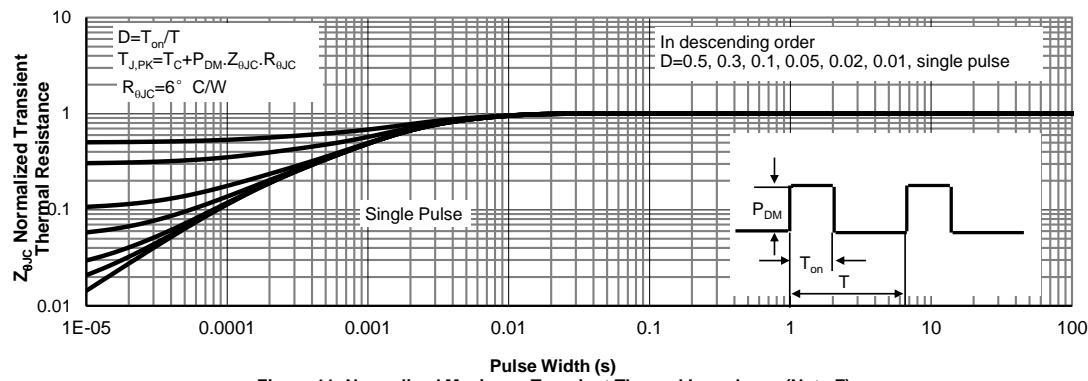


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

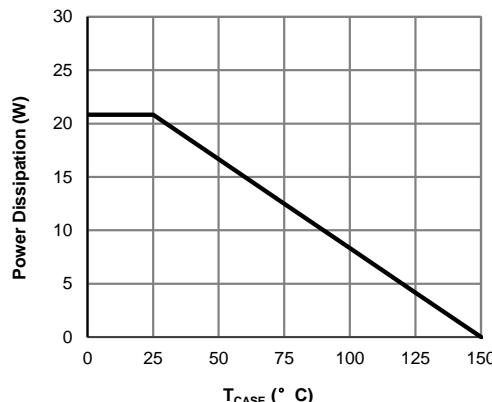
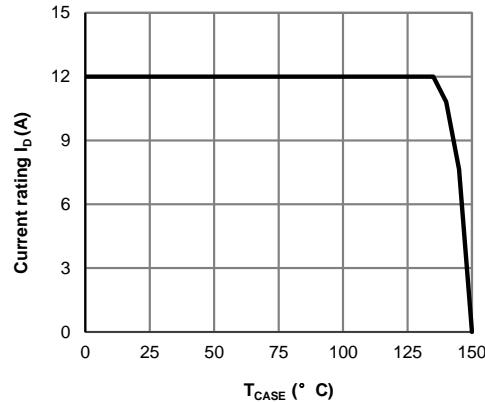
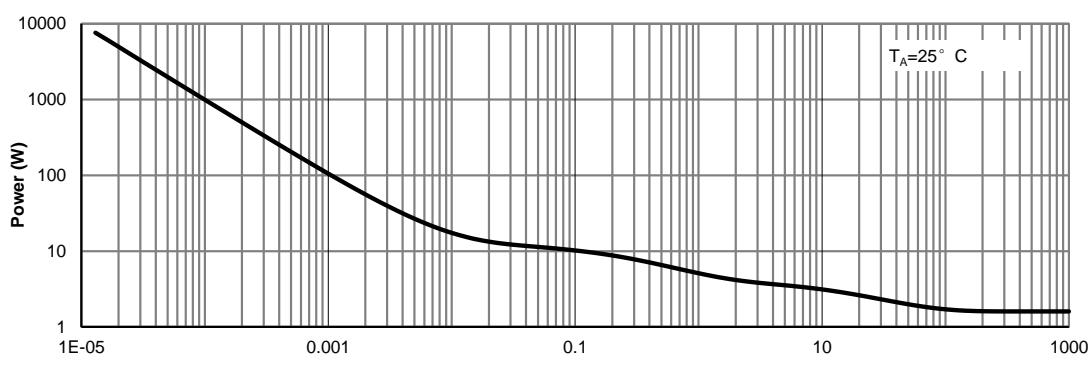
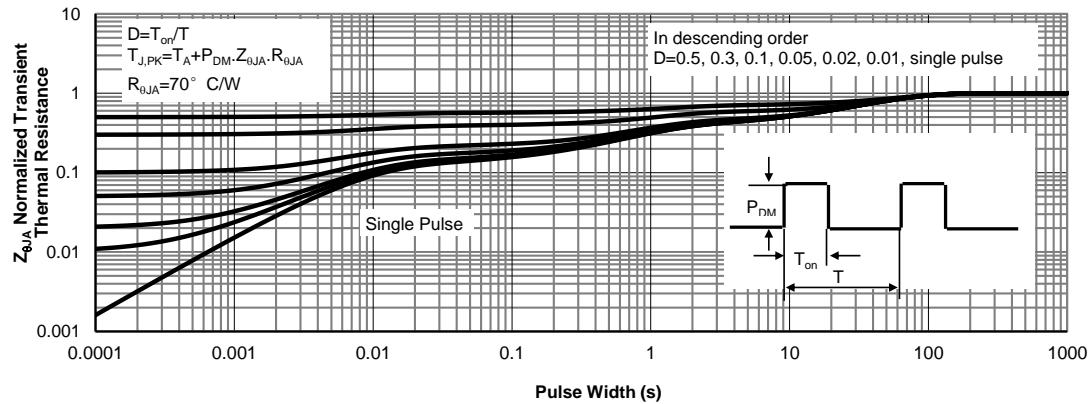
TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

Figure 12: Power De-rating (Note F)

Figure 13: Current De-rating (Note F)

Figure 14: Single Pulse Power Rating Junction-to-Ambient (Note H)

Figure 15: Normalized Maximum Transient Thermal Impedance (Note H)

Figure A: Gate Charge Test Circuit & Waveforms

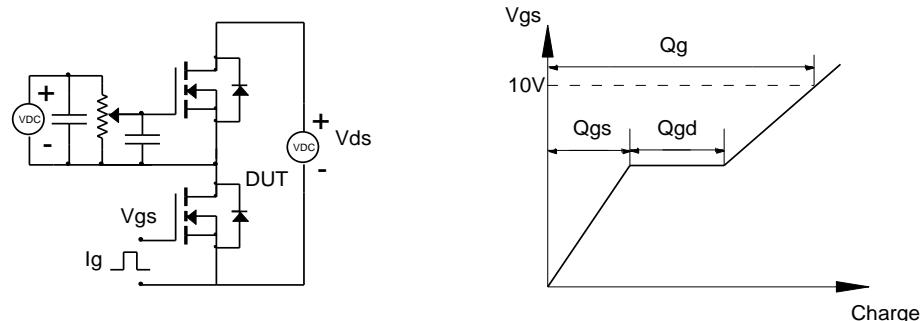


Figure B: Resistive Switching Test Circuit & Waveforms

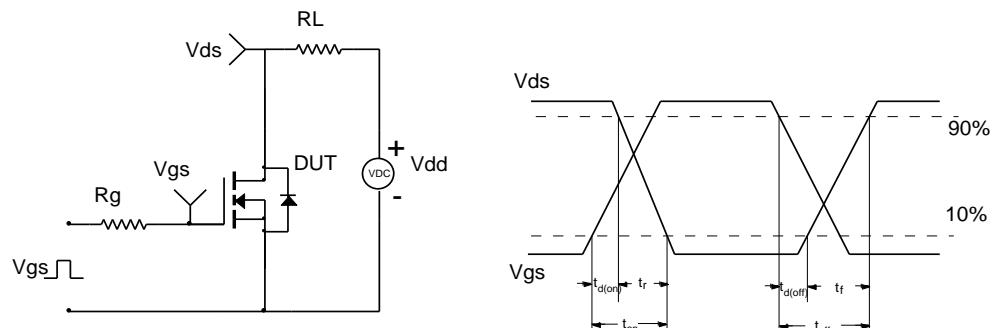


Figure C: Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

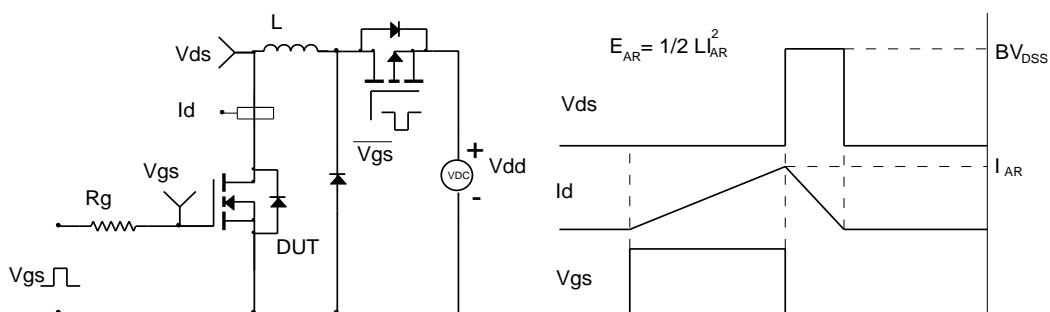


Figure D: Diode Recovery Test Circuit & Waveforms

