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STGAP2SICSA

Datasheet

Galvanically isolated 4 A single gate driver for SiC MOSFETs

SO-8W

Product status link
STGAP2SICSA

Product label
SUSTAINABLE TECHNOLOGY

Features

- AEC-Q100 qualified
- High voltage rail up to 1200 V
- Driver current capability: 4 A sink/source @25°C
- 100 V/ns Common Mode Transient Immunity (CMTI)
- Overall input-output propagation delay: 45 ns
- Rail-to-rail outputs
- 4 A Miller CLAMP dedicated pin
- UVLO function
- Gate driving voltage up to 26 V
- 3.3 V, 5 V TTL/CMOS inputs with hysteresis
- Temperature shut-down protection
- Standby function
- 6 kV galvanic isolation
- Wide body SO-8W package
- UL 1577 recognized

Application

- Motor driver for home appliances, factory automation, industrial drives and fans
- 600/1200 V inverters
- Battery chargers
- Induction heating
- Welding
- UPS
- Power supply units
- DC-DC converters
- Power Factor Correction

Description

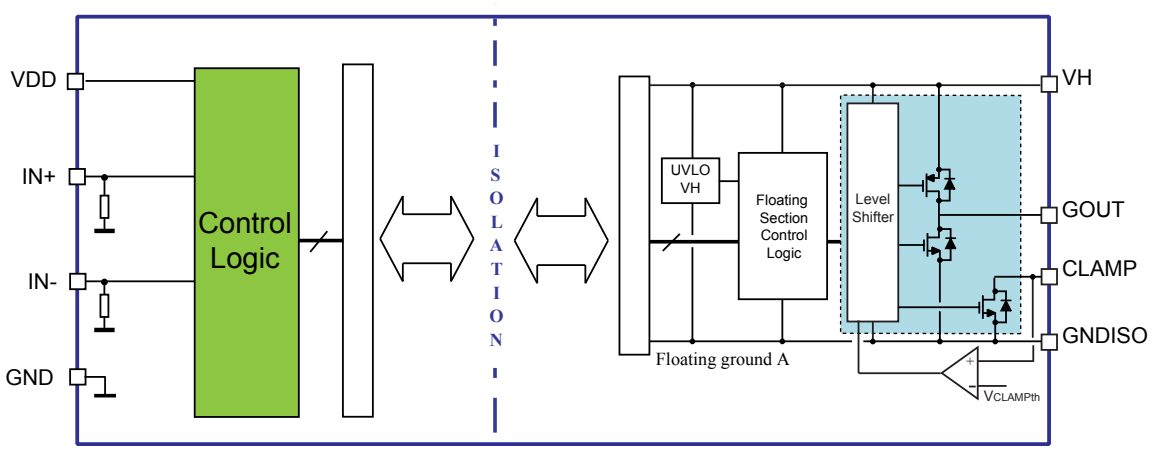
The STGAP2SICSA is a single gate driver which provides galvanic isolation between the gate driving channel and the low voltage control and interface circuitry.

The gate driver is characterized by 4 A capability and rail-to-rail outputs, making the device also suitable for mid and high power applications such as power conversion and motor driver inverters in industrial applications. The device has a single output pin and Miller CLAMP function that prevents gate spikes during fast commutations in half-bridge topologies. This configuration provides high flexibility and bill of material reduction for external components.

The device integrates protection functions: UVLO with optimized value for SiC MOSFETs and thermal shut down are included to facilitate the design of highly reliable systems. Dual input pins allow the selection of signal polarity control and implementation of HW interlocking protection to avoid cross-conduction in case of controller malfunction. The input to output propagation delay is less than 45 ns, which delivers high PWM control accuracy. A standby mode is available to reduce idle power consumption.

1 Block diagram

Figure 1. **Block diagram**



2 Pin description and connection diagram

Figure 2. **Pin connection (top view)**

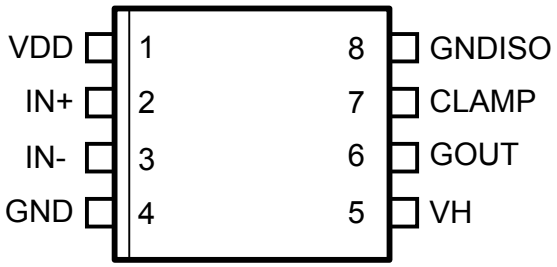


Table 1. **Pin Description**

Pin #	Pin Name	Type	Function
1	VDD	Power Supply	Driver logic supply voltage.
2	IN+	Logic Input	Driver logic input, active high.
3	IN-	Logic Input	Driver logic input, active low.
4	GND	Power Supply	Driver logic ground.
5	VH	Power Supply	Gate driving positive voltage supply.
6	GOUT	Analog Output	Sink/Source output.
7	CLAMP	Analog Output	Active Miller Clamp.
8	GNDISO	Power Supply	Gate driving Isolated ground.

3 Electrical data

3.1 Absolute maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Test condition	Min.	Max.	Unit
VDD	Logic supply voltage vs. GND	-	-0.3	6	V
V_{LOGIC}	Logic pins voltage vs. GND	-	-0.3	6	V
VH	Positive supply voltage (VH vs. GNDISO)	-	-0.3	28	V
V_{OUT}	Voltage on gate driver outputs (GON, GOFF, CLAMP VS. GNDISO)	-	-0.3	VH+0.3	V
T_J	Junction temperature	-	-40	150	°C
T_{STG}	Storage temperature	-	-50	150	°C
ESD	HBM (human body model)	-	2		kV

3.2 Recommended operating conditions

Table 3. Recommended operating conditions

Symbol	Parameter	Test conditions	Min.	Max.	Unit
VDD	Logic supply voltage vs. GND	-	3.1	5.25	V
V_{LOGIC}	Logic pins voltage vs. GND	-	0	5.5	V
VH	Positive supply voltage (VH vs. GNDISO)	-	Max(VH_{ON})	26	V
F_{SW}	Maximum switching frequency(1)	-	-	1	MHz
t_{OUT}	Output pulse width (GOUT, GON-GOFF)	-	100	-	ns
T_J	Operating Junction Temperature	-	-40	125	°C

1. *Actual limit depends on power dissipation and T_J.*

3.3 Thermal data

Table 4. Thermal data

Symbol	Parameter	Package	Value	Unit
$R_{th(JA)}$	Thermal resistance junction to ambient	SO-8W	130	°C/W

4 Electrical characteristics

Test Conditions: T_J = -40 to 125 °C, VH = 18 V, VDD = 5 V unless otherwise specified)

Table 5. Electrical characteristics

Symbol	Pin	Parameter	Test conditions		Min	Typ	Max	Unit
Dynamic characteristics								
t_{Don}	IN+, IN-	Input to output propagation delay ON	VDD = 5 V	T_J=25°C		45		ns
				-40°C ≤ T_J ≤ +125°C	30	-	80	
			VDD = 3.3 V	T_J=25°C		60		
				-40°C ≤ T_J ≤ +125°C	40	-	95	
t_{Doff}	IN+, IN-	Input to output propagation delay OFF	VDD = 5 V	T_J=25°C		45		ns
				-40°C ≤ T_J ≤ +125°C	30	-	80	
			VDD = 3.3 V	T_J=25°C		60		
				-40°C ≤ T_J ≤ +125°C	40	-	95	
PWD		Pulse Width Distortion $\lvert t_{Don} - t_{Doff} \rvert$					20	ns
t_r		Rise time	T_J=25°C		-	30	-	ns
t_f		Fall time	C_L= 4.7 nF See Figure 9		-	30	-	ns
CMTI [1]		Common-mode transient immunity, $\lvert dV_{ISO}/dt \rvert$	V_{CM} = 1500 V, See Figure 10		100			V/ns
Supply voltage								
VH_{on}	VH	VH UVLO turn on threshold			14.5	15.6	16.4	V
VH_{off}	VH	VH UVLO turn off threshold			13.8	14.8	15.7	V
VH_{hyst}	VH	VH UVLO hysteresis			0.50	0.75	0.95	V
I_{QHU}	VH	VH under-voltage quiescent supply current	VH = 13 V			1.3	1.9	mA
I_{QH}	VH	VH quiescent supply current				1.3	1.9	mA
I_{QHSBY}	VH	Stand-by VH quiescent supply current	Standby mode			400	700	µA
SafeClp	GOUT / GOFF	GOFF active clamp	I_{GOFF} = 0.2 A VH floating	T_J=25°C		1.9	2.2	V
				-40°C ≤ T_J ≤ +125°C			3.4	
I_{QDD}	VDD	VDD quiescent supply current				1	1.3	mA
I_{QDDSBY}	VDD	Stand-by VDD quiescent supply current	Standby mode			40	65	µA

Symbol	Pin	Parameter	Test conditions	Min	Typ	Max	Unit
Logic Inputs							
V_{il}	IN+, IN-	Low level logic threshold voltage		0.29·VDD	1/3·VDD	0.39 ·VDD	V
V_{ih}	IN+, IN-	High level logic threshold voltage		0.58 ·VDD	2/3·VDD	0.7·VDD	V
I_{INh}	IN+, IN-	INx logic “1” input bias current	INx = 5 V	28	50	70	µA
I_{INl}	IN+, IN-	INx logic “0” input bias current	INx = GND			1	µA
R_{pd}	IN+, IN-	Inputs pull-down resistors	INx = 5 V	60	100	160	kW
Driver buffer section							
I_{GON}	GOUT / GON	Source short circuit current	T_J = 25°C (1)		4.4		A
			-40 °C ≤ T_J ≤ 125 °C	3		5.5	
V_{GONH}	GOUT / GON	Source output high level voltage	I_{GON} = 100 mA		VH-0.11	VH-0.21	V
R_{GON}	GOUT / GON	Source R_{DS_ON}	I_{GON} = 100 mA		1.12	2.11	Ω
I_{GOFF}	GOUT / GOFF	Sink short circuit current	T_J = 25°C (1)		4		A
			-40 °C ≤ T_J ≤ 125 °C	2.4		5.5	
V_{GOFFL}	GOUT / GOFF	Sink output low level voltage	I_{GOFF} = 100 mA		90	180	mV
R_{GOFF}	GOUT / GOFF	Sink R_{DS_ON}	I_{GOFF} = 100 mA		0.90	1.80	Ω
Clamp Miller function							
$V_{CLAMPth}$	CLAMP	CLAMP voltage threshold	V_{CLAMP} vs. GNDISO	1.3	2	2.6	V
I_{CLAMP}	CLAMP	CLAMP short circuit current	V_{CLAMP} = 18 V T_J = 25°C (1)		4		A
			-40 °C ≤ T_J ≤ 125 °C	2.4		5.5	
V_{CLAMP_L}	CLAMP	CLAMP low level output voltage	I_{CLAMP} = 100 mA		96	220	mV
R_{CLAMP}	CLAMP	CLAMP R_{DS_ON}	I_{CLAMP} = 100 mA		0.96	2.20	Ω
Over-temperature protection							
T_{SD}		Shut down temperature (1)		170			°C
T_{hys}		Temperature hysteresis (1)			20		°C
Stand-by							
t_{STBY}		Stand-by time	See Section 6.7	200	280	500	µs
t_{WUP}		Wake-up time	See Section 6.7	10	20	35	µs
t_{awake}		Wake-up delay	See Section 6.7	90	130	200	µs
$t_{stbyfilt}$		Stand-by filter	See Section 6.7	200	280	800	ns

1. *Characterization data, not tested in production*

5 Isolation

Table 6. Isolation and safety-related specifications

Parameter	Symbol	Value	Unit	Conditions
Clearance (Minimum External Air Gap)	CLR	8	mm	Measured from input terminals to output terminals, shortest distance through air
Creepage (*) (Minimum External Tracking)	CPG	8	mm	Measured from input terminals to output terminals, shortest distance path along body
Comparative Tracking Index (Tracking Resistance)	CTI	≥ 400	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group	-	II	-	Material Group (DIN VDE 0110, 1/89, Table 1)

Table 7. Isolation characteristics

Parameter	Symbol	Test Conditions	Characteristic	Unit
Maximum Working Isolation Voltage	V_{IORM}	-	1200	V_{PEAK}
Input to Output test voltage In accordance with VDE 0884-11	V_{PR}	Method a, Type test	1920	V_{PEAK}
		$V_{PR} = V_{IORM} \times 1.6$, t_m = 10 s		
		Partial discharge < 5 pC		
		Method b1, 100 % Production test	2250	V_{PEAK}
		$V_{PR} = V_{IORM} \times 1.875$, t_m = 1 s		
		Partial discharge < 5 pC		
Transient Overvoltage (Highest Allowable Overvoltage)	V_{IOTM}	t_{ini} = 60 s Type test	6000	V_{PEAK}
Maximum Surge TestVoltage	V_{IOSM}	Type test	6000	V_{PEAK}
Isolation Resistance	R_{IO}	V_{IO} = 500 V; Type test	$>10^9$	Ω

Table 8. Isolation voltage as per UL 1577

Parameter	Symbol	Characteristic	Unit
Isolation Withstand Voltage, 1min (Type test)	V_{ISO}	3535/5000	V_{RMS}/V_{PEAK}
Isolation TestVoltage, 1sec (100% production)	$V_{ISOtest}$	4242/6000	V_{RMS}/V_{PEAK}

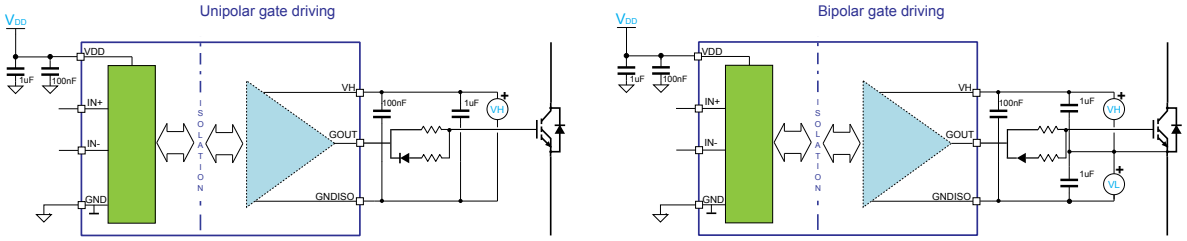
Recognized under the UL 1577 Component Recognition Program - file number E362869

6 Functional description

6.1 Gate driving power supply and UVLO

The STGAP2SiCSA is a flexible and compact gate driver with 4 A output current and rail-to-rail outputs. The device allows implementation of either unipolar or bipolar gate driving.

Figure 3. Power supply configuration for unipolar and bipolar gate driving



Undervoltage protection is available on VH supply pin. A fixed hysteresis sets the turn-off threshold, thus avoiding intermittent operation.

When VH voltage falls below the VHoff threshold, the output buffer enters a “safe state”. When VH voltage reaches the VHon threshold, the device returns to normal operation and sets the output according to actual input pins status.

The VDD and VH supply pins must be properly filtered with local bypass capacitors. The use of capacitors with different values in parallel provides both local storage for impulsive current supply and high-frequency filtering. The best filtering is obtained by using low-ESR SMT ceramic capacitors and are therefore recommended. A 100 nF ceramic capacitor must be placed as close as possible to each supply pin, and a second bypass capacitor with value in the range between 1 µF and 10 µF should be placed close to it.

6.2 Power-up, power-down and “safe state”

The following conditions define the “safe state”:

- GOUT = OFF state;
- CLAMP = ON state;

Such conditions are maintained at power-up of the isolated side (VH < VH_{on}) and during whole device power down phase (VH < VH_{off}), regardless of the value of the input pins.

The device integrates a structure which clamps the driver output to a voltage not higher than SafeClp when VH voltage is not high enough to actively turn the internal GOFF MOSFET on. If VH positive supply pin is floating or not supplied the GOFF pin is therefore clamped to a voltage smaller than SafeClp.

If the supply voltage VDD of the control section of the device is not supplied, the output is put in safe state, and remains in such condition until the VDD voltage returns within operative conditions.

After power-up of both isolated and low voltage sides, the device output state depends on the status of the input pins.

6.3 Control inputs

The device is controlled through the IN+ and IN- logic inputs, in accordance with the truth table below.

Table 9. Inputs truth table (applicable when device is not in UVLO or "safe state")

Input pins		Output pin
IN+	IN-	GOUT
L	L	LOW
H	L	**HIGH**
L	H	LOW
H	H	LOW

A deglitch filter allows input signals with duration shorter than tdeglitch to be ignored, thereby preventing noise spikes potentially present in the application from generating unwanted commutations.

6.4 Miller Clamp function

The Miller clamp function allows the control of the Miller current during the power stage switching in half-bridge configurations. When the external power transistor is in the OFF state, the driver operates to avoid the induced turn-on phenomenon that may occur when the other switch in the same leg is being turned on, due to the C_{GD} capacitance.

During the turn-off period the gate of the external switch is monitored through the CLAMP pin. The CLAMP switch is activated when gate voltage goes below the voltage threshold, $V_{CLAMPth}$, thus creating a low impedance path between the switch gate and the GNDISO pin.

6.5 Watchdog

The isolated HV side has a watchdog function in order to identify when it is not able to communicate with LV side, for example because the VDD of the LV side is not supplied. In this case the output of the driver is forced in “safe state” until communication link is properly established again.

6.6 Thermal shutdown protection

The device provides a thermal shutdown protection. When junction temperature reaches the T_{SD} temperature threshold, the device is forced in “safe state”. The device operation is restored as soon as the junction temperature is lower than 'T_{SD} - T_{hys}'.

6.7 Standby function

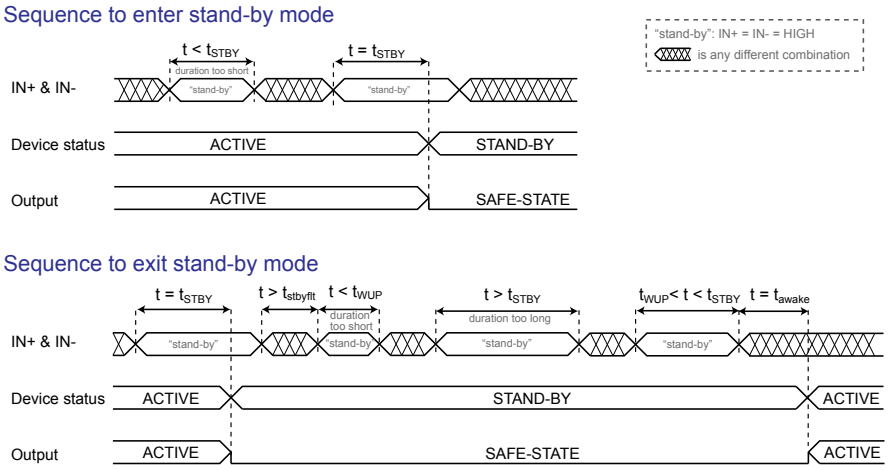
In order to reduce the power consumption of both control interface and gate driving sides the device can be put in standby mode. In standby mode the quiescent current from VDD and VH supply pins is reduced to I_{QDDSBY} and I_{QHSBY} respectively, and the output remains in “safe state” (the output is actively forced low).

The way to enter standby is to keep both IN+ and IN- high (“standby” value) for a time longer than t_{STBY}. During stand-by the inputs can change from the “standby” value.

To exit stand-by, IN+ and IN- must be put in any combination different from the “standby” value for a time longer than $t_{stbyfilt}$, and then in the “standby” value for a time t such that $t_{WUP} < t < t_{STBY}$.

When the input configuration is changed from the “standby” value the output is enabled and set according to inputs state after a time t_{awake}.

Figure 4. Standby state sequences



7 Typical application diagram

Figure 5. **Typical application diagram - Miller Clamp**

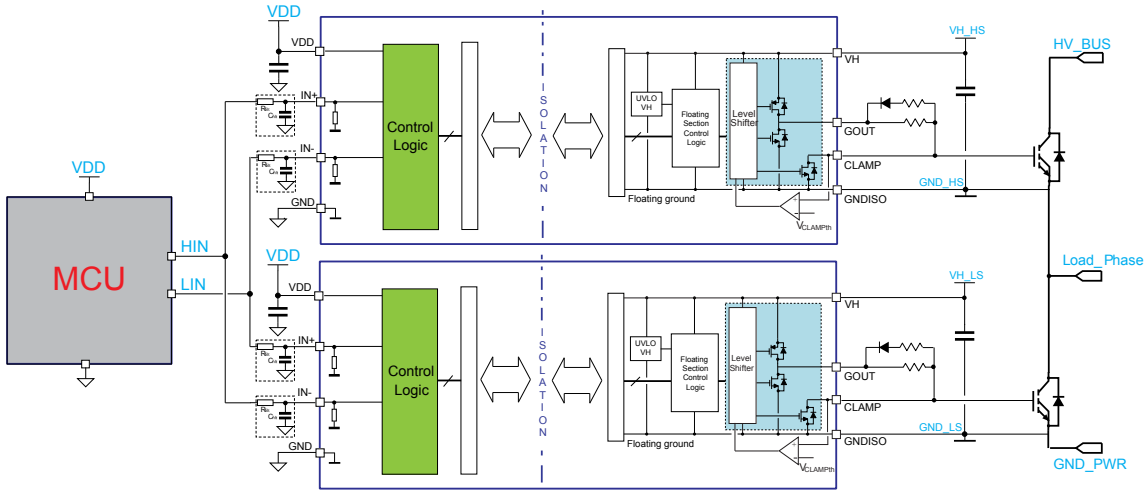
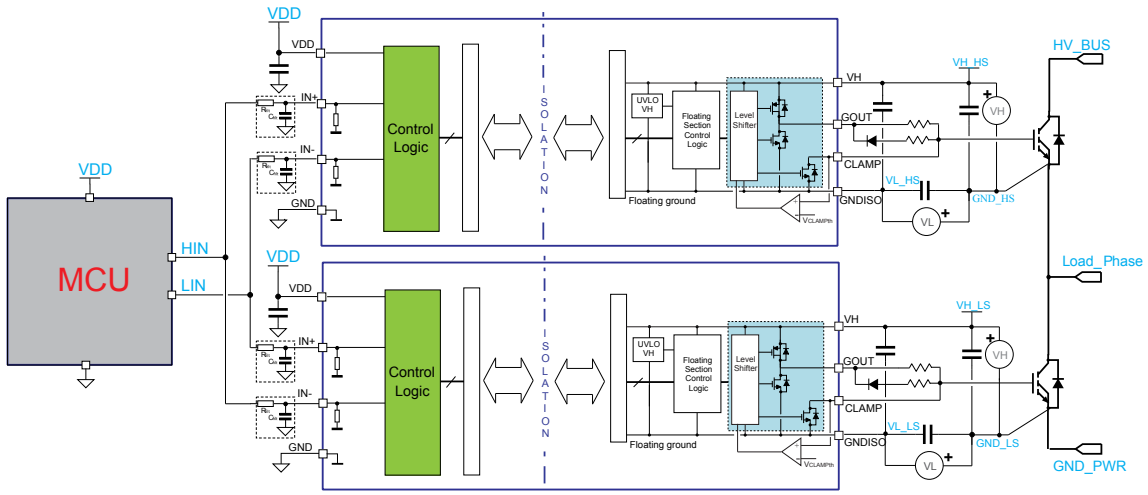


Figure 6. **Typical application diagram - Miller Clamp and negative gate driving**



8 Layout

8.1 Layout guidelines and considerations

In order to optimize the PCB layout, the following considerations should be taken into account:

- SMT ceramic capacitors (or different types of low-ESR and low-ESL capacitors) must be placed close to each supply rail pins. A 100 nF capacitor must be placed between VDD and GND and between VH and GNDISO, as close as possible to device pins, in order to filter high-frequency noise and spikes. In order to provide local storage for pulsed current, a second capacitor with a value between 1 µF and 10 µF should also be placed close to the supply pins.
- It is good practice to add filtering capacitors close to logic inputs of the device (IN+, IN-), particularly for fast switching or noisy applications.
- The power transistors must be placed as close as possible to the gate driver to minimize the gate loop area and inductance that might carry noise or cause ringing.
- To avoid degradation of the isolation between the primary and secondary side of the driver, there should not be any trace or conductive area below the driver.
- If the system has multiple layers, it is recommended to connect the VH and GNDISO pins to internal ground or power planes through multiple vias of adequate size. These vias should be located close to the IC pins to maximize thermal conductivity.

8.2 Layout example

An example of STGAP2SICSA suggested PCB layout with main signals highlighted by different colors is shown in Figure 7 (see Figure 8 for reference schematic). It is recommended to follow this example for correct positioning and connection of filtering capacitors.

Figure 7. STGAP2SICSA suggested PCB layout: top and bottom

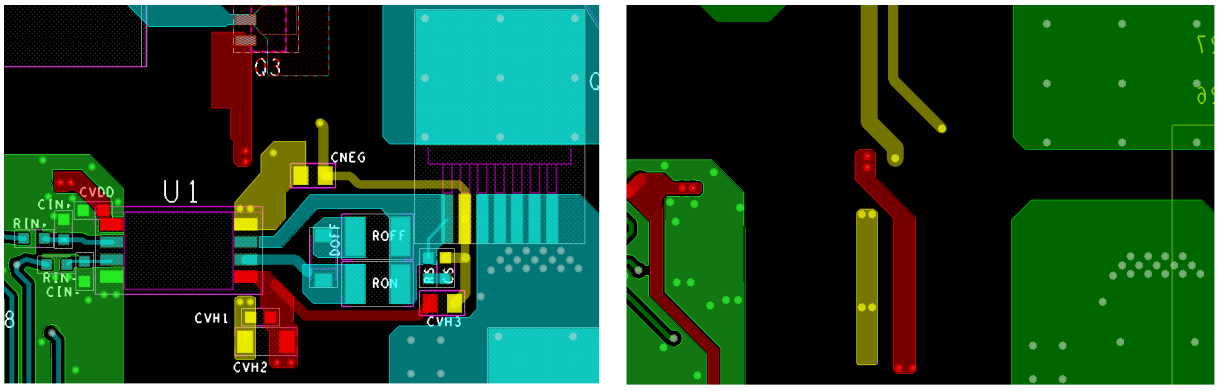
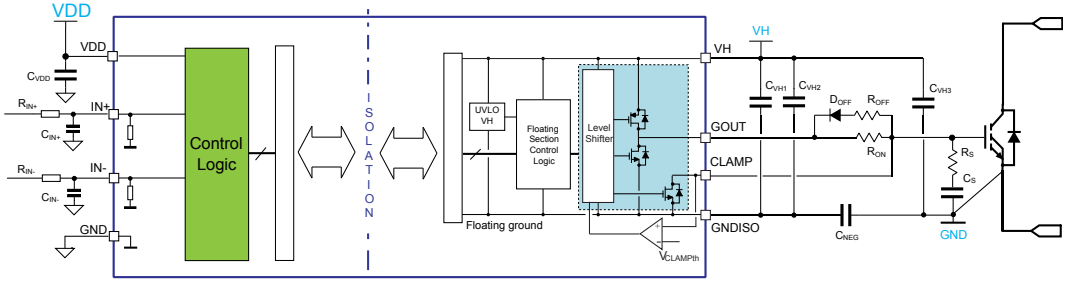


Figure 8. STGAP2SICSA reference schematic for suggested PCB layout



9 Testing and characterization information

Figure 9. **Timings definition**

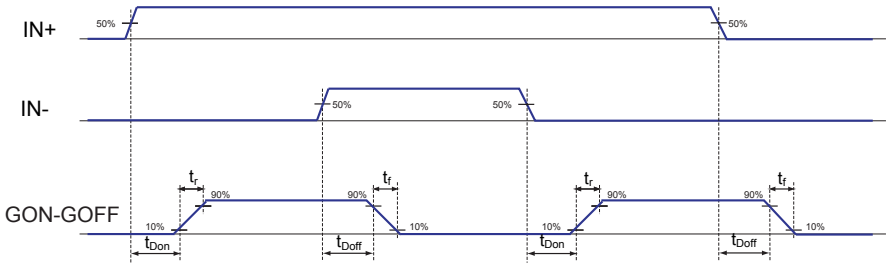
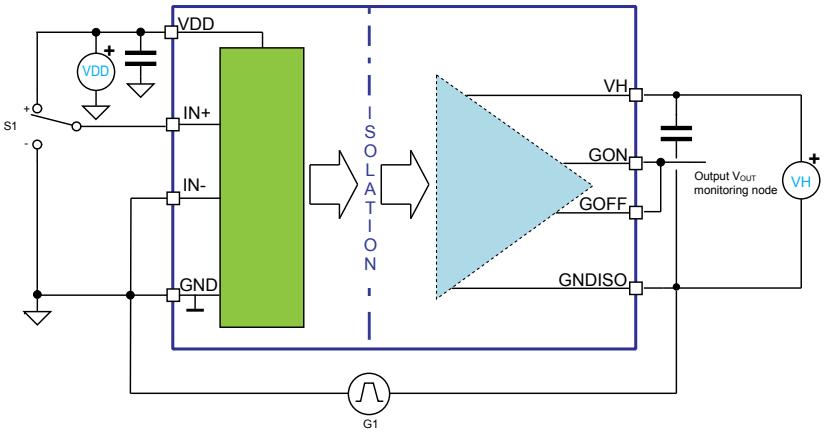


Figure 10. **CMTI test circuit**



10 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

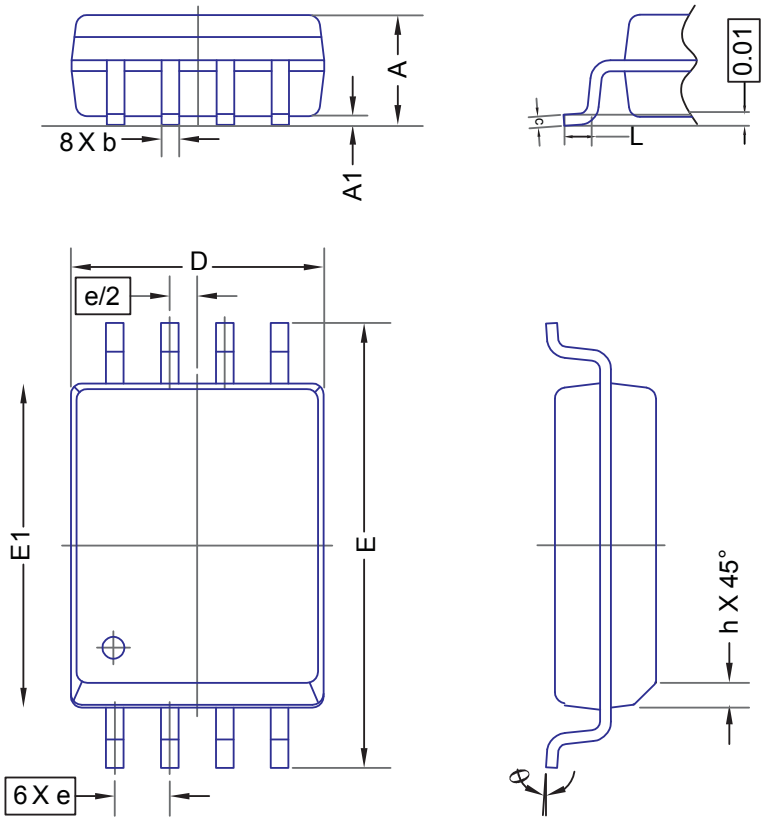
10.1 SO-8W package information

Table 10. SO-8W package dimensions

Symbol	Dimensions (mm)		
	Min.	Typ.	Max
A	2.34		2.64
A1	0.1		0.3
b	0.3		0.51
c	0.2		0.33
D(1)	5.64		6.05
e		1.27 BSC	
E1	7.39		7.59
E	10.11		10.52
L	0.61		0.91
h	0.25		0.76
Θ	0°		8°
aaa		0.25	
bbb		0.25	
ccc		0.1	

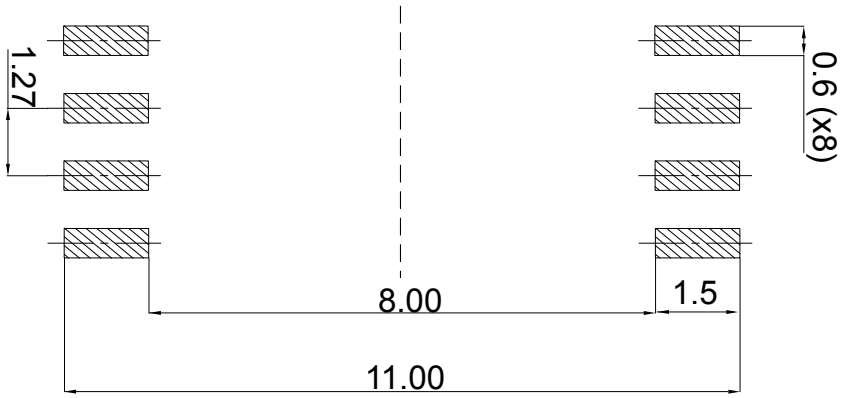
1. *Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm per side.*

Figure 11. **SO-8W mechanical data**



10.2 SO-8W suggested land pattern

Figure 12. **SO-8W suggested land pattern**



11 Ordering information

Table 11. **Device summary**

Order code	Output configuration	Package	Package marking	Packaging
STGAP2SICSAC	GOUT-CLAMP	SO-8W	GP2ISAC	Tube
STGAP2SICSACTR	GOUT-CLAMP	SO-8W	GP2ISAC	Tape and Reel

Revision history

Table 12. **Document revision history**

Date	Version	Changes
12-Apr-2023	1	Initial release.

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