

54ACT11240

Octal Buffers/Line Drivers with 3-State Outputs

These octal buffers or line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. These devices provide inverting outputs and symmetrical $\bar{G}$ (active-low output control) inputs. These devices feature high fan-out and improved fan-in.

The 54ACT11240 is characterized for operation over the full military temperature range of -55°C to 125°C. The 74ACT11240 is characterized for operation from -40°C to 85°C.

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All re-creations are done with the approval of the Original Component Manufacturer (OCM).

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-35835
 - Class Q Military
 - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
 - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OCM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

FOR REFERENCE ONLY

54ACT11240, 74ACT11240 OCTAL BUFFERS/LINE DRIVERS WITH 3-STATE OUTPUTS

SCAS210 – D3410, MAY 1987 – REVISED APRIL 1993

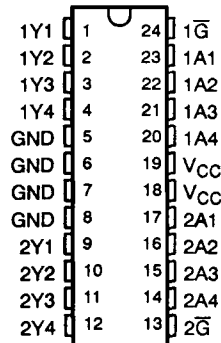
- Inputs Are TTL-Voltage Compatible
- Flow-Through Architecture Optimizes PCB Layout
- Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1- μ m Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic Small-Outline Packages, Plastic Shrink Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

description

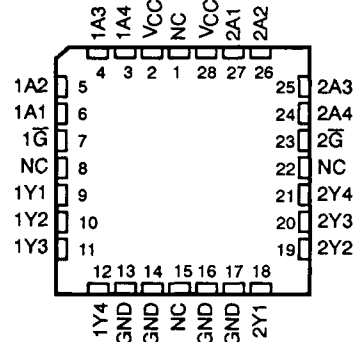
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54ACT11240... JT PACKAGE
74ACT11240... DB, DW OR NT PACKAGE
(TOP VIEW)



54ACT11240... FK PACKAGE
(TOP VIEW)



NC – No internal connection

FUNCTION TABLE
(each buffer)

INPUTS		OUTPUT
$\overline{G}$	A	Y
L	H	L
L	L	H
H	X	Z

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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TEXAS
INSTRUMENTS

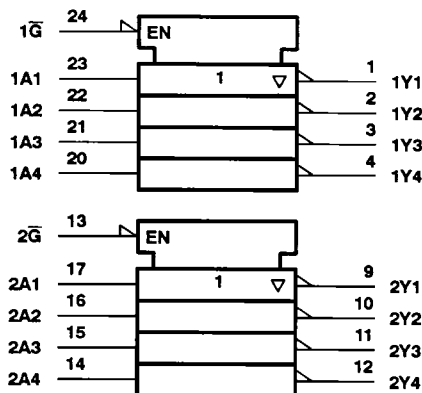
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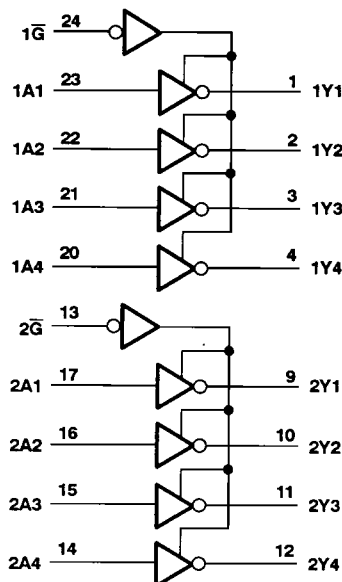
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for the DW, JT, and NT packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	–0.5 V to 6 V
Input voltage range, V_I (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 50 mA
Continuous current through V_{CC} or GND	± 200 mA
Storage temperature range	–65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			54ACT11240		74ACT11240		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = – 50 µA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I _{OH} = – 24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I _{OH} = – 50 mA†	5.5 V				3.85				
	I _{OH} = – 75 mA†	5.5 V						3.85		
V _{OL}	I _{OL} = 50 µA	4.5 V			0.1	0.1		0.1		V
		5.5 V			0.1	0.1		0.1		
	I _{OL} = 24 mA	4.5 V			0.36	0.5		0.44		
		5.5 V			0.36	0.5		0.44		
	I _{OL} = 50 mA†	5.5 V				1.65				
	I _{OL} = 75 mA†	5.5 V						1.65		
I _{OZ}	V _O = V _{CC} or GND	5.5 V			± 0.5	± 10		± 5		µA
I _I	V _I = V _{CC} or GND	5.5 V			± 0.1	± 1		± 1		µA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			8	160		80		µA
ΔI _{CC} ‡	One input at 3.4 V, Other inputs at GND or V _{CC}	5.5 V			0.9	1		1		mA
C _i	V _I = V _{CC} or GND	5 V		4						pF
C _o	V _I = V _{CC} or GND	5 V		10						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

**switching characteristics over recommended operating free-air temperature range,
V_{CC} = 5 V ± 0.5 V (unless otherwise noted)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T _A = 25°C			54ACT11240		74ACT11240		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A	Y	1.5	6.5	9.9	1.5	11.1	1.5	10.6	ns
t _{PHL}			1.5	6	8	1.5	9.2	1.5	8.7	
t _{PZH}	G	Y	1.5	7.5	11.7	1.5	13.1	1.5	12.5	ns
t _{PZL}			1.5	7.3	11.5	1.5	12.8	1.5	12.3	
t _{PHZ}	G	Y	1.5	7.3	9.4	1.5	10.3	1.5	10	ns
t _{PLZ}			1.5	7.9	10.3	1.5	11.2	1.5	10.8	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

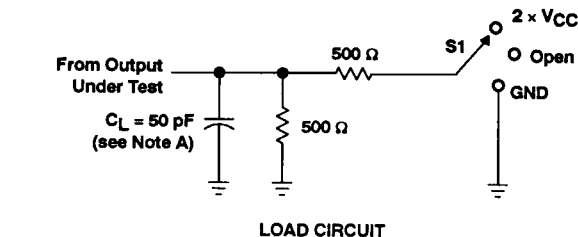
PARAMETER		TEST CONDITIONS		TYP	UNIT
C _{pd}	Power dissipation capacitance per buffer	Outputs enabled	C _L = 50 pF, f = 1 MHz	47	pF
		Outputs disabled		13	



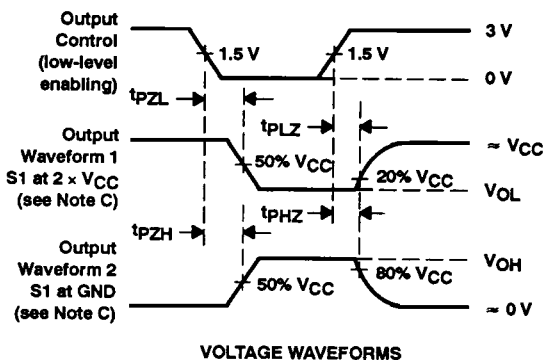
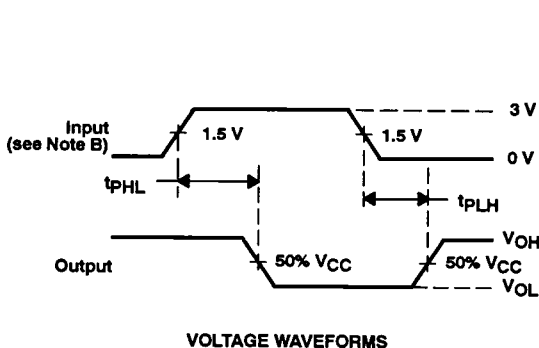
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PARAMETER MEASUREMENT INFORMATION



TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PZH}	GND



NOTES: A. C_L includes probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics: PRR $\leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r = 3 \text{ ns}$, $t_f = 3 \text{ ns}$.

C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
 Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms