

STL33N60M2-VB Datasheet

N-Channel 650 V (D-S) Super Junction Power MOSFET

PRODUCT SUMMARY

V_{DS} (V) at T_J max.	650	
$R_{DS(on)}$ at 25 °C (Ω)	$V_{GS} = 10$ V	0.160

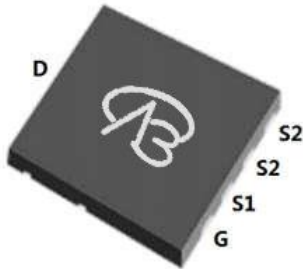
FEATURES

- Low figure-of-merit (FOM) $R_{on} \times Q_g$
- Low input capacitance (C_{iss})
- Reduced switching and conduction losses
- Ultra low gate charge (Q_g)
- Avalanche energy rated (UIS)

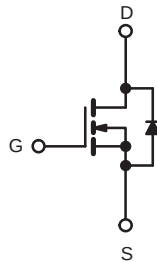


APPLICATIONS

- Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- Lighting
 - High-intensity discharge (HID)
 - Fluorescent ballast lighting



DFN8*8



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V _{DS}	650	V
Gate-Source Voltage			V _{GS}	± 30	
Continuous Drain Current (T _J = 150 °C)	V _{GS} at 10 V	T _C = 25 °C	I _D	20	A
		T _C = 100 °C		12	
Pulsed Drain Current ^a			I _{DM}	60	
Linear Derating Factor				1.67	W/°C
Single Pulse Avalanche Energy ^b			E _{AS}	580	mJ
Maximum Power Dissipation			P _D	90	W
Operating Junction and Storage Temperature Range			T _J , T _{stg}	-55 to +150	°C
Drain-Source Voltage Slope	T _J = 125 °C		dV/dt	50	V/ns
Reverse Diode dV/dt ^d		15			
Soldering Recommendations (Peak Temperature) ^c	for 10 s			260	°C

Notes

- Repetitive rating; pulse width limited by maximum junction temperature.
- $V_{DD} = 100$ V, starting $T_J = 25$ °C, $L = 30$ mH, $R_g = 25$ Ω , $I_{AS} = 13$ A.
- 1.6 mm from case.
- $I_{SD} \leq I_D$, $dI/dt = 100$ A/ μ s, starting $T_J = 25$ °C.

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	62	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	-	0.38	

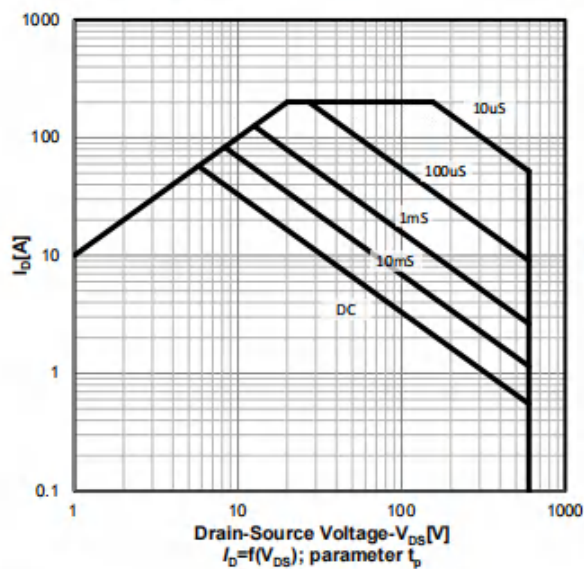
SPECIFICATIONS ($T_J = 25\text{ °C}$, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}$, $I_D = 1\text{ mA}$	650	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C , $I_D = 1\text{ mA}$	-	0.70	-	V/°C
Gate-Source Threshold Voltage (N)	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	2.5	-	4.5	V
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 20\text{ V}$	-	-	± 100	nA
		$V_{GS} = \pm 30\text{ V}$	-	-	± 1	μA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 650\text{ V}$, $V_{GS} = 0\text{ V}$	-	-	1	μA
		$V_{DS} = 520\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 125\text{ °C}$	-	-	100	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$, $I_D = 1.5\text{ A}$	-	0.160	-	Ω
Forward Transconductance	g_{fs}	$V_{DS} = 30\text{ V}$, $I_D = 1.5\text{ A}$	-	5.6	-	S
Dynamic						
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}$, $V_{DS} = 100\text{ V}$, $f = 1\text{ MHz}$	-	2600	-	pF
Output Capacitance	C_{oss}		-	330	-	
Reverse Transfer Capacitance	C_{rss}		-	4	-	
Effective Output Capacitance, Energy Related ^a	$C_{o(er)}$	$V_{DS} = 0\text{ V to } 520\text{ V}$, $V_{GS} = 0\text{ V}$	-	63	-	pF
Effective Output Capacitance, Time Related ^b	$C_{o(tr)}$		-	213	-	
Total Gate Charge	Q_g	$V_{GS} = 10\text{ V}$, $I_D = 20\text{ A}$, $V_{DS} = 520\text{ V}$	-	60	-	nC
Gate-Source Charge	Q_{gs}		-	39	-	
Gate-Drain Charge	Q_{gd}		-	47	-	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 520\text{ V}$, $I_D = 20\text{ A}$, $V_{GS} = 10\text{ V}$, $R_g = 9.1\text{ }\Omega$	-	18	25	ns
Rise Time	t_r		-	24	55	
Turn-Off Delay Time	$t_{d(off)}$		-	80	-	
Fall Time	t_f		-	12	-	
Gate Input Resistance	R_g	$f = 1\text{ MHz}$, open drain	-	0.8	-	Ω
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	20	A
Pulsed Diode Forward Current	I_{SM}		-	-	60	
Diode Forward Voltage	V_{SD}	$T_J = 25\text{ °C}$, $I_S = 8\text{ A}$, $V_{GS} = 0\text{ V}$	-	-	1.5	V
Reverse Recovery Time	t_{rr}	$T_J = 25\text{ °C}$, $I_F = I_S = 8\text{ A}$, $dI/dt = 100\text{ A}/\mu\text{s}$, $V_R = 400\text{ V}$	-	60	-	ns
Reverse Recovery Charge	Q_{rr}		-	5.8	-	μC
Reverse Recovery Current	I_{RRM}		-	45	-	A

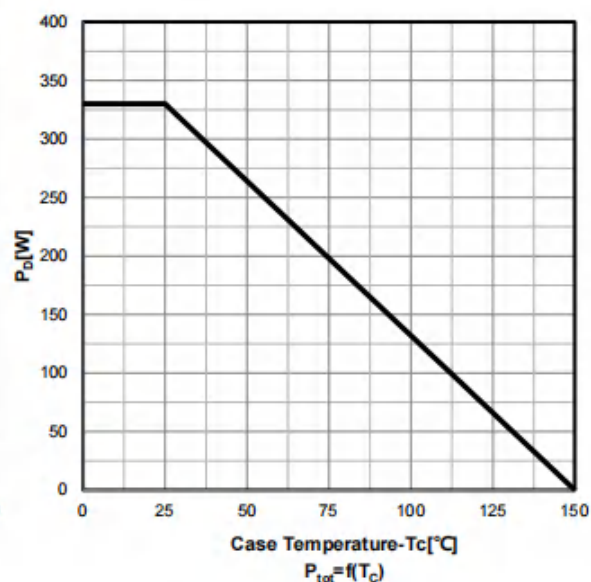
Notes

- a. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS} .
 b. $C_{oss(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS} .

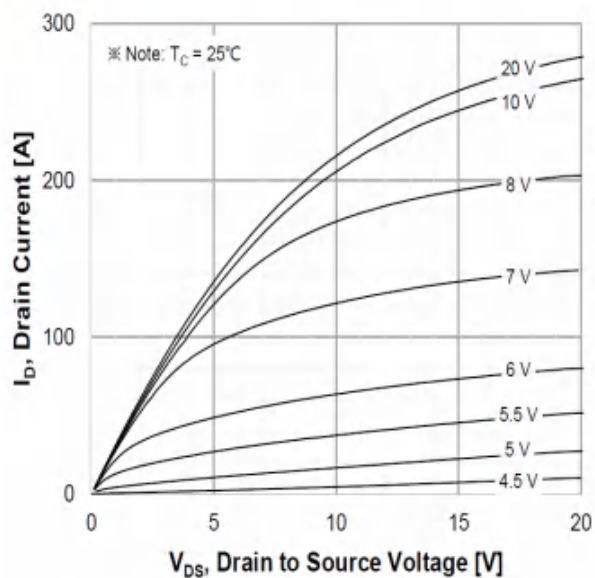
Safe operating area $T_C=25\text{ }^{\circ}\text{C}$
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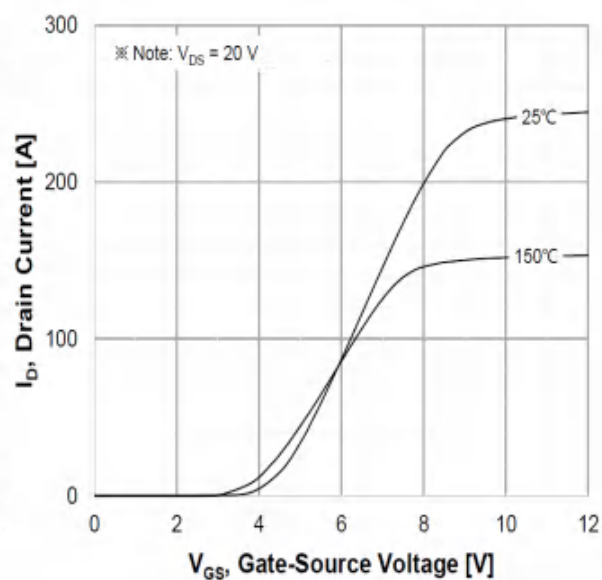
Power dissipation



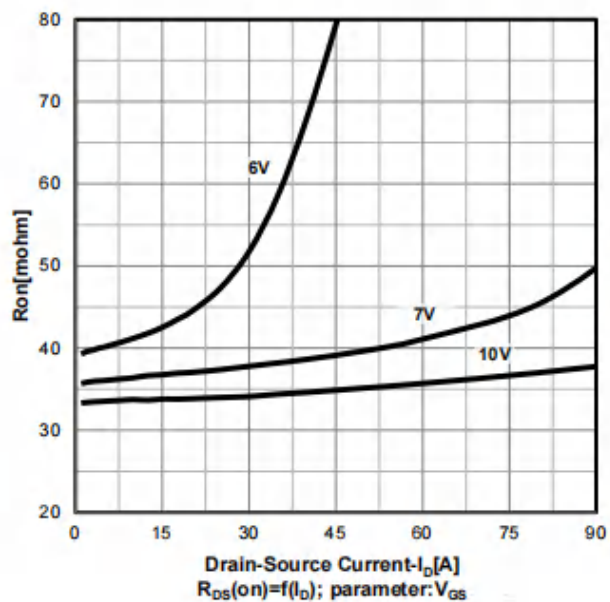
Typ. output characteristics $T_J=25\text{ }^{\circ}\text{C}$



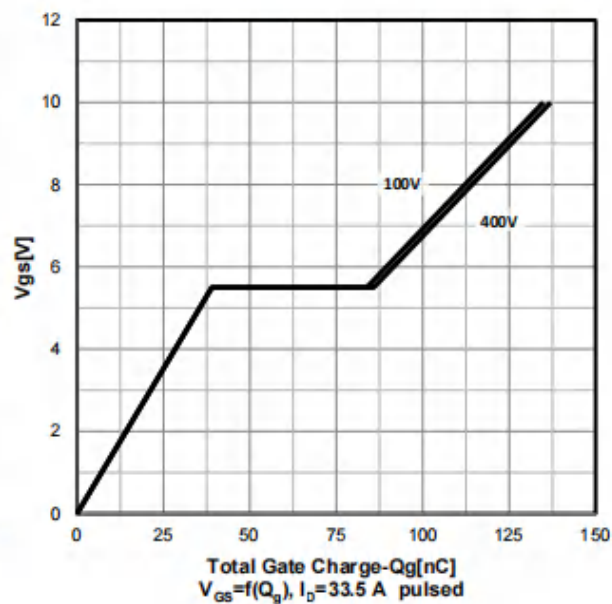
Transfer characteristics



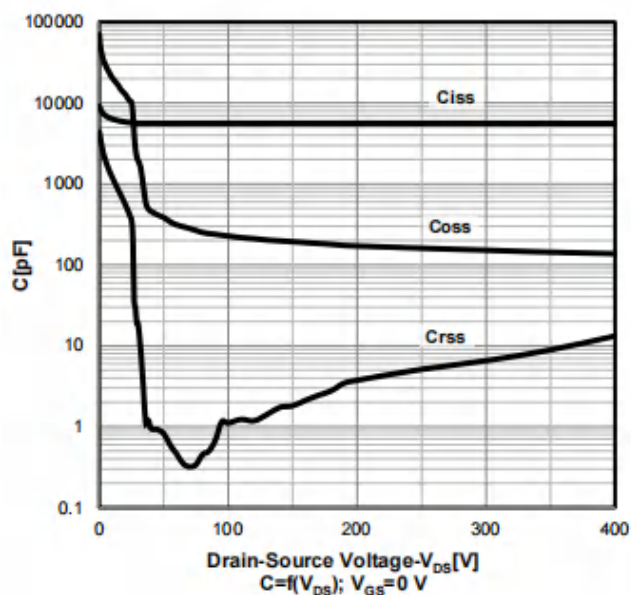
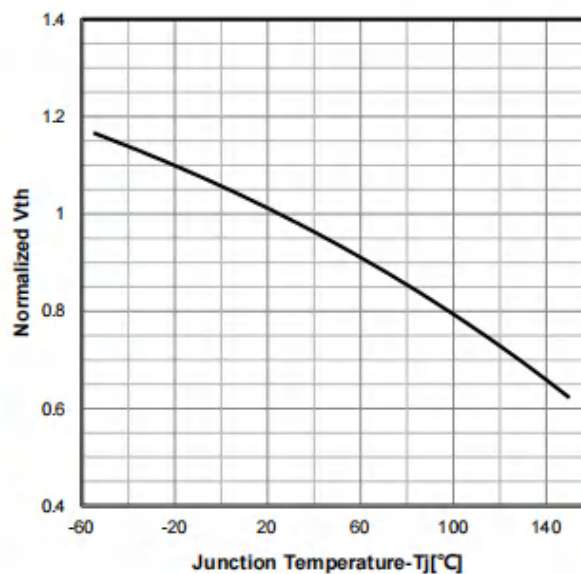
Typ. drain-source on-state resistance



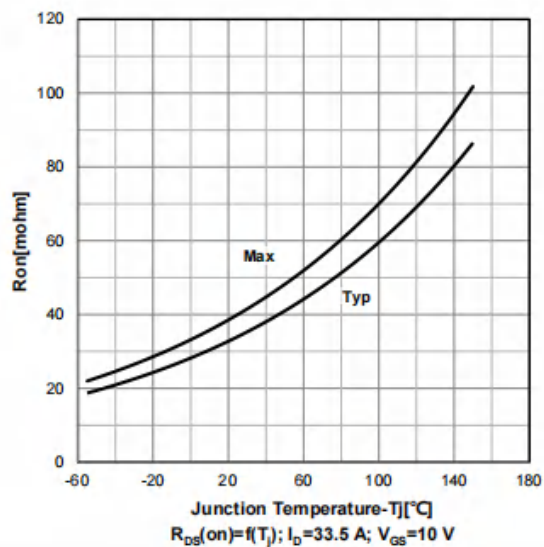
Typ. gate charge characteristics



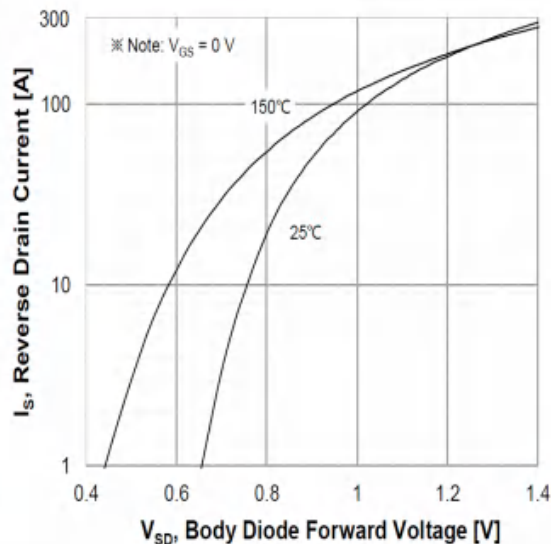
Typ. capacitances

Normalized $V_{GS(th)}$ characteristics

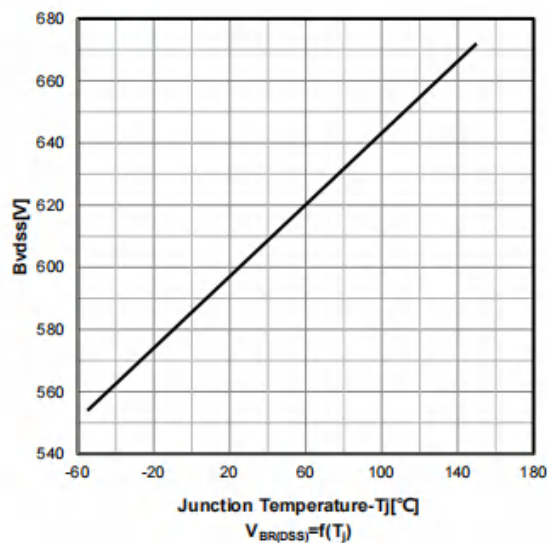
On-resistance vs temperature



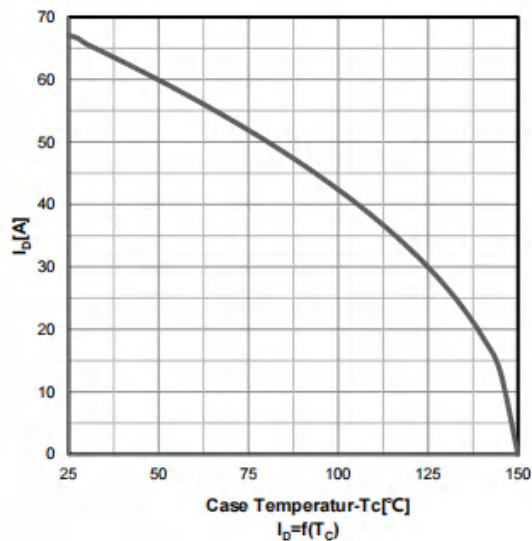
Forward characteristics of reverse diode



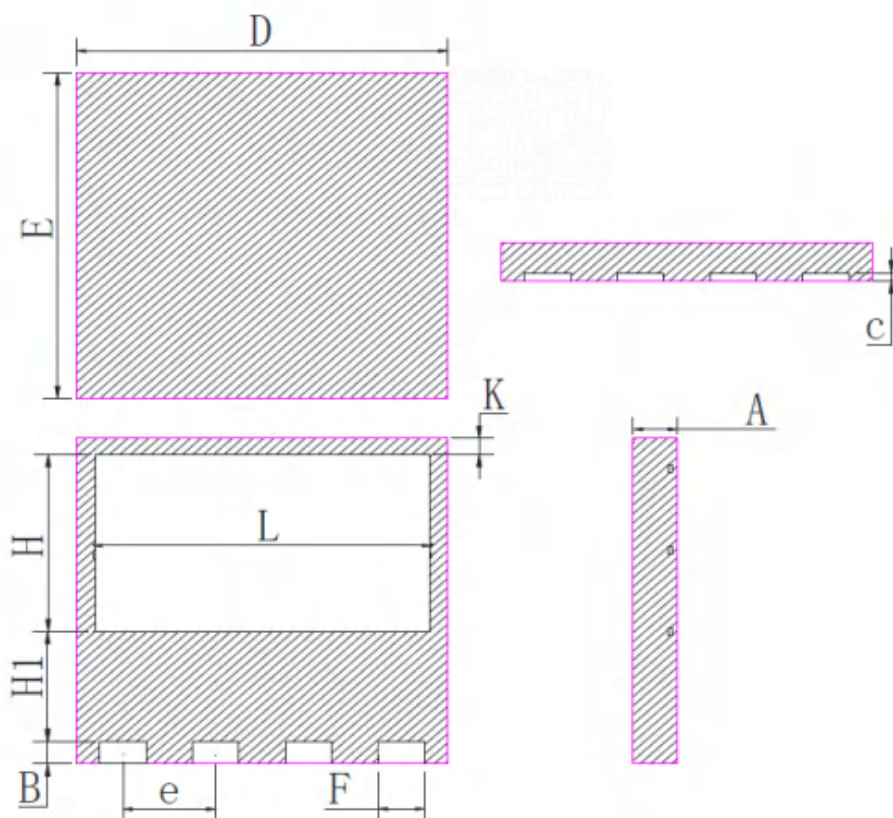
Drain-source breakdown voltage



Drain current vs temperature



Package Outline : D F N 8 X 8



Symbol	Min	Typ	Max
A	0.90	0.95	1.00
B	0.45	0.55	0.65
C	0.153	0.203	0.253
D	7.90	8.00	8.10
E	7.90	8.00	8.10
e	1.90	2.00	2.10
F	0.90	1.00	1.10
H	4.20	4.35	4.45
H1	2.60	2.70	2.80
K	0.30	0.40	0.50
L	7.10	7.20	7.30

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