■ General Description

OCA72559FQAD is a mono, filter-free Class D audio power amplifier with optimized automatic gain control (AGC) and synchronous Boost. AGC functions are not only configured to prevent audio signal distortion but also to enhance sound quality and volume automatically. It also can be configured to protect the speaker from damage at high power levels. The high voltage boost achieves high output voltage which can improve music signal dynamic range significantly. OCA72559FQAD is cable of driving 6.1W at 4.2V into a 6Ω load or 5.4W at 4.2V into a 8Ω load with speaker mode.

OCA72559FQAD also supports speaker and receiver 2-in-1 application. In receiver mode, the noise floor can be achieved 9 μVrms and total harmonic distortion (THD) can be achieved 0.008% with 0.1W at 4.2V into a 8Ω load.

In addition to these features, I2C interface makes easier commutation between AP and OCA72559FQAD.

The device is a RoHs compliant FCQAD 2mm x 3mm x 0.55mm -20L package.

■ Applications

- Smartphones, Cellphone, PDAs
- Bluetooth, wireless handsets
- Portable equipment

■ Features

- Power Voltage Range: 2.7V to 5.5V
- Boost Output Voltage Ranger: up to 10.5V
- Support Speaker & Receiver 2-in-1 mode
- Overall Efficiency up to 85
- Output power 5.4W@8Ω, 6.1W@6Ω,
- Adjustable speaker-guard power level: 0.5W~2W@8Ω,100mW/Step
- Low Noise:
  9 μVrms (Class D Receiver@0dB)
  18 μVrms (Class D Receiver@9dB)
  35 μVrms (Class D Speaker@18dB)
- PSRR: -82dB @ 217Hz
- Optimized AGC control for sound quality
- Battery tracking for low voltage protection
- Excellent TDD noise suppression and POP-Click noise suppression
- Shut Down Current: 0.1μA
- Support 1.8V I2C interface
- FCQFN20L, 2mm x 3mm x 0.55mm

■ Pin Configuration

FCQFN-20(Top View)

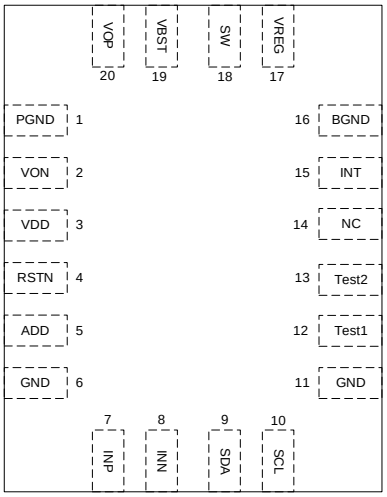


Figure 1, Pin Assignments of OCA72559FCR

Pin Name	Pin No. FCQFN-20L	Pin Function
PGND	1	Class D power ground
VON	2	Negative audio output terminal
VDD	3	Power supply
RSTN	4	Reset pin, active low reset, the internal 2MΩ pull-down resistor in chip
ADD	5	I2C slave address pin
GND	6	Ground
INP	7	Positive audio input terminal
INN	8	Negative audio input terminal
SDA	9	I2C data
SCL	10	I2C clock
GND	11	Ground
TEST1	12	TEST pins, connect to GND in application
TEST1	13	TEST pins, connect to GND in application
NC	14	NC pins, connect to GND in application
INT	15	INT pins, connect to GND in application
BGND	16	Boost power ground
VREG	17	Charge pump output pin
SW	18	Boost switch pin
VBST	19	Boost output pin
VOP	20	Positive audio output terminal

■ Typical Application Circuit

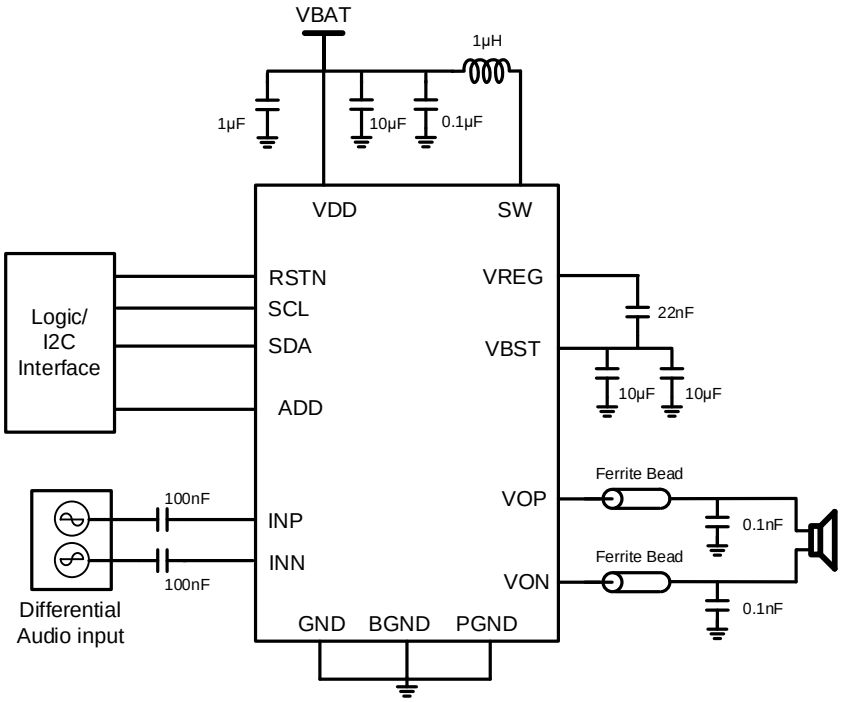


Figure 2, Typical Application Block diagram of OCA72559FQAD

■ Ordering Information

Part Number	Package Type	Marking	Package Qty	Temperature	Eco Plan	Lead
OCA72559FQAD	FC-QFN2030-20L	BLU	3000pcs	-40～85℃	Green	Su/Ag/Cu

■ Block Diagram

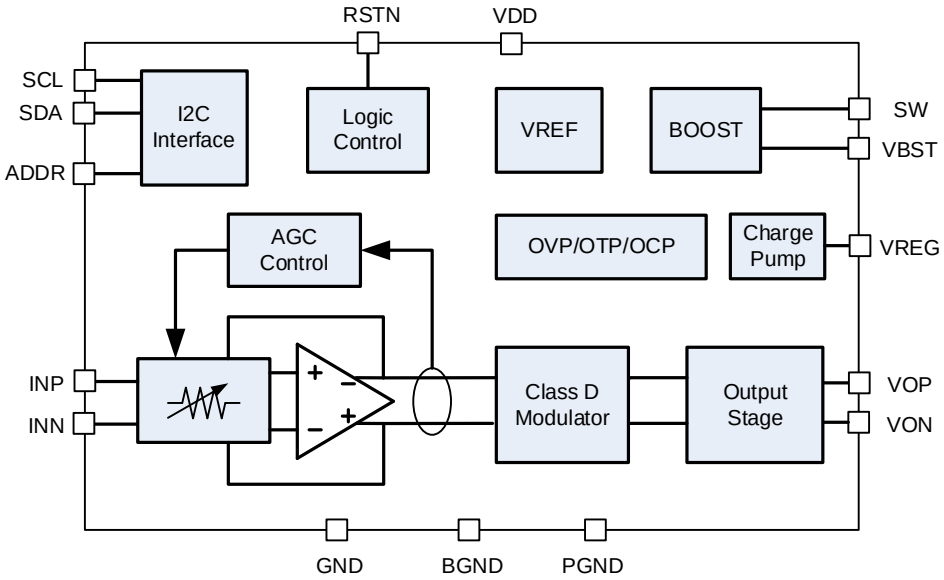


Figure 3, OCA72559FQAD Block Diagram

■ Absolute Maximum Ratings[1] (T_A=25°C unless otherwise noted)

Parameter	Symbol	Rating	Unit
Power Voltage Range	VDD	-0.3 to 6.5	V
Boost Output Voltage Range	VBST	-0.3 to 12	V
Boost Switch Pin Voltage	SW	-0.3 to VBST+2	V
Input Voltage Range	INP,INN	-0.3 to VDD+0.3	V
Output Voltage Range	VOP,VON	-0.3 to VBST+0.3	V
Human Body Model	HBM	2	kV
Charged Device Model	CDM	1.5	kV
Storage Temperature Range	T_S	-55 to +150	°C
Maximum Operating Junction Temperature Range	T_J	-40 to 125	°C

Notes1: Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

■ Recommended Operating Conditions[2](T_A=25°C unless otherwise noted)

Parameter	Symbol	Rating	Unit
Power Supply Voltage	VDD	2.7 ~ 5.5	V
Ambient Operating Temperature	T_A	-40 to 85	°C
Thermal Resistance	$R_{\theta JA}$	58	°C /W

Notes2: The device is not guaranteed to function outside of its operating conditions

■ Electrical Characteristics

(Unless otherwise noted, typical values are at T_A=25°C, VDD= 4.2V, VBST=9.0V, R_L= 8Ω+33μH, f=1kHz)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
VDD	Power Supply Voltage		2.7		5.5	V
V_{UVLO}	Under-Voltage Lockout Threshold			2.5		V
$V_{UVLO-HYS}$	UVLO hysteresis voltage			50		mV
I_{SD}	Shutdown current	VDD=3.6V, RSTN=0V		0.1	1	μA
T_{ON}	Turn-on Time			45		ms
BOOST						
VBST	Boost Output Voltage[4]	VDD=2.7V to 5.5V		9.5		V
V_{OVP}	Over Voltage Protection Threshold	VDD=2.7V to 5.5V		VBST +0.5		V
$V_{OVP-HYS}$	OVP hysteresis voltage	VDD=2.7V to 5.5V		200		mV
I_{L_PEAK}	Inductor Peak Current limit[4]			3.5		A
F_{SW}	Switching Frequency	Switch frequency	1.2	1.6	2	MHz
D_{MAX}	The Maximum Duty Cycle			90		%
T_{ST}	Soft Start Time	C_{OUT}=22μF		2		ms
η	Boost Efficiency	VDD=4.2V, I_{LOAD}=200mA		87		%
Speaker Mode						
V_{OS}	Output offset voltage	AC ground input	-30		30	mV
η_T	Speaker Mode Total Efficiency	VDD=4.2V, P_O=0.4W, R_L=8Ω+33μH		86		%
		VDD=4.2V, P_O=2.5W, R_L=8Ω+33μH		82		%
I_Q	Speaker Quiescent Current at ADP BOOST MODE	VDD=4.2V, Input ac ground. R_L=8Ω+33μH		7		mA

	Speaker Quiescent Current	VDD=4.2V, Input ac ground. R_L=8Ω+33μH, VBST=9V		18		
	Speaker Quiescent Current	VDD=4.2V, Input ac ground. R_L=8Ω+33μH, VBST=10.5V		20		
V_{IN}	Recommend Input Signal Amplitude	VDD=2.7V to 5.5V			1	Vp
F_{OSC}	Modulation Frequency	VDD=2.7V to 5.5V	600		1000	kHz
P_{AGC}	AGC Power[4]	R_L=8Ω+33μH	0.72	0.8	0.88	W
		R_L=6Ω+33μH	0.96	1.067	1.17	
PSRR	Power Supply Rejection Rate	VDD=4.2V, Vpp-sin=200mV, 217Hz		-82		dB
		VDD=4.2V, Vpp-sin=200mV, 1kHz		-80		
A_V	Speaker Gain[4]	VDD=2.7V to 5.5V		24		dB
R_{DSON}	PA Driver On-state Resistance	High side + Low side		250		mΩ
SNR	Signal-to-Noise Ratio	VDD=4.2V, PO=4.75W, RL=8Ω+33μH, A_V=18dB		103		dB
		VDD=4.2V, PO=0.8W, RL=8Ω+33μH, A_V=18dB		95		
E_N	Speaker Output Noise	20Hz to 20kHz, input AC ground with A-weighting filter, A_V=24dB		44		μV
		20Hz to 20kHz, input AC ground with A-weighting filter, A_V=18dB		34		μV
R_{IN}	Speaker Input Inner Resistance	A_V=24dB		9		kΩ
		A_V=18dB		18		
F_{IN}	Speaker Input Cut-off Frequency	C_{IN}=47nF, A_V=24dB		376		Hz
		C_{IN}=47nF, A_V=18dB		188		
		C_{IN}=68nF, A_V=24dB		260		
		C_{IN}=68nF, A_V=18dB		130		
		C_{IN}=100nF, A_V=24dB		177		
		C_{IN}=100nF, A_V=18dB		88		
THD+N	Total Harmonic Distortion + Noise	VDD=4.2V, PO=0.8W, R_L=8Ω+33μH, f=1kHz		0.012		%
P_O	Speaker Output Power	THD+N=1%, R_L=8Ω+33μH, VDD=4.2V, VBST=9.0V, I_{L_PEAK}=4A		4.8		W
		THD+N=10%, R_L=8Ω+33μH, VDD=4.2V, VBST=9.0V, I_{L_PEAK}=4A		5.8		
		THD+N=1%, R_L=6Ω+33μH, VDD=4.2V, VBST=9.0V, I_{L_PEAK}=4A		5.7		
		THD+N=10%, R_L=6Ω+33μH, VDD=4.2V, VBST=9.0V, I_{L_PEAK}=4A		6.5		
Receiver Mode						
I_Q	Receiver Mode Quiescent Current	VDD=4.2V, Input ac ground. R_L=8Ω+33μH		6.8		mA
η	Receiver Mode Total Efficiency	VDD=4.2V, P_O=0.8W, R_L=8Ω+33μH		91		%
A_V	Receiver Mode Gain[4]	VDD=2.7V to 5.5V		0		dB
R_{IN}	Receiver Mode Input Inner Resistance	A_V=9dB		38		kΩ
F_{IN}	Receiver Mode Input Cut-off Frequency	C_{IN}=47nF, A_V=9dB		89		Hz
		C_{IN}=68nF, A_V=9dB		62		

		C_{IN}=100nF, A_V=9dB		42		
E_N	Receiver Mode Output Noise	20Hz to 20kHz, input AC ground with A-weighting filter, A_V=0dB		9		μV
		20Hz to 20kHz, input AC ground with A-weighting filter, A_V=9dB		13.5		
THD+N	Total Harmonic Distortion + Noise	VDD=4.2V, PO=0.1W, R_L=8Ω+33μH, f=1kHz		0.008		%
PSRR	Power Supply Rejection Rate	VDD=4.2V, Vpp-sin=200mV, 217Hz		82		dB
		VDD=4.2V, Vpp-sin=200mV, 1kHz		75		
P_O	Receiver Mode Output Power	THD+N=1%, R_L=8Ω+33μH, VDD=4.2V,GAIN=7.5~10.5dB		1.0		W
Automatic Gain Control (AGC)						
T_{AT_Lim}	Limiter Attack Time[4]			0.08		ms/dB
T_{AT_Fast}	Fast AGC Attack Time[4]			0.64		ms/dB
T_{AT_Slow}	Slow AGC Attack Time[4]			41		ms/dB
T_{RLT}	Slow AGC Release Time			21		ms/dB
A_{MAX}	The Maximum Attenuation Gain	VDD=2.7V to 5.5V		-13.5		dB
Battery Tracking Function						
V_{B-TH}	Battery Protection Threshold[4]			3.4		V
V_{B-HYS}	Battery Protection Threshold Hysteresis			100		mV
Thermal Information						
T_{SHDN}	Thermal Shutdown Temperature			160		°C
T_{PRO}	Thermal Protection Temperature			150		°C
T_{REC}	Thermal Protection Recovery Temperature			130		°C
I/O Interface						
V_{IH}	High Level Input Voltage of SCL, SDA, RSTN, ADD		1.3		VDD	V
V_{IL}	Low Level Input Voltage of SCL, SDA, RSTN, ADD				0.45	V
$V_{OLSDA/INT}$	Low level Output Voltage	I_{OL}=2mA			0.3	V
$I_{OLSDA/INT}$	Low level Output Current	$V_{OLSDA/INT}$=0.2V	10			mA

I2C Compatible Timing Specifications (SCL, SDA), see Figure 4						
f_{SCL}	SCL clock frequency	Standard Mode	-	-	100	KHz
		Fast Mode	-	-	400	KHz
t_{LOW}	Low period of the SCL clock	Standard Mode	4.7	-	-	us
		Fast Mode	1.3	-	-	us
t_{HIGH}	High period of the SCL clock	Standard Mode	4.0	-	-	us
		Fast Mode	0.6	-	-	us
t_{BUF}	Bus free time between a STOP and START condition	Standard Mode	4.7	-	-	us
		Fast Mode	1.3	-	-	us
$t_{HD,STA}$	Hold time for a repeated START condition	Standard Mode	4.0	-	-	us
		Fast Mode	0.6	-	-	us
$t_{SU,STA}$	Setup time for a repeated START condition	Standard Mode	4.7	-	-	us
		Fast Mode	0.6	-	-	us
$t_{SU,DAT}$	Data setup time	Standard Mode	0.25	-	-	us
		Fast Mode	0.1	-	-	us
$t_{HD,DAT}$	Data hold time	Standard Mode	0.05	-	3.45	us
		Fast Mode	0.05	-	0.9	us
t_{RCL1}	Rise time of SCL signal after a repeated START condition and after an acknowledge bit	Standard Mode	$20+0.1C_B$	-	1000	ns
		Fast Mode	$20+0.1C_B$	-	1000	ns
t_{RCL}	Rise time of SCL signal	Standard Mode	$20+0.1C_B$	-	1000	ns
		Fast Mode	$20+0.1C_B$	-	300	ns
t_{FCL}	Fall time of SCL signal	Standard Mode	$20+0.1C_B$	-	300	ns
		Fast Mode	$20+0.1C_B$	-	300	ns
t_{RDA}	Rise time of SDA signal	Standard Mode	$20+0.1C_B$	-	1000	ns
		Fast Mode	$20+0.1C_B$	-	300	ns
t_{FDA}	Fall time of SDA signal	Standard Mode	$20+0.1C_B$	-	300	ns
		Fast Mode	$20+0.1C_B$	-	300	ns
$t_{SU,STO}$	Setup time for STOP condition	Standard Mode	4.0	-	-	us
		Fast Mode	0.6	-	-	us
C_B	Capacitive load for SCL and SDA		-	-	0.4	nF

Note3: OCA72559FQAD is guaranteed to meet performance specifications over the –40°C to +85°C operating temperature range by design, characterization and correlation with statistical process controls.

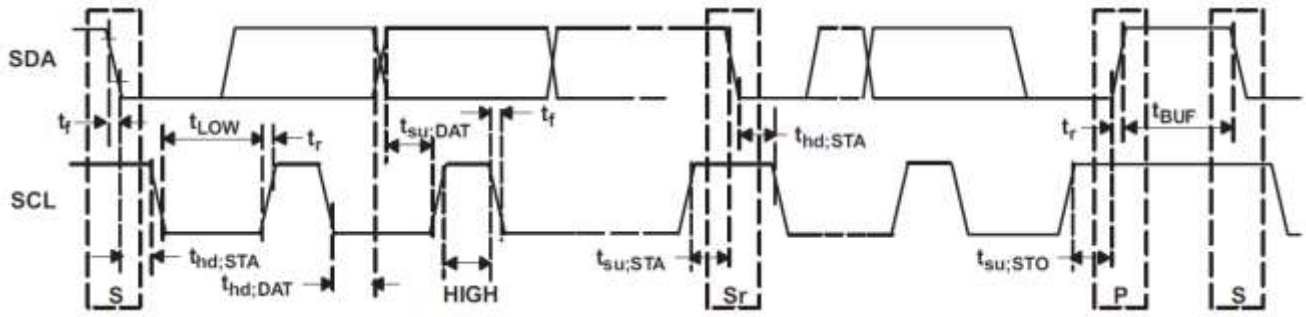
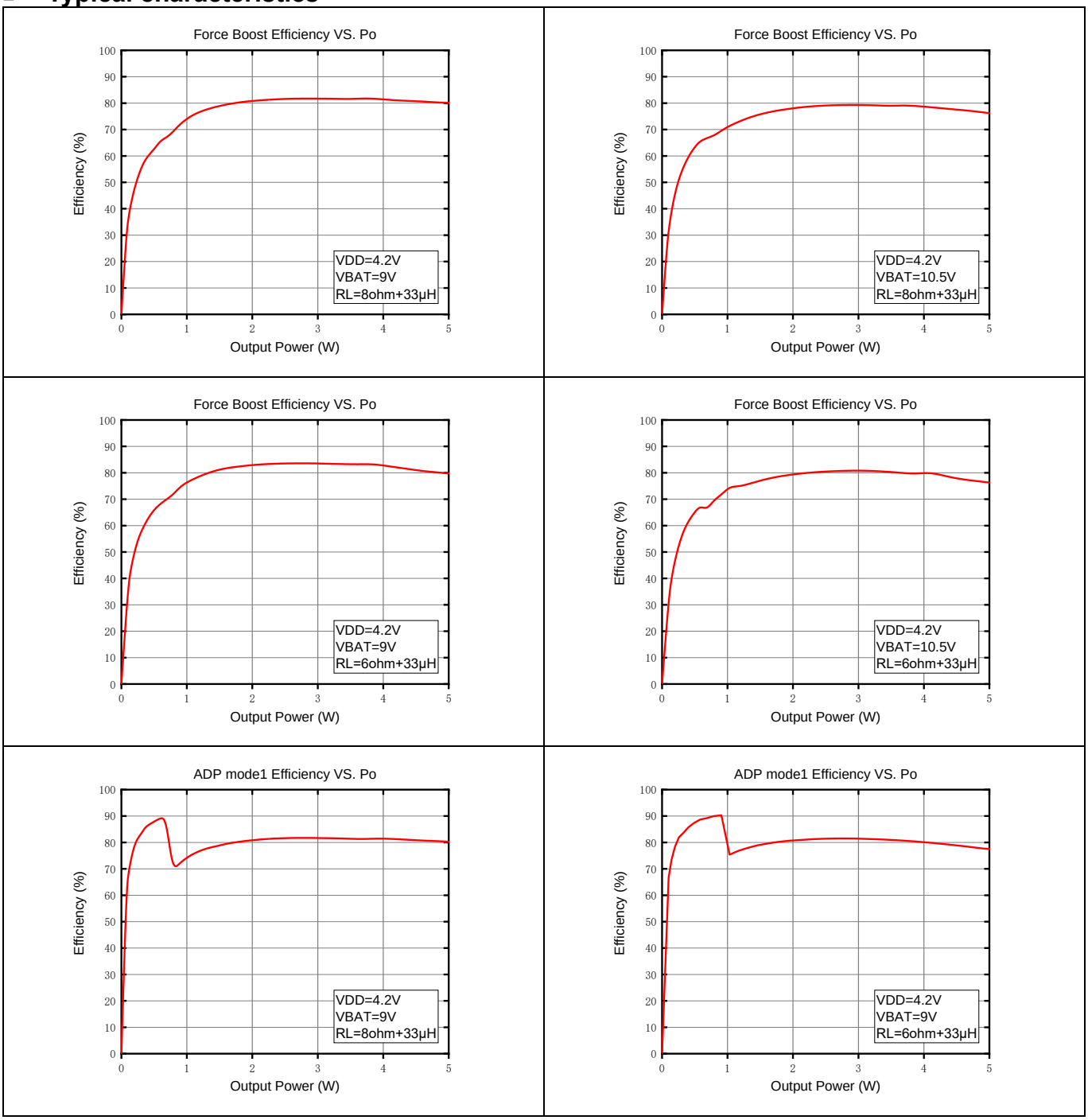
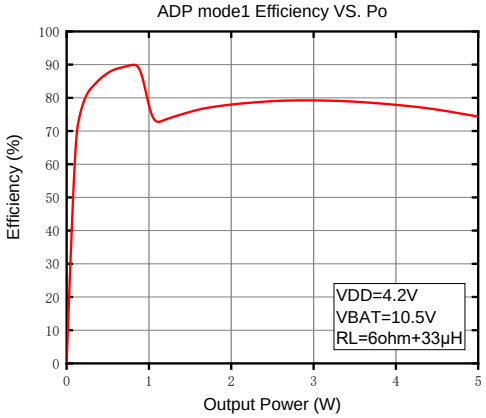


Figure 4,Serial Interface Timing for F/S-Mode I2C

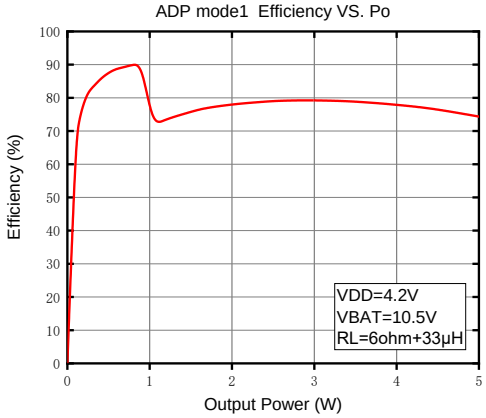
■ Typical characteristics



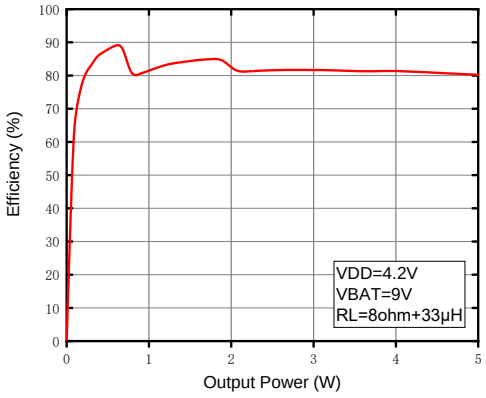
ADP mode1 Efficiency VS. Po



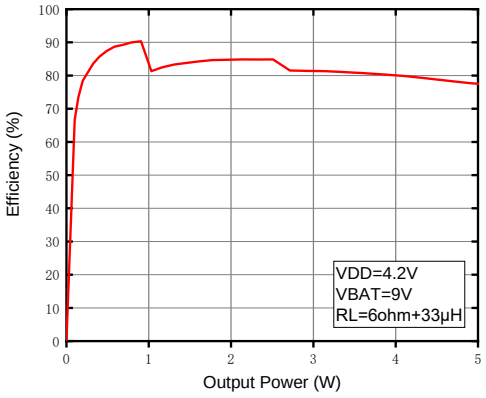
ADP mode1 Efficiency VS. Po



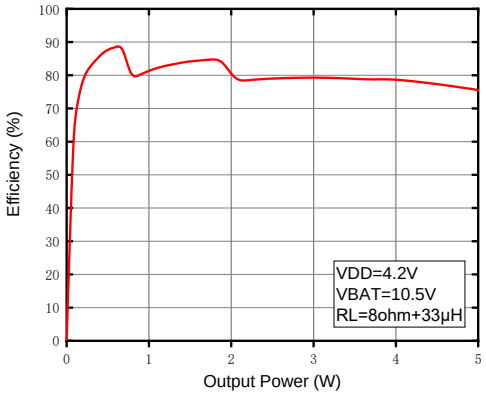
ADP mode2 Efficiency VS. Po



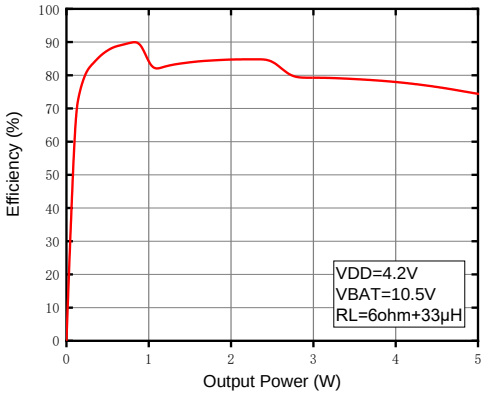
ADP mode2 Efficiency VS. Po



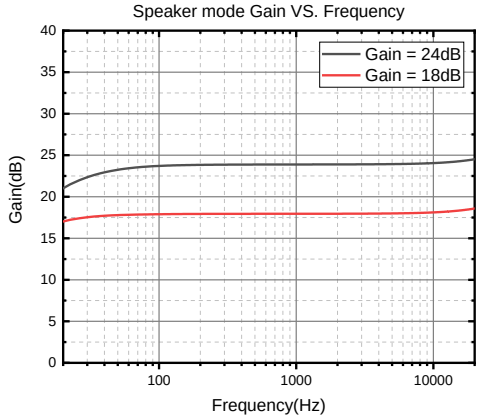
ADP mode2 Efficiency VS. Po



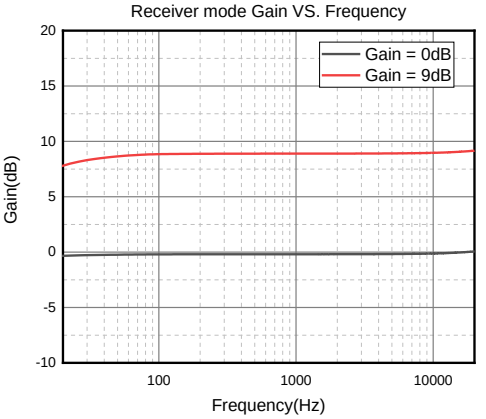
ADP mode2 Efficiency VS. Po



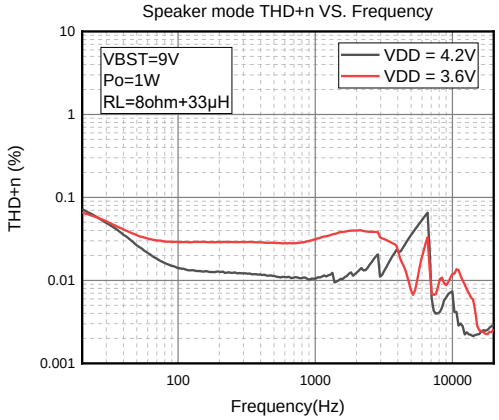
Speaker mode Gain VS. Frequency



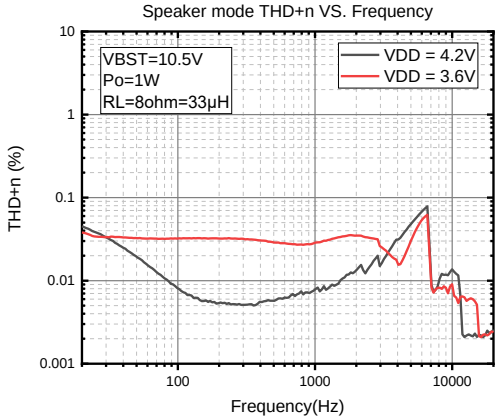
Receiver mode Gain VS. Frequency



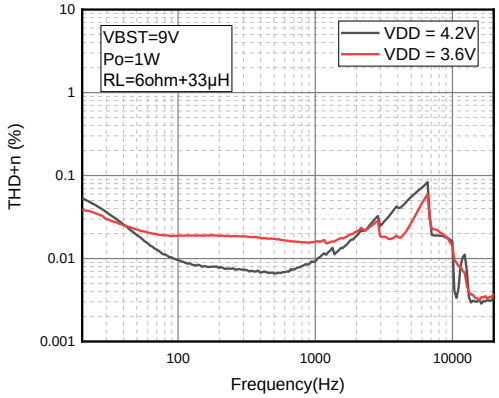
Speaker mode THD+n VS. Frequency



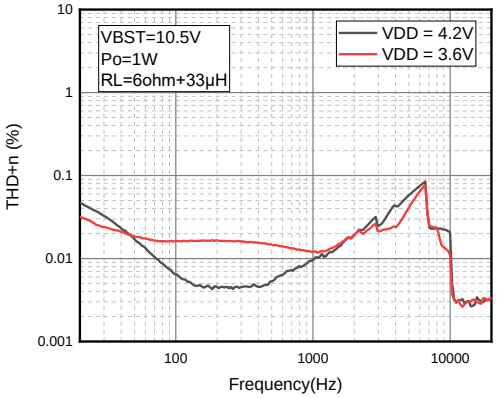
Speaker mode THD+n VS. Frequency



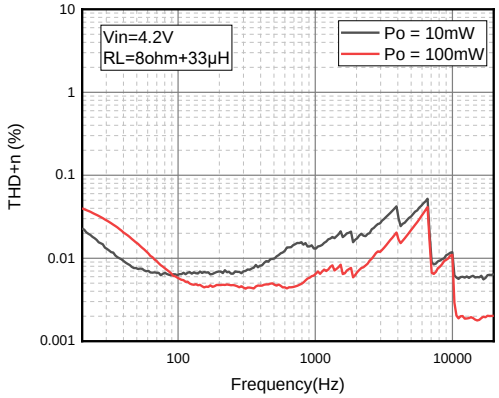
Speaker mode THD+n VS. Frequency



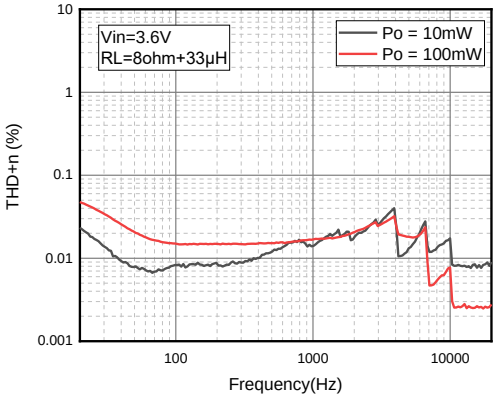
Speaker mode THD+n VS. Frequency



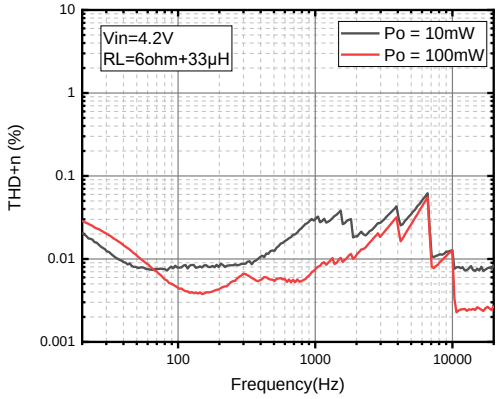
Receiver mode THD+n VS. Frequency



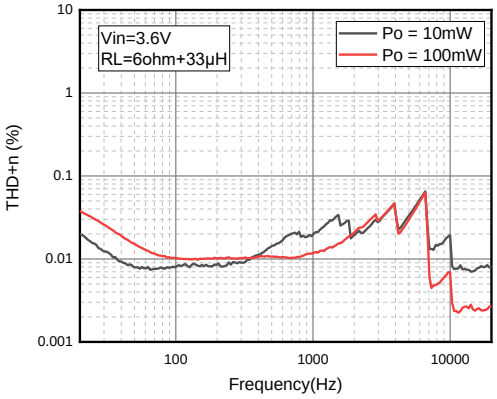
Receiver mode THD+n VS. Frequency



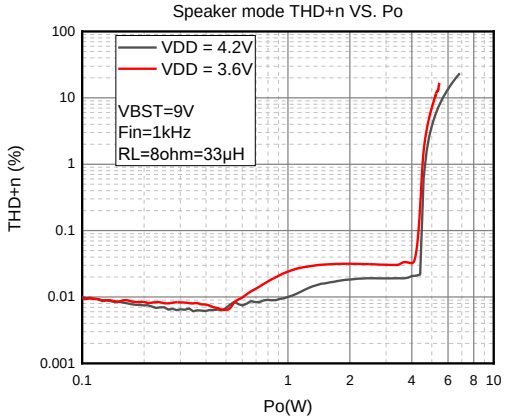
Receiver mode THD+n VS. Frequency



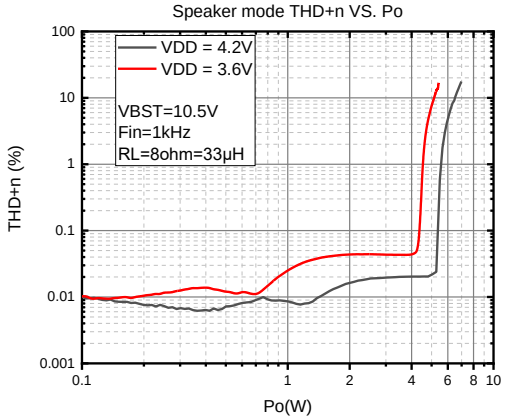
Receiver mode THD+n VS. Frequency



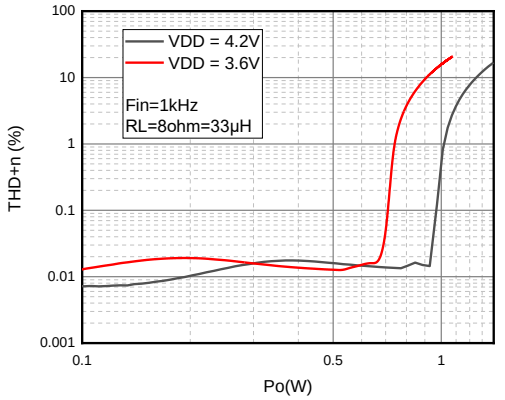
Speaker mode THD+n VS. Po



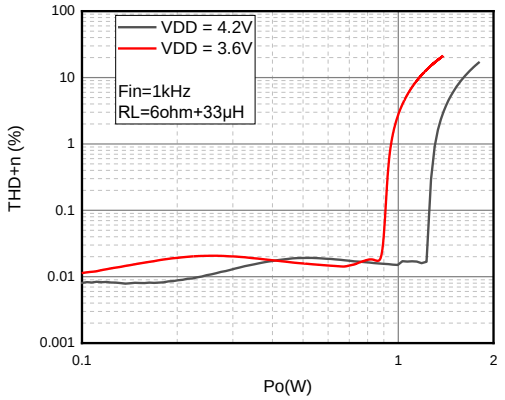
Speaker mode THD+n VS. Po



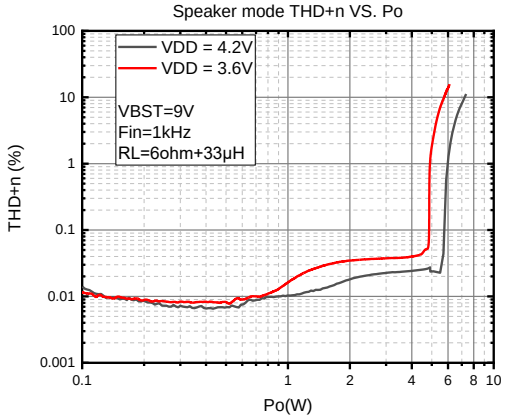
Receiver mode THD+n VS. Po



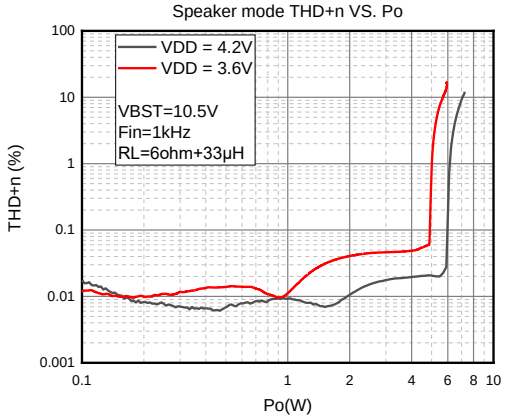
Receiver mode THD+n VS. Po



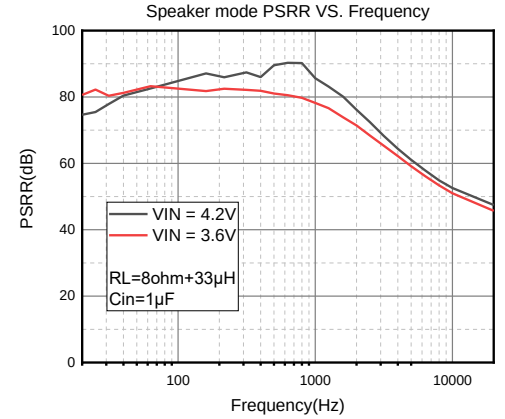
Speaker mode THD+n VS. Po



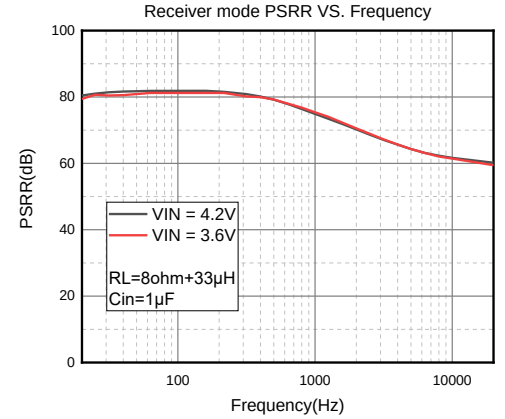
Speaker mode THD+n VS. Po

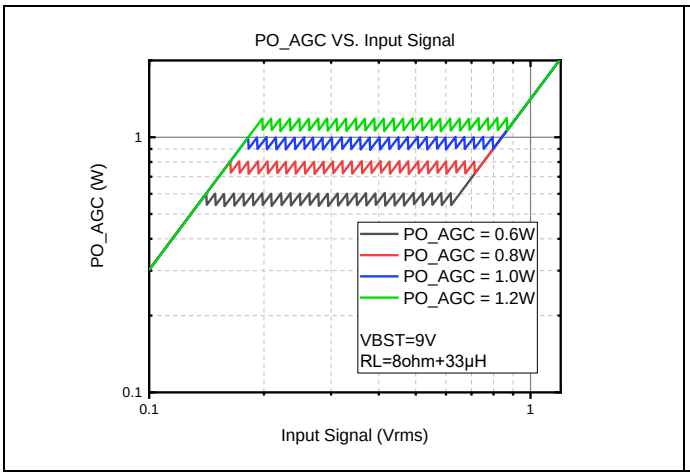


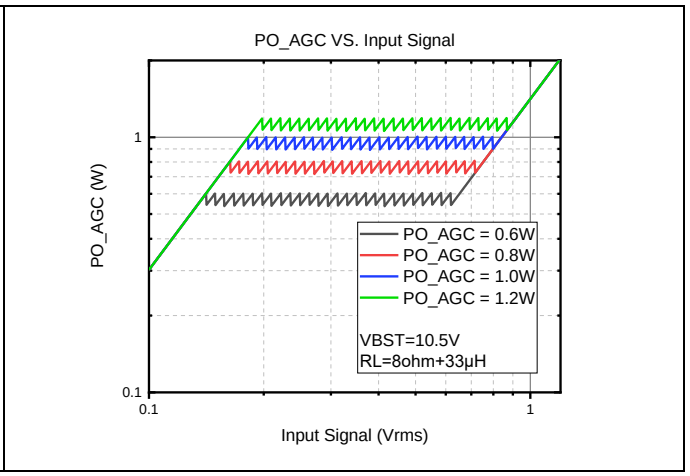
Speaker mode PSRR VS. Frequency



Receiver mode PSRR VS. Frequency







■ Detail Description

OCA72559FQAD is a mono, filter-free Class D audio power amplifier with optimized automatic gain control (AGC) and synchronous Boost. AGC functions are not only configured to prevent audio signal distortion but also to enhance sound quality and volume automatically. It also can be configured to protect the speaker from damage at high power levels. The high voltage boost achieves high output voltage which can improve music signal dynamic range significantly. OCA72559FQAD also supports speaker and receiver 2-in-1 application. In receiver mode, the noise floor can be achieved 9μVrms and total harmonic distortion (THD) can be achieved 0.008% with 0.1W at 4.2V into an 8Ω load. The AGC/Boost function is programmable via a digital I2C interface.

Automatic Gain Control:

The Automatic Gain Control (AGC) feature provides continuous automatic gain adjustment to the amplifier through an internal programable gain control circuit. When it is enabled, AGC monitors This feature enhances the perceived audio loudness and at the same time prevents speaker damage from occurring (Limiter function).

The AGC function is implemented by Limiter, Fast AGC and Slow AGC. It detects the audio input and change internal gain to modify output signal amplitude. The gain step of AGC is 0.5dB. The AGC basic behavior is shown in Figure5.

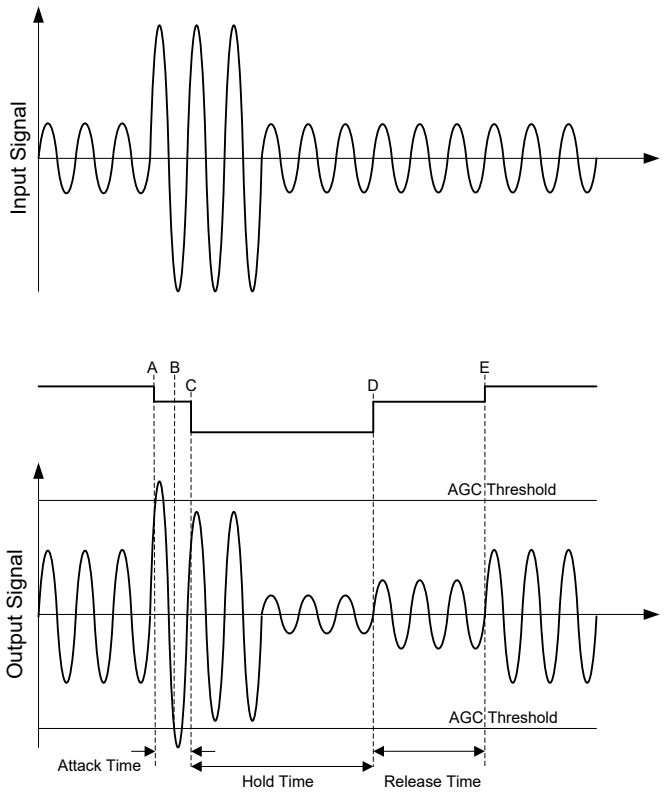


Figure 5,The AGC basic behavior

A. Gain decreases with no delay; attack time is reset. Release time and hold time are reset.

B. Signal amplitude above limiter level, but gain cannot change because attack time is not over.

C. Attack time ends; gain is allowed to decrease from this point forward by one step. Gain decreases because the amplitude remains above limiter threshold. All times are reset.

D. Gain increases after release time finishes and signal amplitude remains below desired level. All times are reset after the gain increase.

E. Gain increases after release time is finished again because signal amplitude remains below desired level. All times are reset after the gain increase.

Supply Tracking Limiters:

OCA72559FQAD monitors battery voltage (VBAT) and the Boost voltage (VBST) along with the audio signal to automatically decrease gain when VBAT or VBST voltage is lower than a programmable threshold. The limiters

threshold can be configured to track the monitored voltage below a programmable voltage which is set by register 0x02h [4:3]. The output voltage is set by 0x02h [1:0] when device is under Supply Tracking.

Speaker & Receiver 2 in 1:

OCA72559FQAD supports Speaker application and Receiver application which can be set by register. The Speaker and Receiver signal use one signal path together, customers do not need extra component, so the system cost and PCB space are saved.

OCS-Zero adjustment

Traditional AGC doesn't contain OCS-Zero adjustment technology; AGC gain changes generally at the peak, the gain variation at the peak would generate a certain transient distortion, such distortions are audibly imperceptible. Such as individual songs have a slight click.

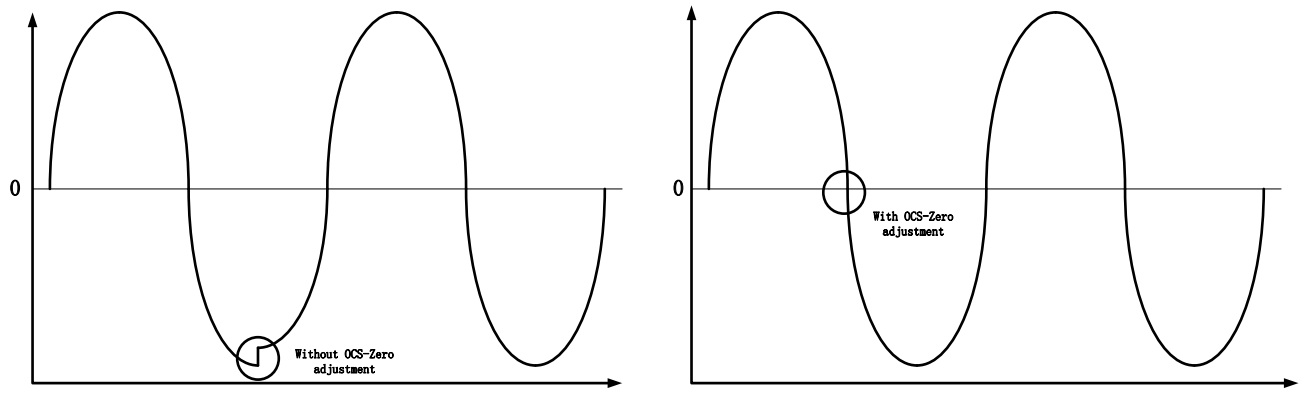


Figure 6, Traditional AGC & OCS-Zero AGC

Power Protection under Lower Battery voltage

Phone battery voltage will drop in the process of phone in use. When the battery voltage is low, a sudden high current could let the phone shut down. Power protection under low battery voltage feature can limit Audio PA current when battery voltage is low. It monitors battery voltage and modify the AGC gain automatically if the battery voltage is below the safety threshold, so as to decrease the output voltage and the power supply current, which effectively prevents high current.

Sync Boost technology

Peak current mode synchronous PWM Boost as Class D power stage supply is integrated to increase output voltage dynamic range. 1.6MHz switching frequency reduces PCB size and external component size.

Boost output voltage can be set through the I2C register 0x03h [4:0] and current limit can be configured by register 0x04h[4:2].

Soft-start function to prevent overshoot current during powering-on, Integrated the output protection circuit and self-recovery function; integrated Anti-Ring circuit to reduce EMI in DCM mode; built-in substrate switching shutdown circuit, effectively preventing the input and output leakage current anti-irrigation.

Sync Adaptive Boost technology

To improve system efficiency during low or middle audio output, adaptive Boost method is adopted. The Boost output varies with output level. When PA output power is less than Boost_Level_1, the Boost is at direct though mode and VBST is equal to VDD. When PA output power is more than Boost_Level_1, the VBST is equal to ADP_MEDIUM_STEP. When PA output power is more than Boost_Level_2, the VBST is equal to BSTVOUT.

Speaker & Receiver 2 in 1 application

OCA72559FQAD built-in speaker and receiver 2-in-1 application mode, through the register settings, class D-type 2-in-1 receiver mode gain can be adjusted through the I2C register 0x05, adjustable range of 7.5~10.5dB. Speaker and Receiver signal use one signal path together, customers do not need extra component, so the system cost and PCB space are saved.

TDD noise suppression/ Radiation noise suppression

OCA72559FQAD features a unique conduction noise suppression circuit, making the power amplifier to maintain high PSRR value even in the input resistance, the input capacitance deviation of 10% or more, this greatly inhibits the generation of conducted noise.

Thermal AGC/ over temperature protection

Thermal AGC/ over temperature protection can automatically adjust the gain of the system, reduce the power consumption of the chip, to prevent damage in case of excessive temperature according to chip temperature. The OCA72559QAD has an automatic temperature detection mechanism, when the chip temperature exceeds the preset threshold of thermal AGC temperature (150°C), the chip will start the automatic gain control circuit to decrease the gain of the system, thereby reducing the energy consumption of the chip, thus slow or stop chip temperature continues to rise. When the chip temperature is restored to normal operating range (below 130°C), the automatic gain control circuit will restore the system gain to the original state. When the chip operates in a fault condition, the chip temperature is too high, up to a preset temperature protection temperature threshold (160°C), the system starts overheating protection, the chip will be turned off, restarts to resume normal work when the chip temperature returns to normal operating range (less than 130°C)

Automatic recovery of overcurrent protection

OCA72559FQAD with automatic recovery of the output overcurrent protection function, when the overcurrent occurs, OCA72559FQAD internal protection circuit will chip off to ensure that the chip is not damaged, when the short-circuit fault is eliminated, the chip will automatically resume working without restarting

■ Device Address

ADDR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADDR = L	1	0	1	1	0	0	0	R/W
ADDR = H	1	0	1	1	0	1	1	R/W
ADDR = SCL	1	0	1	1	0	0	1	R/W
ADDR = SDA	1	0	1	1	0	1	0	R/W

■ Register Map

ADDR	Register Name	Type	Reset Value	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
00H	Device ID	RO	0x09	0	0	0	0	1	0	0	1
01H	System Control	R/W	0x38	Reserved	CHIP_EN	CP_EN	BOOST_EN	PA_EN	REV_MODE_EN	Reserved	HVBAT_EN
02H	Battery Track	R/W	0x09	Reserved	Deglitch Time Setting		Battery Track Threshold		Battery Tracking EN	Battery Track Mode Output	
03H	BSTVOUT	R/W	0x0A	Reserved			BST_VOUT Setting				
04H	Not Used	R/W	0x09	Reserved							
05H	Boost Current Control	R/W	0x08	Reserved				BOOST_IPEAK			
06H	PA Setting	R/W	0x10	Reserved			Gain Setting				
07H	Slow AGC Output	R/W	0x83	Reserved			Slow AGC_ENN	Slow AGC Output Level			
08H	Slow AGC Control	R/W	0x4E	Slow AGC Release Time			Slow AGC Attack Time			Reserved	
09H	Fast AGC Output	R/W	0x03	Reserved				Fast AGC Output Level			
0AH	Fast AGC Control	R/W	0x08	Reserved			Fast AGC Attack Time			----	
0BH	Limiter Control	R/W	0x4A	Reserved					Limiter Attack Time		LIMITER_ENN
0CH	Adaptive Boost Control	R/W	0x03	Reserved				Limiter Attack control	Adaptive Mod Setting		
0DH	Adaptive Boost Timer	R/W	0x77	Boost Level 2 Duration time				Boost Level 1 Duration time			
0EH	Adaptive Boost Parameter	R/W	0x7A	Reserved							
0FH	Adaptive Boost Threshold	R/W	0x23	ADP_MEDIUM_STEP		BOOST_LEVEL 2 SETTING			BOOST_LEVEL 1 SETTING		

DEVICE ID

Address: 00h

Reset Value: 8'b 0000_1001

Type: Read

Bits	Name	Size	Description
[7:6]	Vendor ID	2	Vendor ID
[5:3]	Version ID	3	Device Version ID
[2:0]	Revision ID	3	Revision History ID

System Control

Address: 01h

Reset Value: 8'b 0011_1000

Type: Read/Write

Bits	Name	Size	Description
7	Reserved	1	Do Not Use
6	CHIP_EN	1	Chip Enable/Disable

			0: Chip Disable
			1: Chip Enable
5	CP_EN	1	Charge Pump Enable/Disable
			0: Charge pump Disable
			1: Charge pump Enable
4	BOOST_EN	1	Boost Enable/Disable
			0: Boost Disable
			1: Boost Enable
3	PA_EN	1	PA Enable/Disable
			0: PA Disable
			1: PA Enable
2	RCV_MODE_EN	1	Receiver Mode Enable/Disable
			0: Receiver Mode Disable
			1: Receiver Mode Enable
1	Reserved	1	Do Not Use
0	HVBAT_EN	1	High Voltage Battery Mode Enable/Disable
			0: High Voltage Battery Mode Disable
			1: High Voltage Battery Mode Enable

Battery Track

Address: 02h

Reset Value: 8'b 0000_1001

Type: Read/Write

Bits	Name	Size	Description
7	Reserved	1	Do Not Use
[6:5]	Deglitch Time Setting	2	Deglitch Time
			00: 1mS
			01: 500μS
			10: 200μS
			11: No Deglitch setting
[4:3]	Battery Track Threshold	2	Battery Track Threshold Voltage:
			00: 3.3V
			01: 3.4V
			10: 3.5V
			11: 3.6V
2	Battery Track EN	1	Battery Track Enable/Disable
			0: Battery Track Disable
			1: Battery Track Enable
[1:0]	Battery Track Mode Output	2	Battery Track Output Voltage:
			00: 5V
			01: 5.5V
			10: 6V
			11: 6.5V

BSTVOUT

Address: 03h

Reset Value: 8'b 0000_1010

Type: Read/Write

Bits	Name	Size	Description
[7:5]	Reserved	3	Do Not Use
[4:0]	BST_VOUT	5	Boost Output Voltage
			00000: 6.5V
			00001: 6.75V
			00010: 7.0V
			00011: 7.25V
			00100: 7.5V
			00101: 7.75V
			00110: 8.0V
			00111: 8.25V
			01000: 8.5V
			01001: 8.75V
			01010: 9.0V
			01011: 9.25V
			01100: 9.5V
			01101: 9.75V
			01110: 10.0V
			01111: 10.25V
			10000: 10.5V

Boost Parameter

Address: 04h

Reset Value: 8'b 0000_1001

Type: Read/Write

Bits	Name	Size	Description
[7:0]	Reserved	8	Do Not Use

Boost Current Control

Address: 05h

Reset Value: 8'b 0000_1000

Type: Read/Write

Bits	Name	Size	Description
[7:4]	Reserved	4	Do Not Use
[3:0]	BST_IPEAK	4	Boost Peak Current Limit
			0010: 2A

			0011: 2.25A
			0100: 2.5A
			0101: 2.75A
			0110: 3A
			0111: 3.25A
			1000: 3.5A
			1001: 3.75A
			1010: 4A
			1011: 4.25A
			1100: 4.5A

PA Setting

Address: 06h

Reset Value: 8'b 0001_0000

Type: Read/Write

Bits	Name	Size	Description
[7:5]	Reserved	3	Do Not Use
[4:0]	Gain Setting (RCV_MODE_EN=1, valid value: 00000~00111; RCV_MODE_EN=0, valid value: 01000~10010)	5	PA Gain Setting
			00000: 0dB
			00001: 1.5dB
			00010: 3dB
			00011: 4.5dB
			00100: 6dB
			00101: 7.5dB
			00110: 9dB
			00111: 10.5dB
			01000: 12dB
			01001: 13.5dB
			01010: 15dB
			01011: 16.5dB
			01100: 18dB
			01101: 19.5dB
			01110: 21dB
			01111: 22.5dB
			10000: 24dB
			10001: 25.5dB
			10010: 27dB

Slow AGC Output

Address: 07h

Reset Value: 8'b 0100_0011

Type: Read/Write

Bits	Name	Size	Description	
[7:5]	Reserved	3	Do Not Use	
4	Slow AGC_ENN	1	Slow AGC Enable/Disable	
			0: Enable	
			1: Disable	
[3:0]	Slow AGC Output Level	4	Slow AGC Output Level	
			0000: 0.5W@8ohm	0000: 0.67W@6ohm
			0001: 0.6W@8ohm	0001: 0.8W@6ohm
			0010: 0.7W@8ohm	0010: 0.93W@6ohm
			0011: 0.8W@8ohm	0011: 1.07W@6ohm
			0100: 0.9W@8ohm	0100: 1.20W@6ohm
			0101: 1.0W@8ohm	0101: 1.33W@6ohm
			0110: 1.1W@8ohm	0110: 1.47W@6ohm
			0111: 1.2W@8ohm	0111: 1.6W@6ohm
			1000: 1.3W@8ohm	1000: 1.73W@6ohm
			1001: 1.4W@8ohm	1001: 1.87W@6ohm
			1010: 1.5W@8ohm	1010: 2.0W@6ohm
			1011: 1.6W@8ohm	1011: 2.13W@6ohm
			1100: 1.7W@8ohm	1100: 2.27W@6ohm
			1101: 1.8W@8ohm	1101: 2.4W@6ohm
			1110: 1.9W@8ohm	1110: 2.53W@6ohm
			1111: 2.0W@8ohm	1111: 2.67W@6ohm

Slow AGC Control

Address: 08h

Reset Value: 8'b 0100_1110

Type: Read/Write

Bits	Name	Size	Description
[7:5]	Slow AGC Release Time	3	000: 5.12mS/dB
			001: 10.24mS/dB
			010: 20.48mS/dB
			011: 40.96mS/dB
			100: 81.92mS/dB
			101: 163.84mS/dB
			110: 327.68mS/dB
			111: 655.36mS/dB
[4:2]	Slow AGC Attack Time	3	000: 1.28mS/dB
			001: 2.56mS/dB
			010: 10.24mS/dB
			011: 40.96mS/dB
			100: 81.92mS/dB
			101: 163.84mS/dB
			110: 327.68mS/dB

			111: 655.36mS/dB
[1:0]	Reserved	2	Do Not Use

Fast AGC Output

Address: 09h

Reset Value: 8'b 0000_0011

Type: Read/Write

Bits	Name	Size	Description	
[7:4]	Reserved	4	Do Not Use	
[3:0]	Fast AGC Output Level	4	0000: 1.0W@8ohm	0000: 1.33W@6ohm
			0001: 1.2W@8ohm	0001: 1.60W@6ohm
			0010: 1.4W@8ohm	0010: 1.87W@6ohm
			0011: 1.6W@8ohm	0011: 2.13W@6ohm
			0100: 1.8W@8ohm	0100: 2.40W@6ohm
			0101: 2.0W@8ohm	0101: 2.67W@6ohm
			0110: 2.2W@8ohm	0110: 2.93W@6ohm
			0111: 2.4W@8ohm	0111: 3.2W@6ohm
			1000: 2.6W@8ohm	1000: 3.47W@6ohm
			1001: 2.8W@8ohm	1001: 3.73W@6ohm
			1010: 3.0W@8ohm	1010: 4.0W@6ohm
			1011: Fast AGC Off	1011: Fast AGC Off

Fast AGC Control

Address: 0Ah

Reset Value: 8'b 0000_1000

Type: Read/Write

Bits	Name	Size	Description
[7:5]	Reserved	3	Do Not Use
[4:2]	Fast AGC Attack Time	3	000: 0.16mS/dB
			001: 0.32mS/dB
			010: 0.64mS/dB
			011: 2.56mS/dB
			100: 10.24mS/dB
			101: 40.96mS/dB
			110: 82mS/dB
			111: 164mS/dB
[1:0]	Reserved	2	Do Not Use

Limiter Control

Address: 0Bh

Reset Value: 8'b 0100_1010

Type: Read/Write

Bits	Name	Size	Description	
[7:3]	Reserved	5	Do Not Use	
[2:1]	Limiter Attack Time	2	0x0C [3] =0	0x0C [3] =1
			00: 0.04mS/dB	00: 0.02mS/dB
			01: 0.08mS/dB	01: 0.01mS/dB
			10: 0.16mS/dB	10: 0.005mS/dB
			11: 0.32mS/dB	11: 0.003mS/dB
0	LIMITER_ENN	1	Limiter Enable/Disable	
			0: Enable	
			1: Disable	

Adaptive Boost Control

Address: 0Ch

Reset Value: 8'b 0000_0011

Type: Read/Write

Bits	Name	Size	Description
[7:4]	Reserved	4	Do Not Use
3	Limiter Attack control	1	Limiter Attack control
			0: Normal Limiter Attack
			1: Faster Limiter Attack
[2:0]	Adaptive Mode Setting	3	000: Direct Pass, VBST=VDD
			001: Normal Boost Mode
			010: ADP BOOST MOD1
			011: ADP BOOST MOD2

Adaptive Boost Timer

Address: 0Dh

Reset Value: 8'b 0111_0111

Type: Read/Write

Bits	Name	Size	Description
[7:4]	Boost Level 2 Duration time	4	0000: 1.25mS
			0001: 2.5mS
			0010: 5mS
			0011: 10mS
			0100: 15mS
			0101: 20mS
			0110: 30mS
			0111: 40mS
			1000: 65mS
			1001: 80mS
			1010: 100mS

			1011: 120mS
			1100: 140mS
			1101: 160mS
			1110: 320mS
			1111: 480mS
[3:0]	Boost Level 1 Duration time	4	0000: 1.25mS
			0001: 2.5mS
			0010: 5mS
			0011: 10mS
			0100: 15mS
			0101: 20mS
			0110: 30mS
			0111: 40mS
			1000: 65mS
			1001: 80mS
			1010: 100mS
			1011: 120mS
			1100: 140mS
			1101: 160mS
			1110: 320mS
			1111: 480mS

Adaptive Boost Parameter

Address: 0Eh

Reset Value: 8'b 0111_1010

Type: Read/Write

Bits	Name	Size	Description
[7:0]	Reserved	8	Not used

Adaptive Boost Threshold

Address: 0Fh

Reset Value: 8'b 0010_0011

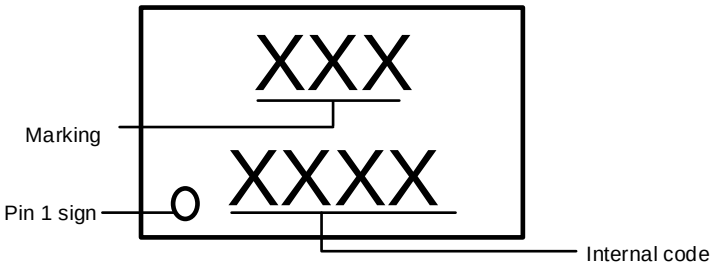
Type: Read/Write

Bits	Name	Size	Description
[7:6]	ADP_MEDIUM_STEP	2	00: ADP Medium Step Voltage=6.5V
			01: ADP Medium Step Voltage=6.75V
			10: ADP Medium Step Voltage=7.0V
			11: ADP Medium Step Voltage=7.25V
[5:3]	BOOST_LEVEL 2 SETTING	3	000: 1.2W
			001: 1.4W
			010: 1.6W
			011: 1.8W

			100: 2.0W
			101: 2.2W
			110: Reserved
			111: Reserved
[2:0]	BOOST_LEVEL 1 SETTING	3	000: 0.1W
			001: 0.2W
			010: 0.3W
			011: 0.4W
			100: 0.5W
			101: Reserved
			110: Reserved
			111: Reserved

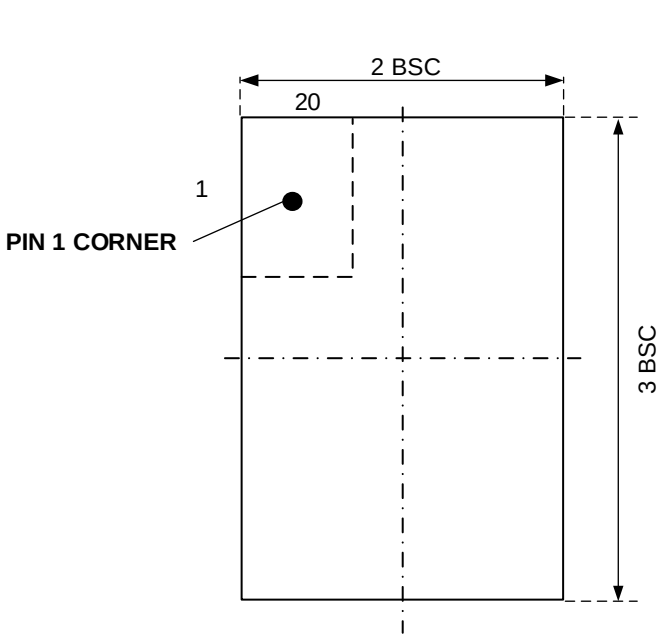
■ Marking Information

FC-QFN2030-20L

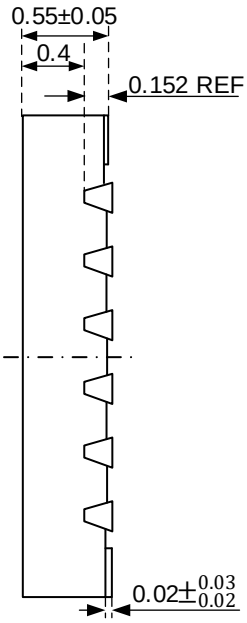


■ Package Information

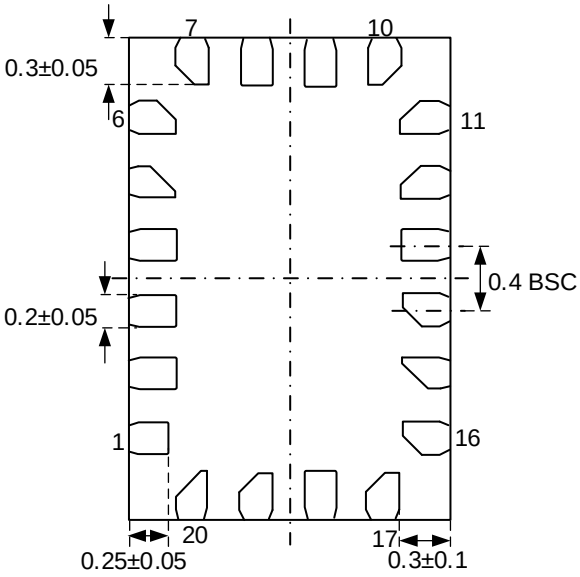
FC-QFN2030-20L



TOP VIEW



SIDE VIEW

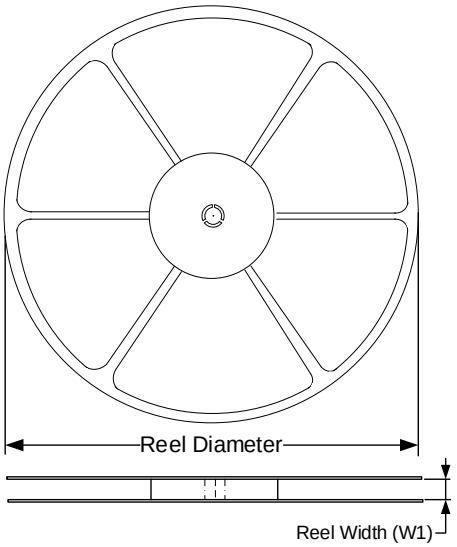


BOTTOM VIEW

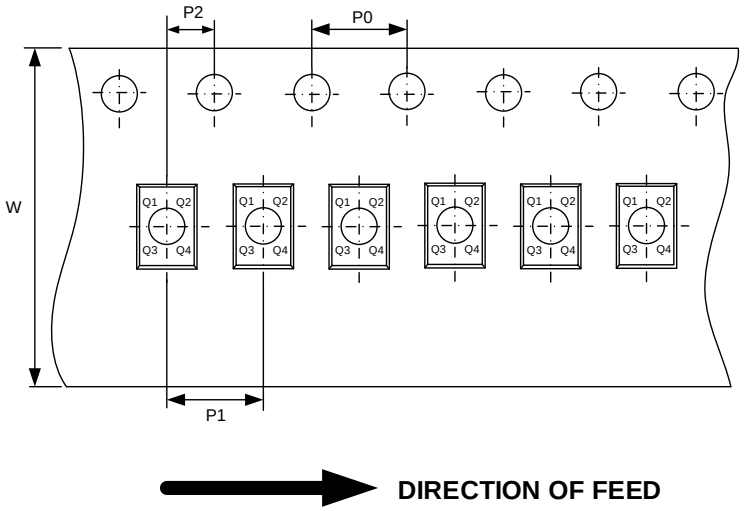
Note: All dimensions are in millimeters.

■ Packing Information

REEL DIMENSIONS



TAPE DIMENSIONS



Package Type	SPQ (PCS)	Reel Diameter (mm)	Reel Width W1(mm)	W (mm)	P0 (mm)	P1 (mm)	P2 (mm)	MSL	PIN 1 Quadrant
FC-QFN2030-20L	3000	180	9.5	12	4.0	4.0	2.0	Level-3	Q1

IMPORTANT NOTICE

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