

N- and P-Channel 20V (D-S) MOSFET

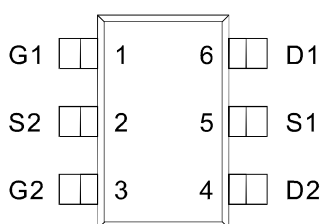
GENERAL DESCRIPTION

The ME3587 is the N- and P-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where low in-line power loss are needed in a very small outline surface mount package.

PIN CONFIGURATION

(TSOP-6)

Top View



Ordering Information: ME3587 (Pb-free)

ME3587-G

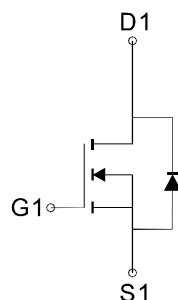
(Green product-Halogen free)

FEATURES

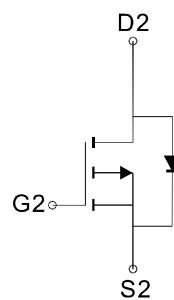
- $R_{DS(ON)} \leq 45m\Omega @ V_{GS}=4.5V$ (N-Ch)
- $R_{DS(ON)} \leq 68m\Omega @ V_{GS}=2.5V$ (N-Ch)
- $R_{DS(ON)} \leq 120m\Omega @ V_{GS}=1.8V$ (N-Ch)
- $R_{DS(ON)} \leq 110m\Omega @ V_{GS}=-4.5V$ (P-Ch)
- $R_{DS(ON)} \leq 130m\Omega @ V_{GS}=-2.5V$ (P-Ch)
- $R_{DS(ON)} \leq 170m\Omega @ V_{GS}=-1.8V$ (P-Ch)
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- Load Switch
- DSC
- LCD Display inverter



N-Channel MOSFET



P-Channel MOSFET

Absolute Maximum Ratings (TA=25°C Unless Otherwise Noted)

Parameter	Symbol	N-channel Maximum Ratings	P-channel Maximum Ratings	Unit
Drain-Source Voltage	V_{DS}	20	-20	V
Gate-Source Voltage	V_{GS}	± 8	± 8	V
Continuous Drain Current *	I_D	$T_A=25^\circ C$ 4.6	-3.1	A
		$T_A=70^\circ C$ 3.2	-2.5	
Pulsed Drain Current	I_{DM}	16	-10	A
Maximum Power Dissipation	P_D	$T_A=25^\circ C$ 1.18	1.18	W
		$T_A=70^\circ C$ 0.7	0.7	
Operating Junction Temperature	T_J	-55 to 150	-55 to 150	$^\circ C$
Thermal Resistance-Junction to Ambient*	$R_{\theta JA}$	150	175	$^\circ C/W$

* The device mounted on 1in² FR4 board with 2 oz copper

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N-Channel Mosfet Electrical Characteristics (TA =25°C Unless Otherwise Specified)

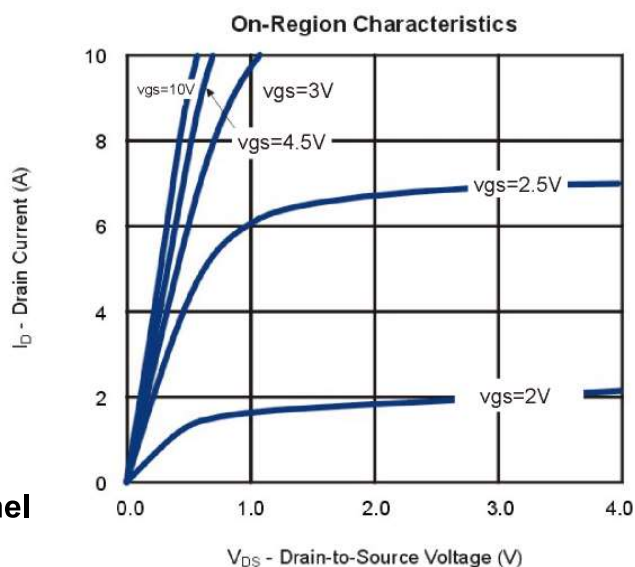
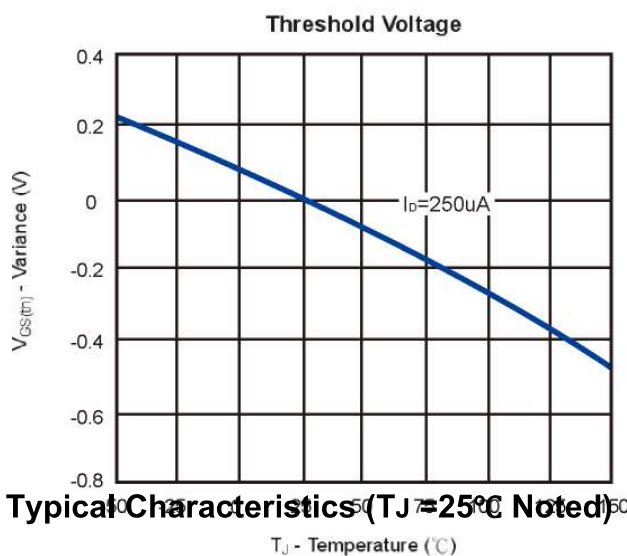
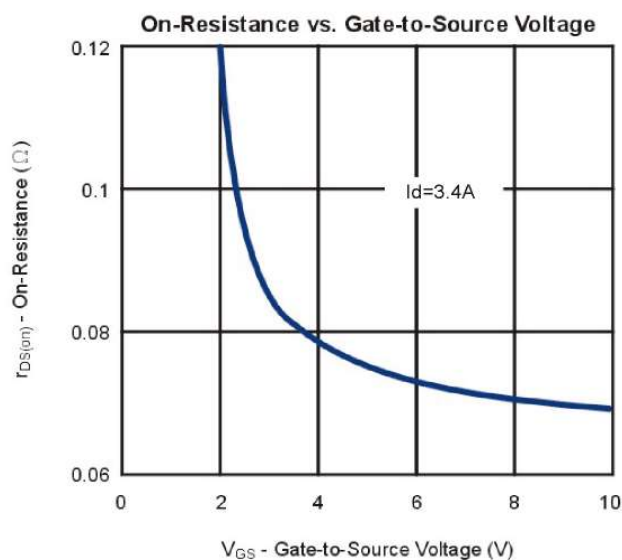
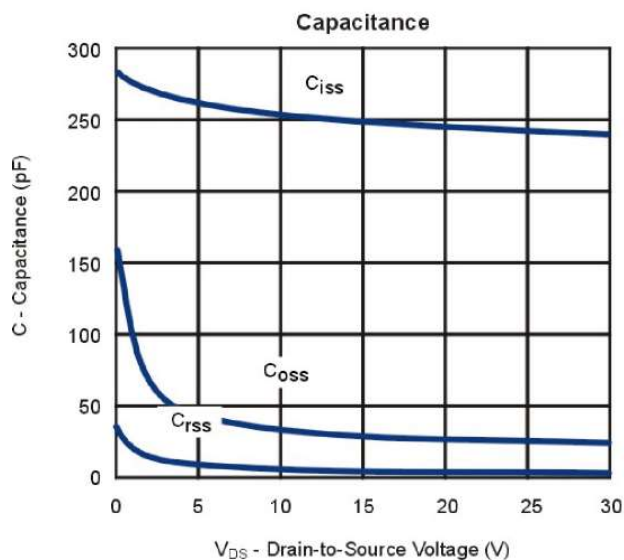
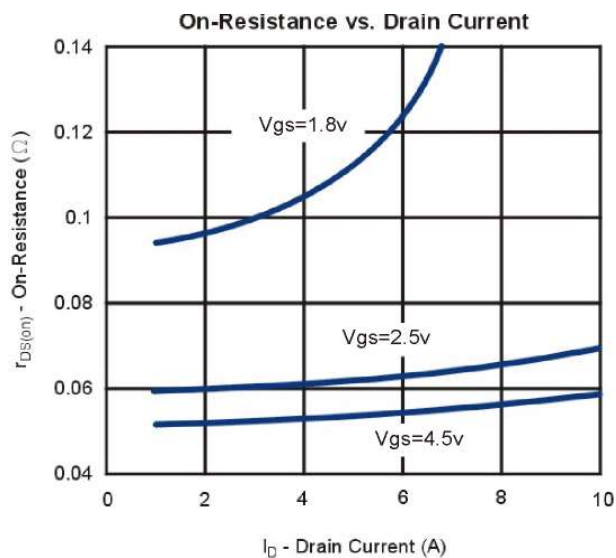
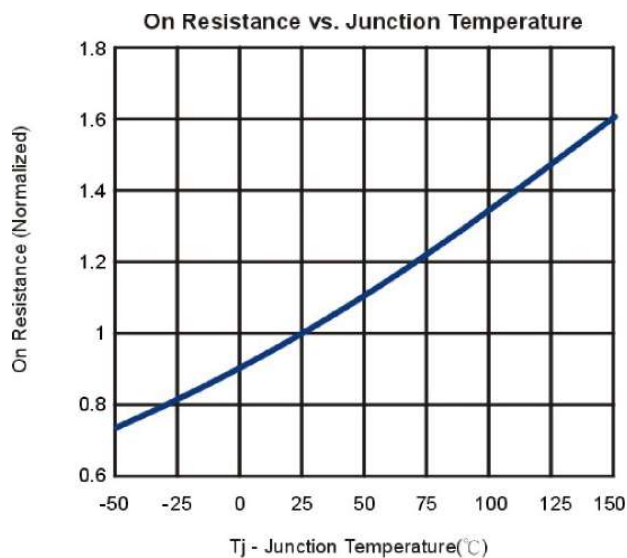
Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	20			V
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	0.5		1.2	V
I_{GSS}	Gate Leakage Current	$V_{DS}=0V, V_{GS}=\pm 8V$			± 100	nA
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=20V, V_{GS}=0V$			1	μA
$R_{DS(on)}$	Drain-Source On-Resistance ^a	$V_{GS}=4.5V, I_D= 3.4A$		37	45	m Ω
		$V_{GS}=2.5V, I_D= 3A$		52	68	
		$V_{GS}=1.8V, I_D= 2A$		92	120	
V_{SD}	Diode Forward Voltage	$I_S=1A, V_{GS}=0V$		0.7		V
DYNAMIC						
Q_g	Total Gate Charge	$V_{DS}=15V, V_{GS}=4.5V, I_D=3.4A$		4.4		nC
Q_{gs}	Gate-Source Charge			1.6		
Q_{gd}	Gate-Drain Charge			0.8		
R_g	Gate resistance	$V_{DS}=0V, V_{GS}=0V, f=1MHz$		1.2		Ω
C_{iss}	Input Capacitance	$V_{DS}=15V, V_{GS}=0V, f=1MHz$		340		pF
C_{oss}	Output Capacitance			50		
C_{rss}	Reverse Transfer Capacitance			15		
$t_{d(on)}$	Turn-On Delay Time	$V_{DS}=10V, R_L=10\Omega$ $R_{GEN}=3\Omega, V_{GS}=5V$		11		ns
t_r	Turn-On Rise Time			17		
$t_{d(off)}$	Turn-Off Delay Time			30		
t_f	Turn-Off Fall time			3		

Notes: a. Pulse test; pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$

b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.

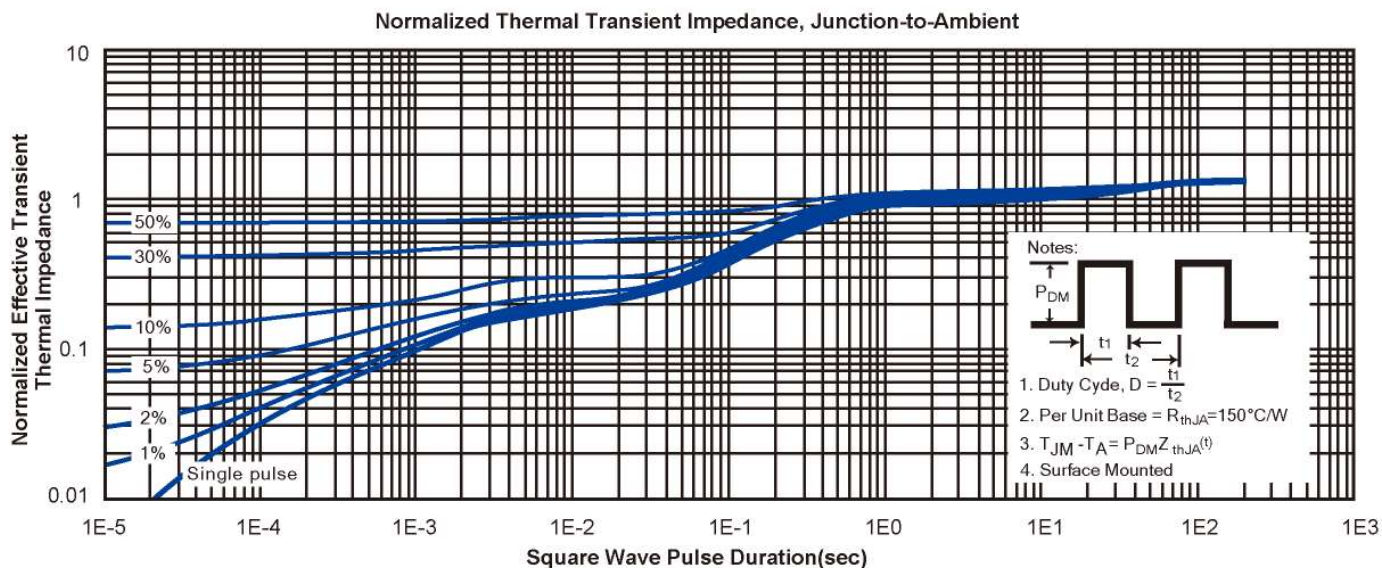
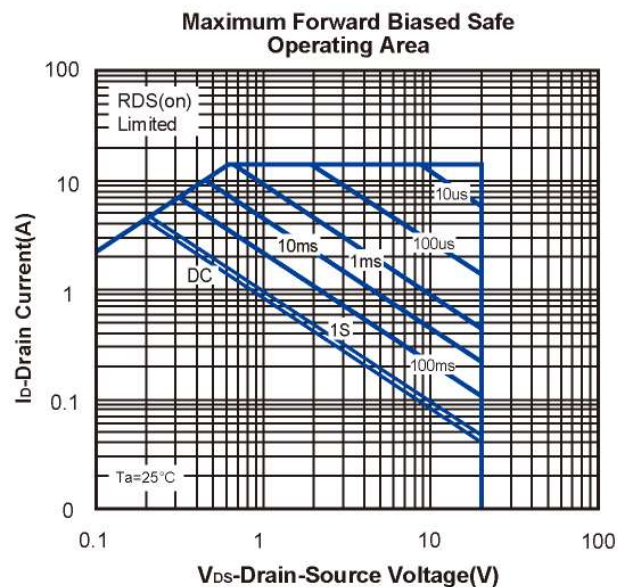
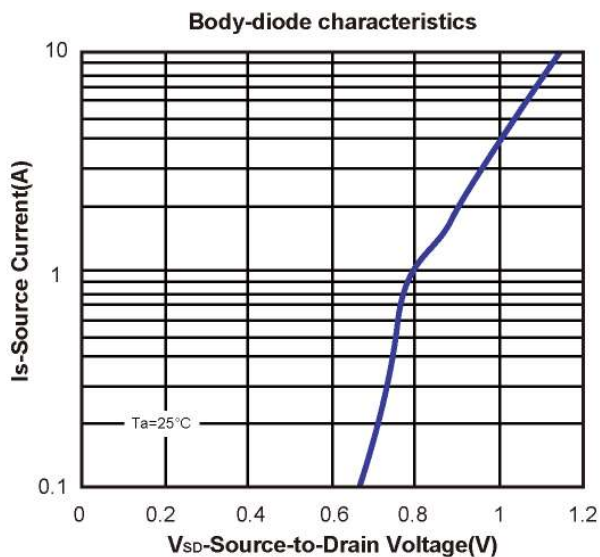
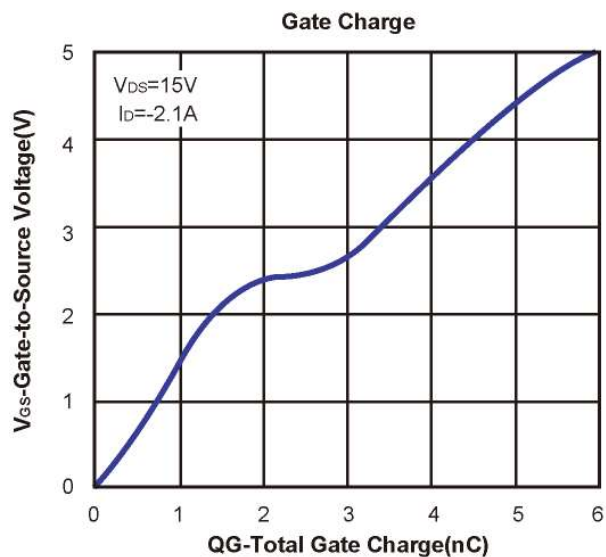
Typical Characteristics (TJ =25°C Noted) N-Channel

N- and P-Channel 20V (D-S) MOSFET



Typical Characteristics (Tj = 25°C Noted) N-Channel

N- and P-Channel 20V (D-S) MOSFET



N- and P-Channel 20V (D-S) MOSFET

P-Channel Electrical Characteristics (T_A =25°C Unless Otherwise Specified)

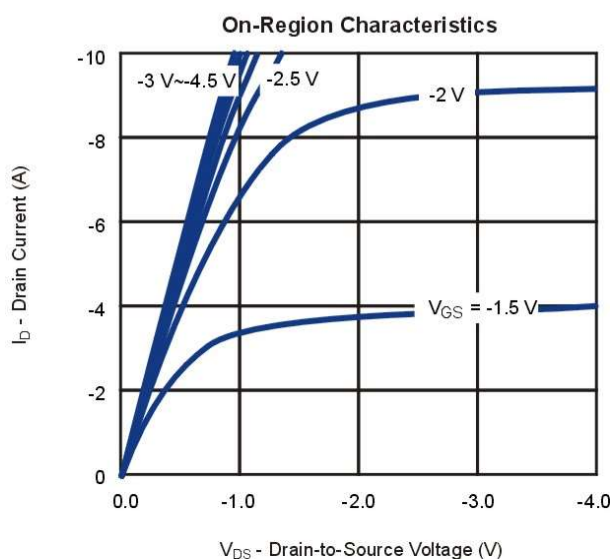
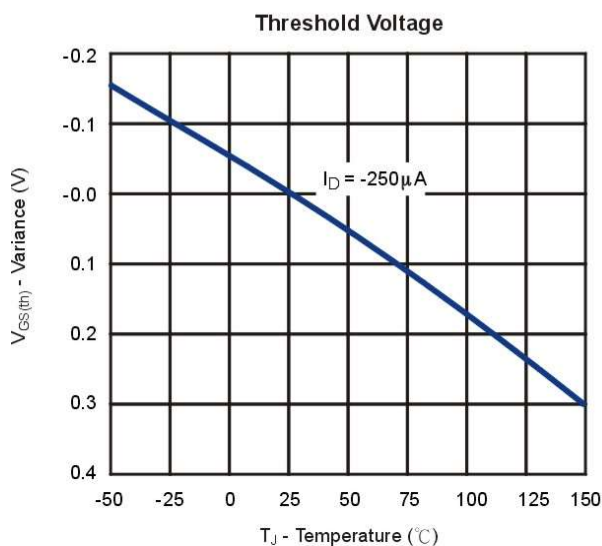
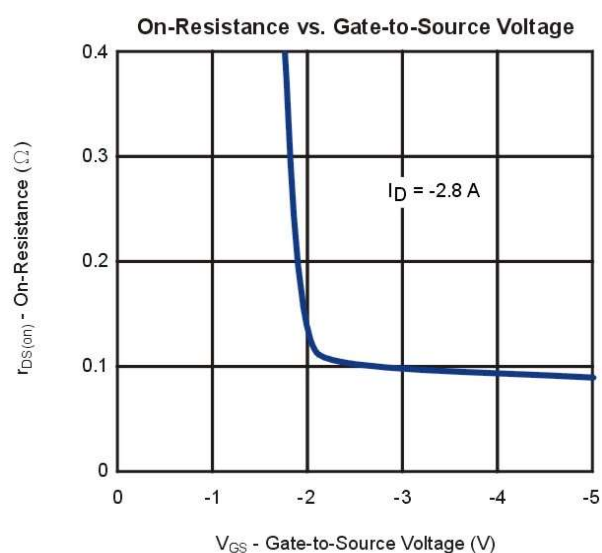
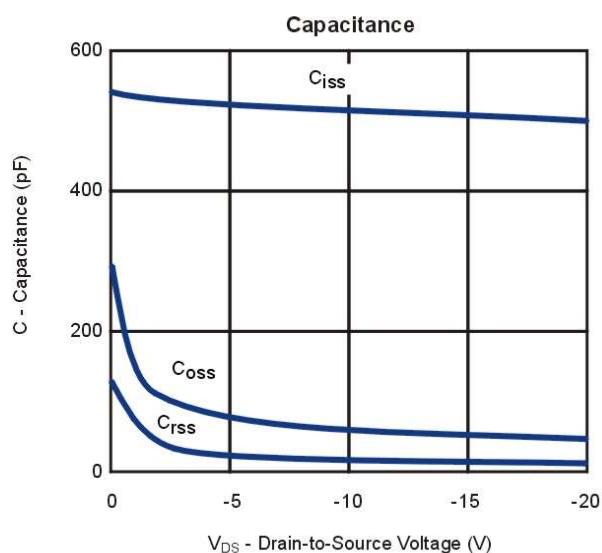
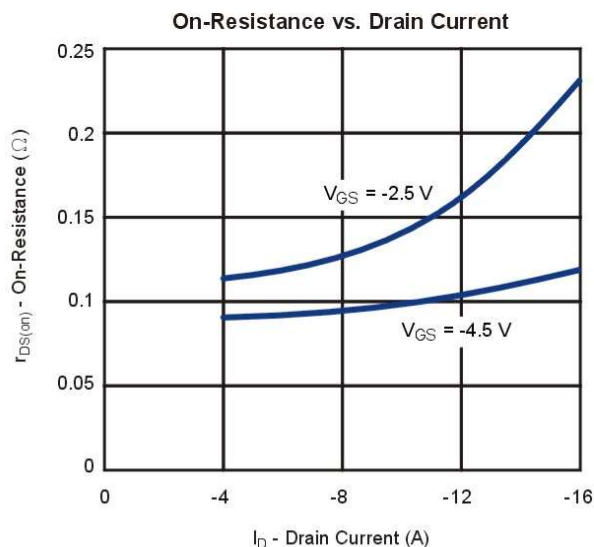
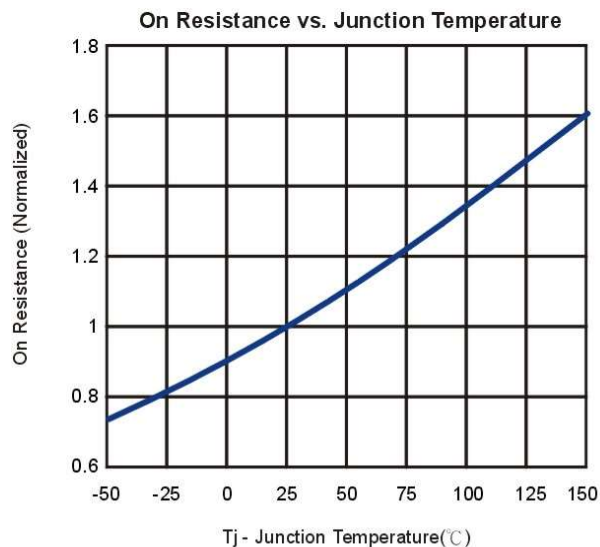
Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =-250μA	-20			V
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =-250μA	-0.4		-1	V
I _{GSS}	Gate Leakage Current	V _{DS} =0V, V _{GS} =±8V			±100	nA
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =-20V, V _{GS} =0V			-1	μA
R _{DS(ON)}	Drain-Source On-Resistance ^a	V _{GS} =-4.5V, I _D = -2.8A		85	110	mΩ
		V _{GS} =-2.5V, I _D = -2A		110	130	
		V _{GS} =-1.8V, I _D = -1A		130	170	
V _{SD}	Diode Forward Voltage	I _S =-1A, V _{GS} =0V		-0.7	-1.4	V
DYNAMIC						
Q _g	Total Gate Charge	V _{DS} =-15V, V _{GS} =-4.5V, I _D =-2.8A		5		nC
Q _{gs}	Gate-Source Charge			1.5		
Q _{gd}	Gate-Drain Charge			0.9		
C _{iss}	Input Capacitance	V _{DS} =-15V, V _{GS} =0V, f=1MHz		480		pF
C _{oss}	Output Capacitance			46		
C _{rss}	Reverse Transfer Capacitance			10		
t _{d(on)}	Turn-On Delay Time	V _{DS} =-6V, R _L =6Ω R _{GEN} =6Ω, V _{GS} =-4.5V		50		ns
t _r	Turn-On Rise Time			30		
t _{d(off)}	Turn-Off Delay Time			40		
t _f	Turn-Off Fall time			11		

Notes: a. Pulse test; pulse width ≤ 300us, duty cycle ≤ 2%

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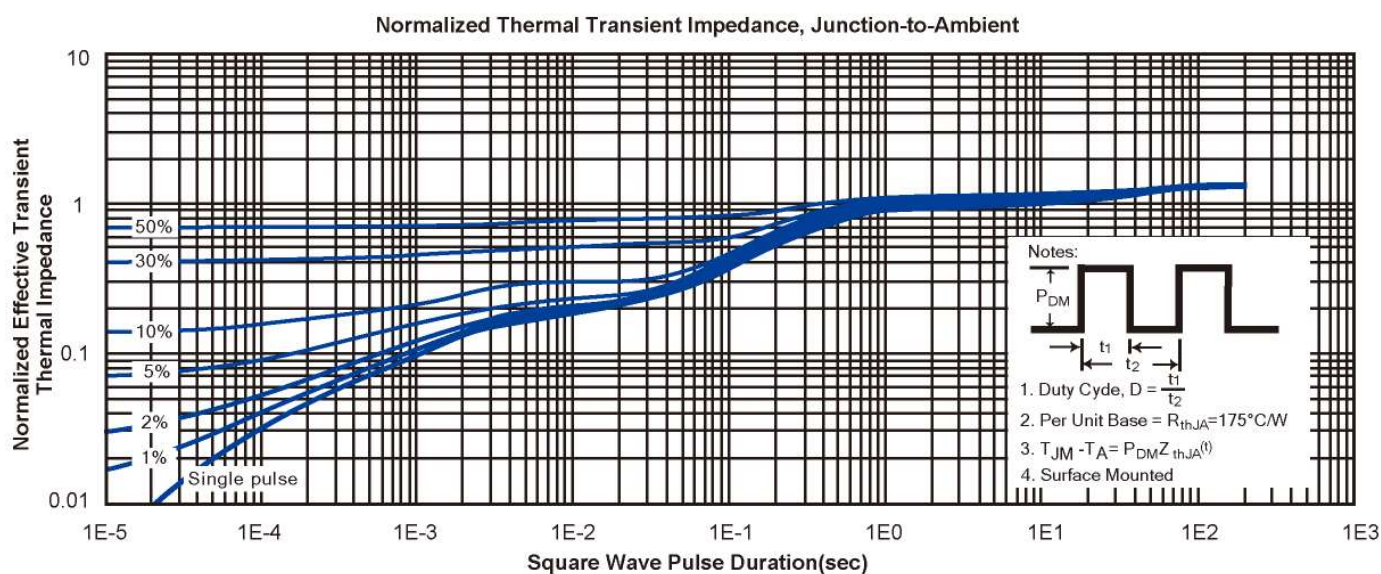
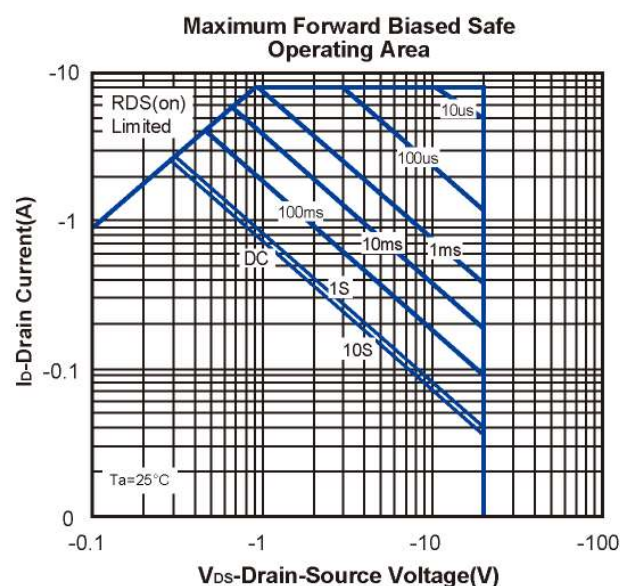
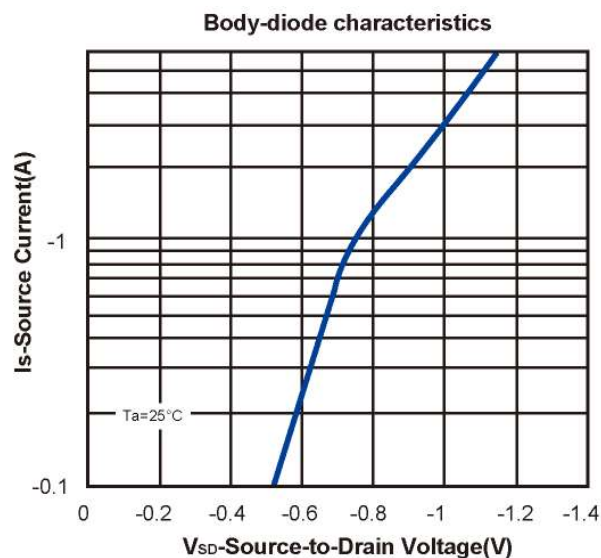
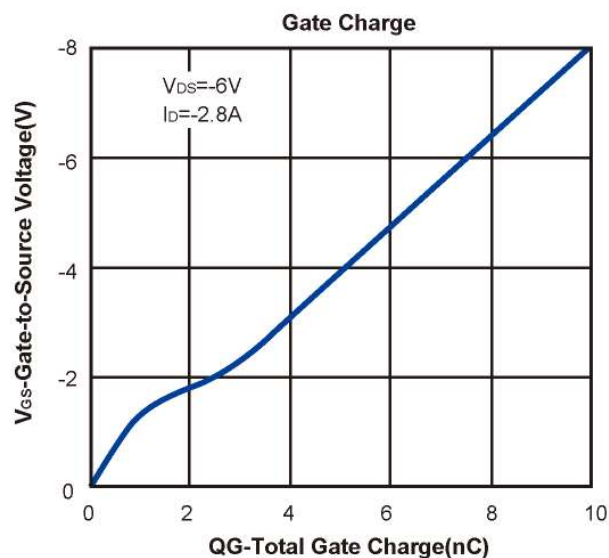
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Typical Characteristics (T_J = 25°C Noted) P-Channel

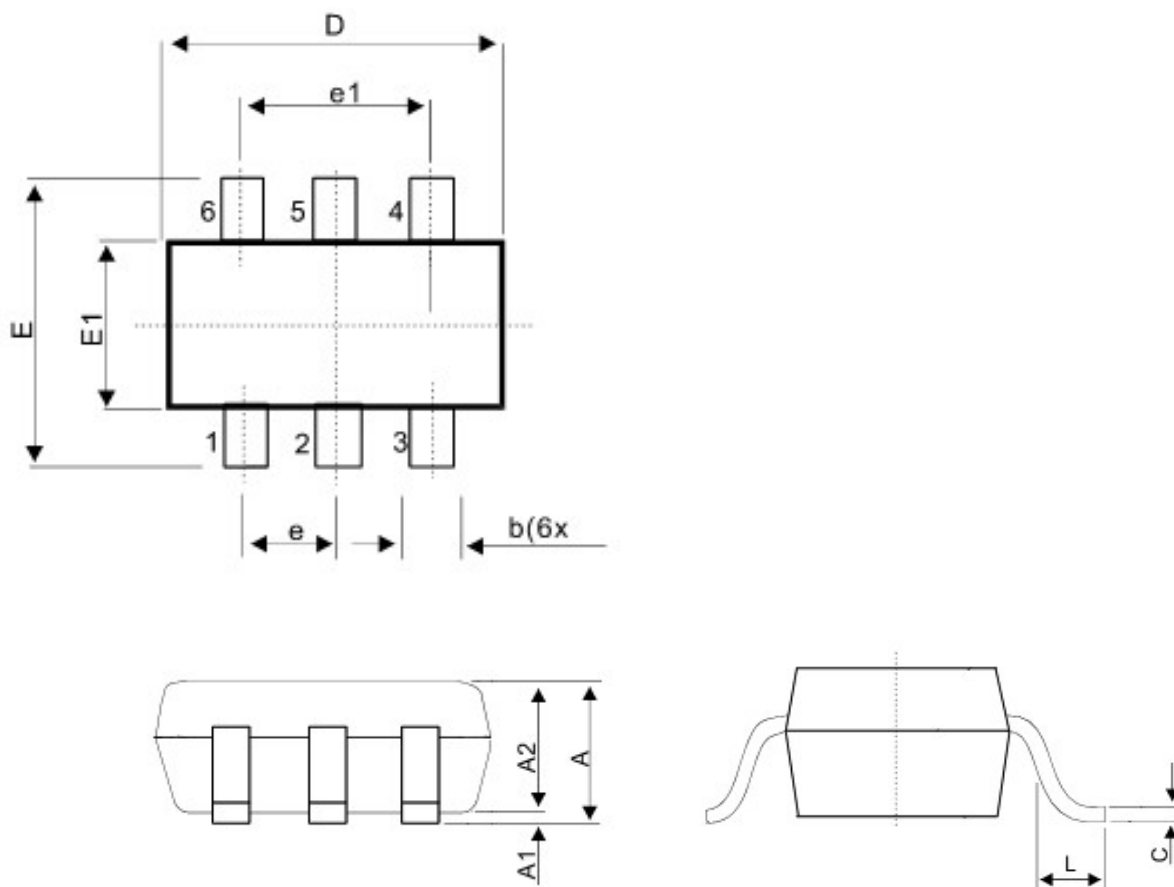


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Typical Characteristics (T_J =25°C Noted) P-Channel



TSOP-6 Package Outline



SYMBOL	MILLIMETERS (mm)	
	MIN	MAX
A	0.90	1.20
A1	0.01	0.10
A2	0.90	1.15
b	0.25	0.50
C	0.10	0.20
D	2.80	3.10
E	2.60	3.00
E1	1.50	1.70
e	0.95 BSC	
e1	1.90 BSC	
L	0.30	0.60