DATASHEET

TW5866

9D1 H.264 CODEC with 8-Channel A/V Decoder

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TW5866 is a H.264 CODEC solution with integrated 8-channel analog A/V decoders. TW5866 supports up to 9D1 of H.264 video encoding, 8D1 of H.264 video decoding, or 4D1 H.264 full duplex codec. In addition, TW5866 supports motion JPEG encoding and video preview through BT.656 interfaces and PCI interfaces. TW5866 can be used in low cost H.264 hardware compression PCI card to support either 8-channel with a single chip, or 16-channel with two chips. It can also work with two external TW2866 to support 16-CIF H.264 compression. TW5866 can also be used in embedded DVR applications as an AV front-end chip working with display mux capable SOCs.

TW5866 integrates 8 A/V decoders. It takes 8 CVBS analog inputs fed into eight internal high quality NTSC/PAL video decoders. In addition, it has 2 digital BT.656 / 1120 interfaces, running up to 108/148.5 MHz, capable of receiving up to 8 D1, 2 720P / 1080i / 1080p HD video sources. When used as D1 input, the digital interface takes multi-channel video signal from external video decoders, such as TW2866 / TW2867. This allows the TW5866 to support a total of 16 D1 video channels. All the SD / HD video streams are fed into H.264 encoder, MJPEG encoder for compression, and to PCI interface and digital 656 output interface for preview purposes. The H.264 decoded stream from the on-chip video decoder is fed through two BT.656 / 1120 playback interfaces to drive the external display processors. The BT.656 playback interfaces runs up to 108 MHz and is capable of delivering multi-channel byte-interleaving or field/frame interleaving format for total of 8 D1 playback channels.

TW5866 supports functions per channel, such as motion detection, night detection, and blind detection engine for channel alarm notification. It features triple scalers per channel for each of the H.264 encode, MJPEG, and PCI preview paths. Each of these scalers is independently configurable. TW5866 also features per channel OSDs and motion adaptive de-interlacer. TW5866 supports 8-channel of motion adaptive 2D de-interlacers and 2D noise reduction.

TW5866 integrates a H.264 baseline level 3 compliant encoder capable of performing up to either 9 D1 equivalent video encoding (225 fps for PAL and 270 fps for NTSC), 8 D1 decoding, 17 channel G.726 ADPCM hardware audio encoder with one channel for two way audio communication, and one channel ADPCM audio decoding. The H.264 video encoder supports dual-bitstream compression for both local storage and network streams. It also features a motion JPEG encoder for up to 25 frames per second shared among all video channels.

TW5866 provides PCI interface for external CPU control and bitstream upload. The PCI interface runs at 33 or 66 MHz The external CPU can access the internal meta-data associated with each H.264 channel for video analytic purposes.

Analog Video Decoder

- 8 CVBS analog inputs fed into 8 sets of video decoder accept all NTSC(M/N/4.43) / PAL (B/D/G/H/I/K/L/M/N/60) standards with auto detection
- Integrated video analog anti-aliasing filters and 10-bit CMOS ADCs for each video decoder
- High performance adaptive 4H comb filters for all NTSC/PAL standards
- IF compensation filter for improvement of color demodulation
- Color Transient Improvement (CTI)
- Automatic white peak control
- Programmable hue, saturation, contrast, brightness and sharpness
- Proprietary fast video locking system for non-real-time application
- Noise Reduction to remove impulse noise

Digital Input Ports

- BT.656
  - Two BT.656 ports at up to 108 MHz interfaced with 2 external TW2866s
  - Byte-interleaving supports 4 channels multiplexing with each channel of interlaced D1 at 60/50 fps
- BT.1120
  - Two BT.1120 ports to support external HD video sources of 720P / 1080i / 1080p format at 74.25 / 148.5 MHz
  - One cascade input supporting cascade of multiple TW5866 chips. This is pin shared with one playback port

Pre-processing

- Per channel triple high performance down scalers of each channel scale independently for H.264, JPEG and preview output
- Per channel motion detector with 16 X 12 cells
- Per channel night / blind detections
- Per channel noise reduction and de-interlacing to convert Interlaced video into progressive before compression
- Per channel OSD for information overlay
  - Single Box
  - 1-bit per pixel text

– 2-bit per pixel text or mask
– 12-bit per pixel bitmap

Digital Preview Ports

- Two BT.656 ports provides preview raw video output to external display processors
- Byte-Interleaving interlaced D1 for each port at 27 / 54 / 108 MHz

Digital Playback Ports

- Playback video for external display chips
- Two BT.656 ports for multi-channel 8 D1 playback
  – BT.656 Byte-Interleaving at 27 / 54 / 108 MHz
  – BT.656 Frame / Field Interleaving w/ D1 / Quad CIF resolution at 27 / 54 / 108 MHz
- Two BT.1120 port for single channel 1440x960 / 1440x1152 / 720p / 1080i playback

H.264 Video Encoder

- H.264 baseline profile @ level 3 encoding
- Bit rate from 64 kbps up to 10 Mbps each channel
- Maximum 225 fps (PAL) or 270 fps (NTSC) H.264 encoding
- Full duplex codec with real-time 4 D1 / 16 CIF or non-real-time 8 D1 main stream encoding
- Real-time 4 CIF / 16 QCIF or non-real-time 16 CIF secondary stream encoding
- VBR / CBR controllable
- Configurable GOP interval
- Motion vector granularity at full pel, ½ pel, and ¼ pel
- Motion vector ranges [-256, +255.75]
- In-loop de-blocking filter
- CAVLC entropy coding

H.264 Video Decoder

- H.264 baseline decoder for decoding the bit-stream generated by TW5866 / TW5864 encoders
- Bit rate from 64 kbps up to 10 Mbps each channel
- Maximum 200 fps (PAL) or 240 fps (NTSC)
- Full duplex codec with Real-time 4 D1 or non-real-time 8 D1 stream decoding
- Playback control with normal play, fast forward, slow forward and fast reverse.

Video Analytic Interface

- Per MB type / motion meta-data information
- 16x12 cells motion detection information
- Accessible through PCI / Async Host Interface

Motion JPEG Encoder

- Maximum of 25 fps, shared among all channels
- Support picture sizes of D1, CIF, and half-D1

Analog Audio CODEC

- Integrated five audio ADCs and one audio DAC providing multi-channel audio mixed analog output
- Supports a standard I2S interface for multi-channel audio mux output to external audio playback processor, such as TW2880
- PCM 8/16-bit and u-Law/A-Law 8 -bit for audio word length
- Programmable audio sample rate that covers popular frequencies of 8/16/32/44.1/48kHz

Digital Audio CODEC

- Hardware G.726 ADPCM encoder / decoder
- Encodes maximum of 17 channels, with 1 channel for two way communication
- Decodes 1 channel of audio for playback
- RTC for AV sync

DDR2 Interface

- One 16-bit or two 8-bit external DDR2 SDRAM memories running at up to 333 MHz
- Total 256 MB up to 2 GB
- Auto refresh

Host Interface

- Configurable 32-bit asynchronous host interface / PCI interface
- PCI Interface runs as both initiator and target at 33 / 66 MHz
- Preview video through PCI (33 MHz) supporting resolution such as:
  – 2 D1
  – 1 D1 + 4 CIF
  – 9 CIF
  – 16 QCIF
  – 1 D1 + 15 QCIF
- I²C Interface for external Video Decoder chips configuration
- IRQs and GPIOs

System Clock

- Single 27 MHz external crystal clock input
- 3 built-in PLLs for internal clock generation

Package

- 416 BGA

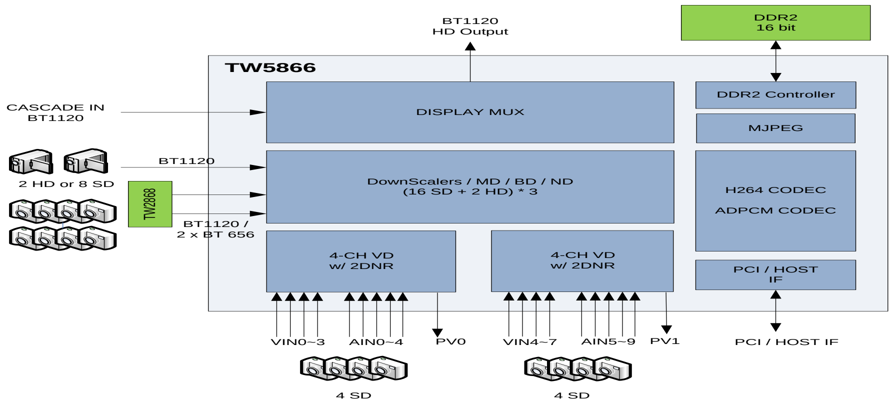

FIGURE 1. TW5866 BLOCK DIAGRAM

Ordering Information

PART NUMBER (NOTE 1)	PART MARKING	PACKAGE (PB-FREE)	PKG. DWG. #
TW5866-BA2-CR	TW5866 BA2-CR	416 BGA (27mmx27mm)	V416.27x27

1. These Intersil Pb-free BGA packaged products employ special Pb-free material sets; molding compounds/die attach materials and SnAg -e2 solder ball terminals, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free BGA packaged products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Application

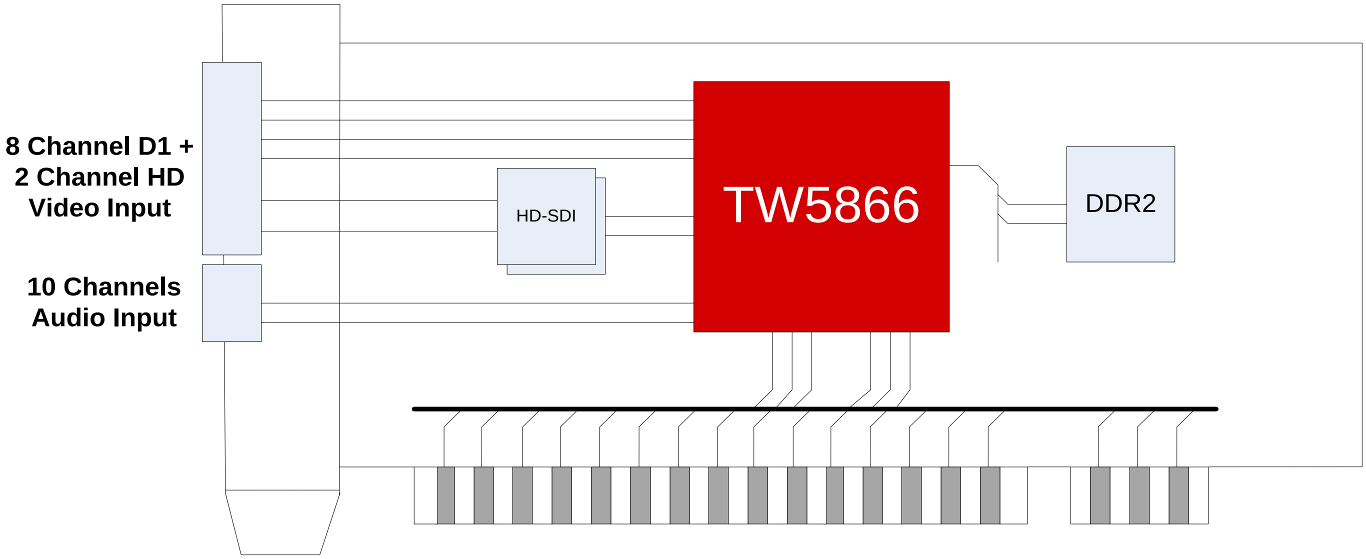

FIGURE 2. TW5866 8-CHANNEL PC CARD SOLUTION

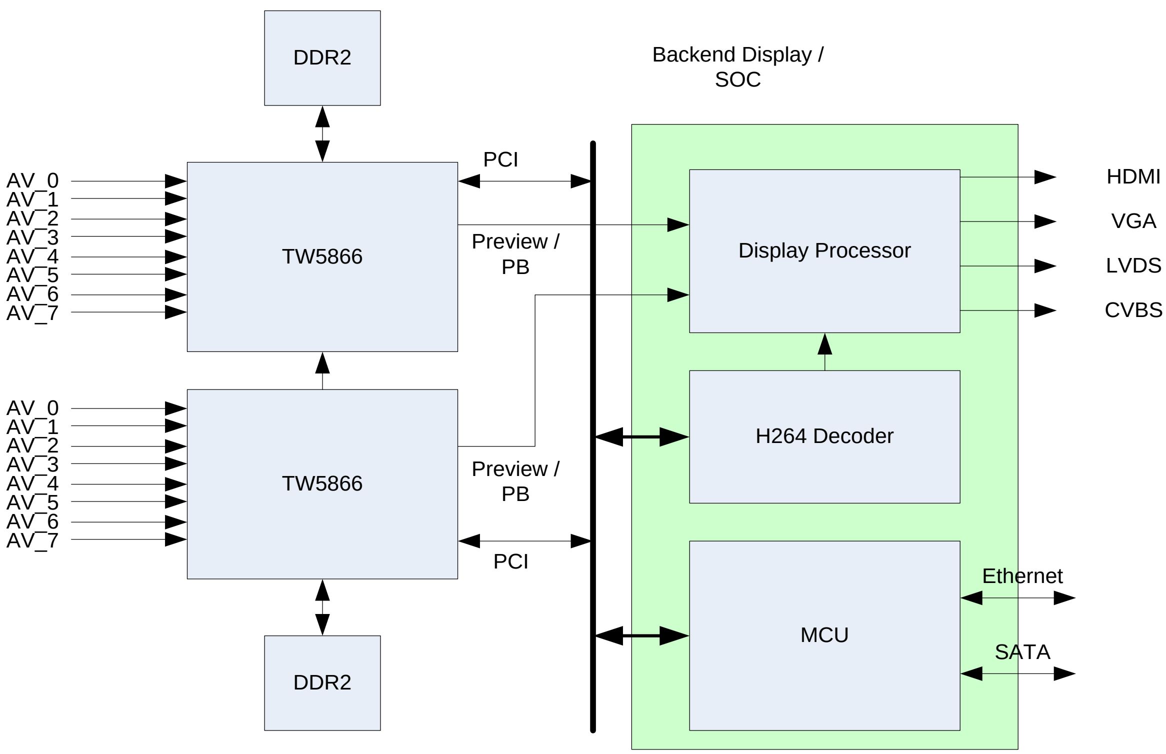

FIGURE 3. TW5866 16-CHANNEL DVR SOLUTION

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Pin Configuration (416 BGA)

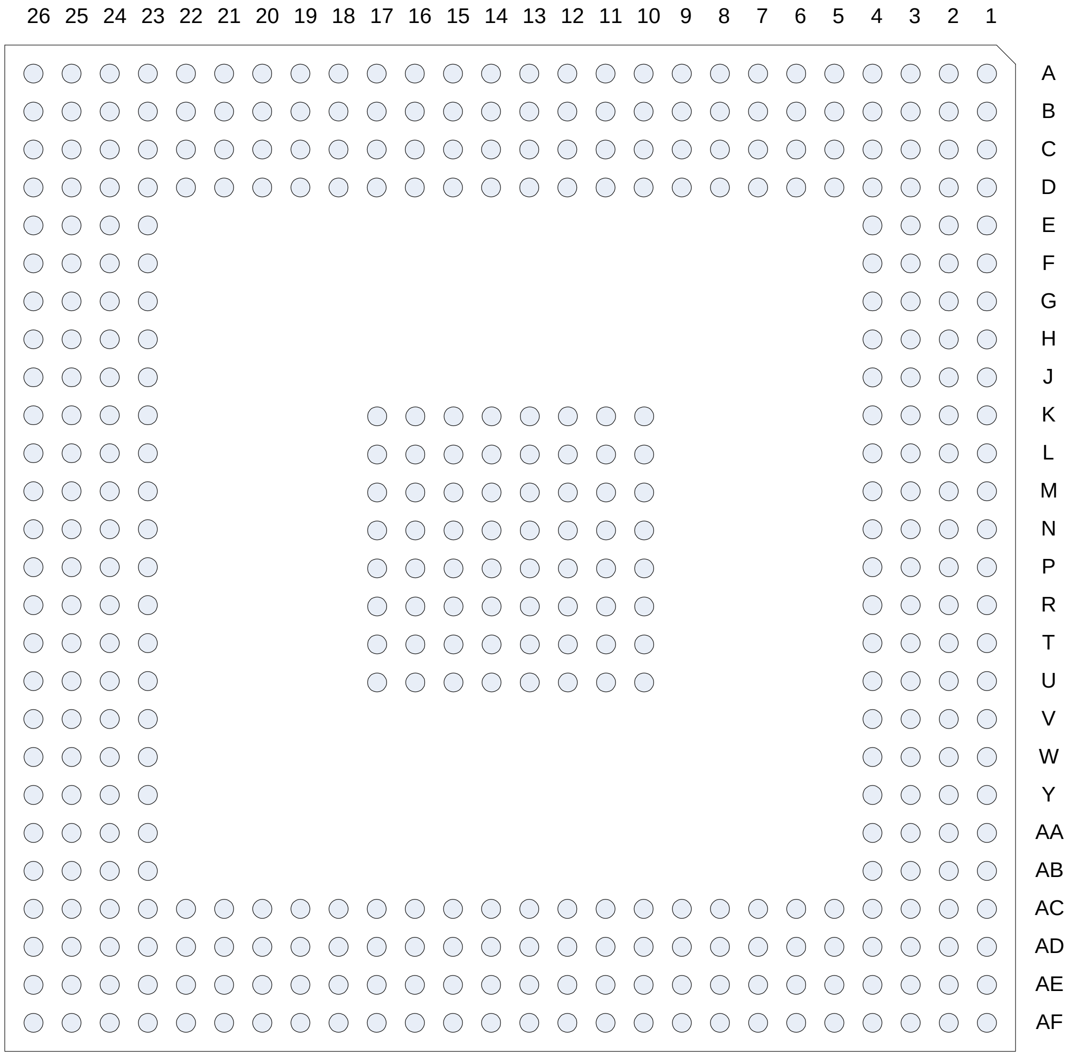


FIGURE 4. TW5866 BALL ARRANGEMENT (BOTTOM VIEW)

Ball Descriptions

Analog Interface

NAME	BALL # (MSB FIRST FOR BUS SIGNALS)	TYPE	DESCRIPTION
VIN1	M2	A	Composite video input of channel 1
VIN2	N1	A	Composite video input of channel 2
VIN3	N4	A	Composite video input of channel 3
VIN4	P3	A	Composite video input of channel 4
VIN5	R2	A	Composite video input of channel 5
VIN6	T1	A	Composite video input of channel 6
VIN7	T4	A	Composite video input of channel 7
VIN8	U3	A	Composite video input of channel 8
AIN1	Y2	A	Audio input of channel 1
AIN2	Y1	A	Audio input of channel 2
AIN3	W4	A	Audio input of channel 3
AIN4	W3	A	Audio input of channel 4
AIN5	AB1	A	Audio input of channel 5
AIN6	AB2	A	Audio input of channel 6
AIN7	AB3	A	Audio input of channel 7
AIN8	AB4	A	Audio input of channel 8
AIN51	W2	A	Audio input of channel 17 when AIN_MD = 1
AIN52	AC1	A	Audio input of channel 18 when AIN_MD = 1
AINNA	Y3	A	AINNA, connect through 2.2uF capacitor to GND
AINNB	AA4	A	AINNB, connect through 2.2uF capacitor to GND
AOUT	V2	A	Audio mixing output.

PCI Interface

NAME	BALL # (MSB FIRST FOR BUS SIGNALS)	TYPE	DESCRIPTION
PCI_AD[31:0]	AF4, AC5, AD5, AE5, AF5, AC6, AD6, AE6, AD7, AC7, AF8, AE8, AD8, AF9, AE9, AD9, AD12, AC12, AF13, AE13, AD13, AC13, AF14, AE14, AF15, AE15, AD15, AF16, AE16, AD16, AC16, AF17	I/O	PCI Address / Data Multiplexed Signals
PCI_CBE_N[3:0]	AF6, AF10, AE12, AD14	I/O	PCI Bus Command and Byte Enable Signals
PCI_PAR	AF12	I/O	PCI Parity Signal
PCI_SERR_N	AC11	I/O	PCI System Error Signal
PCI_PERR_N	AD11	I/O	PCI Parity Error Signal
PCI_STOP_N	AE11	I/O	PCI Stop Signal
PCI_DEVSEL_N	AF11	I/O	PCI Device Select Signal
PCI_TRDY_N	AC10	I/O	PCI Target Ready Signal
PCI_IRDY_N	AD10	I/O	PCI Initiator Ready Signal
PCI_FRAME_N	AE10	I/O	PCI Cycle Frame Signal
PCI_IDSEL	AE7	I/O	PCI Initialization Device Select Signal
PCI_CLK	AF7	I	PCI Clock Signal
PCI_REQ_N	AE4	O	PCI Request Signal
PCI_GNT_N	AD4	I/O	PCI Grant Signal
PCI_INTA_N	AC4	O	PCI Interrupt A signal
PCI_RST_N	AE17	I	PCI Reset signal

Misc Host Interface

NAME	BALL # (MSB FIRST FOR BUS SIGNALS)	TYPE	DESCRIPTION
GPIO[7:0]	AE25, AF25, AE24, AF24, AD23, AE23, AF23, AD22	I/O	General Purpose IO
MODE_SEL	AE22	I	PCI Mode Select. 1: PCI, 0: Asynchronous Host Interface
I2C_SDA	AF26	I/O	I2C Data Signal. The I2C signal is master, and used to control the external TW286x video decoder chips only.
I2C_SCL	AE26	I/O	I2C Clock Signal. The I2C signal is master, and used to control the external TW286x video decoder chips only.
ASYNC_ADDR[17:0]	AC21, AD21, AE21, AF21, AC20, AD20, AE20, AF20, AC19, AD19, AE19, AF19, AC18, AD18, AE18, AF18, AC17, AD17	O	Asynchronous Host Interface Address Bus
ASYNC_CS	AF22	O	Asynchronous Host Interface chip select signal

Digital Video Interface

NAME	BALL # (MSB FIRST FOR BUS SIGNALS)	TYPE	DESCRIPTION
PV1_DATA[7:0]	H3, H2, H1, G3, G2, G1, F2, F1	O	Video data of preview output port 0 in BT. 656
PV1_CLK	J1	O	Clock of preview output port 0
PV2_DATA[7:0]	L3, L2, K3, K2, K1, J4, J3, J2	O	Video data of preview output port 1 in BT. 656
PV2_CLK	L1	O	Clock of preview output port 1
PB1_DATA[7:0]	B24, A25, B25, C25, A26, B26, C26, D26	O	Video playback SD data output port 1 in BT. 656 / Video playback HD data output bit C[7:0] of BT.1120 port 1
PB1_CLK	A24	O	Clock of playback output of SD BT. 656 port 1 / HD BT. 1120 port 1
PB2_DATA[7:0]	B21, A22, B22, C22, D22, A23, B23, C23	O	Video playback SD data output port 2 in BT. 656 / Video playback HD data output bit Y[7:0] of BT.1120 port 1
PB2_CLK	A21	O	Clock of playback output of BT. 656 port 2
PB_HD2_Y_DATA[7:0]	D15, A16, B16, C16, D16, A17, B17, A18	I/O	HD playback port 2 Y[7:0] data output in BT.1120 / HD BT.1120 cascade input port data
PB_HD2_C_DATA[7:0]	B18, C18, D18, A19, B19, B20, C20, D20	I/O	HD playback port 2 C[7:0] data output in BT.1120 / HD BT.1120 cascade input port data
PB_HD2_CLK	A20	I/O	HD playback BT.1120 port 2 clock output / HD BT.1120 cascade input port clock
HD2_Y_DATA[7:0]	A11, B11, A12, B12, C12, D12, B13, C13	I	HD BT.1120 port 2 Y[7:0] data input
HD2_C_DATA[7:0]	D13, A14, B14, C14, D14, A15, B15, C15	I	HD BT.1120 port 2 C[7:0] data input
HD2_CLK	A13	I	HD BT.1120 port 2 clock input
VD1_DATA[7:0]	B6, A7, B7, C7, D7, B8, C8, D8	I	SD BT.656 port 1 data input / HD BT.1120 port 1 data input bit C[7:0]
VD1_CLK	A6	I	SD/HD video clock input port 1 for BT.656/BT.1120
VD2_DATA[7:0]	A9, B9, C9, D9, A10, B10, C10, D10	I	SD BT.656 port 2 data input / HD BT.1120 port 1 data input bit Y[7:0]
VD2_CLK	A8	I	SD BT.656 port 2 clock input

Digital Audio Interface

NAME	BALL # (MSB FIRST FOR BUS SIGNALS)	TYPE	DESCRIPTION
ACLKR	AE2	O	Audio I2S serial clock output of live / playback audio path.
ASYNR	AF1	O	Audio I2S serial sync output of live / playback audio path.
ADATM	AE1	O	Audio I2S serial data output of muxed live / playback audio channels.
ALINKI	AF2	I	Link signal for multi-chip connection serial input
ALINKO	AD1	O	Link signal for multi-chip connection serial output

DDR2 SDRAM Interface

NAME	BALL # (MSB FIRST FOR BUS SIGNALS)	TYPE	DESCRIPTION
DDR_DQ[15:0]	E26, E25, F25, G25, H26, H25, J26, J25, K26, K25, L25, M25, N26, N25, P26, P25	I/O	DDR DRAM data bus.
DDR_ADDR[14:0]	R26, R25, T26, T25, T24, U26, U25, U24, V26, V25, V24, W25, W24, Y25, Y24	O	DDR DRAM address bus
DDR_DQS[1:0]	G26, M26	I/O	DDR DRAM Data Strobe
DDR_DQSB[1:0]	F26, L26	I/O	DDR DRAM Data Strobe
DDR_ODT	AC24	O	DDR2 ODT signal to memory component
DDR_FWI	L24	I	DDR2 PHY Read Gating Signal input, to be loopback from DDR_FWO pin using the same trace length as DDR_CLK.
DDR_FWO	K24	O	DDR2 PHY Read Gating Signal output, to be loopback to DDR_FWI pin using the same trace length as DDR_CLK
DDR_DM[1:0]	G24, N24	O	DDR Byte Mask
DDR_BA[2:0]	AA26, AA25, AA24	O	DDR DRAM bank selection.
DDR_CS	AB26	O	DDR DRAM chip selection.
DDR_RASB	AB25	O	DDR DRAM row address selection.
DDR_CASB	AB24	O	DDR DRAM column address selection.
DDR_WEB	AC26	O	DDR DRAM write enable.
DDR_CLK	Y26	O	DDR DRAM Clock Output
DDR_CLKB	W26	O	DDR DRAM Clock Output
DDR_CKE	AC25	O	DDR Clock Enable

Misc Control Interfaces

NAME	BALL # (MSB FIRST FOR BUS SIGNALS)	TYPE	DESCRIPTION
EXT_SYSCLK	A4	I/O	EXT_PCLK pin is used for internal testing only. This pin should be left open
EXT_MCLK	A5	I/O	EXT_MCLK pin is used for internal testing only. This pin should be left open
EXT_CLK108	D1	I/O	EXT_CLK108 is used for internal testing only. This pin should be left open
EXT_HDCLK	C1	I/O	EXT_HDCLK is used for internal testing only. This pin should be left open
XTI (27 MHz)	B3	I	Crystal (27 MHz) Clock Input
XTO	C3	O	Crystal Clock Output
TEST_EN	AF3	I	Test mode enable signal. For internal use only. Normally tied to 0
RSTB	AE3	I	System reset. Active low.

Power / Ground

NAME	BALL # (MSB FIRST FOR BUS SIGNALS)	TYPE	DESCRIPTION
VDDO	G4, K4, AD2, AC9, AC14, AC22, D24, D21, D19, D17, D11, D3	P	Digital power for output driver 3.3V
VDDI	K17, L17, M17, N17, P17, R17, K14, U14, K13, U13, K12, L12, T12, U12, K11, L11, M11, R11, T11, U11, K10, L10, M10, R10, T10, U10	P	Digital power for internal logic 1.0V
VSSO	H4, L4, AD3, AC8, AC15, AC23, C24, C21, C19, C17, C11, A3	G	Pad Ground
VSSI	L16, M16, N16, P16, R16, T16, T14, L13, T13, R15, M14, N14, P14, R14, M13, N13, P13, R13, M12, N12, P12, R12, N11, P11, N10, P10	G	Core Ground
VDDVADC1	M1	P	Power for Video ADC0 3.3V
VDDVADC2	N2	P	Power for Video ADC1 3.3V
VDDVADC3	N3	P	Power for Video ADC2 3.3V
VDDVADC4	P4	P	Power for Video ADC3 3.3V
VDDVADC5	R1	P	Power for Video ADC4 3.3V
VDDVADC6	T2	P	Power for Video ADC5 3.3V
VDDVADC7	T3	P	Power for Video ADC6 3.3V
VDDVADC8	U4	P	Power for Video ADC7 3.3V
VSSVADC1	M3	G	Ground for Video ADC0
VSSVADC2	M4	G	Ground for Video ADC1
VSSVADC3	P1	G	Ground for Video ADC2
VSSVADC4	P2	G	Ground for Video ADC3
VSSVADC5	R3	G	Ground for Video ADC4
VSSVADC6	R4	G	Ground for Video ADC5
VSSVADC7	U1	G	Ground for Video ADC6
VSSVADC8	U2	G	Ground for Video ADC7
VDDAADC1	Y4, AA1	P	Power for Audio ADC0 3.3V
VDDAADC2	AA2, AA3	P	Power for Audio ADC1 3.3V
VSSAADC1	V4, W1	G	Ground for Audio ADC0
VSSAADC2	AC2, AC3	G	Ground for Audio ADC1
VDDADAC	V1	P	Power for Audio DAC 3.3 V
VSSADAC	V3	G	Ground for Audio DAC 3.3 V

NAME	BALL # (MSB FIRST FOR BUS SIGNALS)	TYPE	DESCRIPTION
VDDMPLL	B5	P	Power for Memory Clock PLL +1.0V
VSSMPLL	C5	G	Ground for Memory Clock PLL
VDDSYSPLL	B4	P	Power for System Clock PLL +1.0V
VSSSYSPLL	C4	G	Ground for System Clock PLL
VDDHDPLL	A2	P	Power for HD playback port Clock PLL +3.3V
VSSHDPLL	B2	G	Ground for HD playback port Clock PLL
VDDSPLL	A1	P	Power Internal 108 MHz clock PLL +3.3V
VSSSPLL	B1	G	Ground Internal 108 MHz clock PLL
VREFSSTL	E24, J24, R24,	P	SSTL Reference Voltage (0.9 V)
VSSRSSTL	F24, H24, P24	G	SSTL Reference Ground
VDDPSSTL	AB23, Y23, V23, T23, P23, M23, K23, H23, F23,	P	SSTL I/O Power +1.8V
VSSPSSTL	AA23, W23, U23, R23, N23, L23, J23, G23, E23,	G	SSTL I/O Ground
VDDSSTL	T17, U17, K16, U16, K15, U15,	P	SSTL Power +1.0V
VSSSSTL	L15, M15, N15, P15, T15, L14	G	SSTL Ground

Unconnected

NAME	BALL # (MSB FIRST FOR BUS SIGNALS)	TYPE	DESCRIPTION
NC	C2, C6, D2, D4, D5, D6, D23, D25, E1, E2, E3, E4, F3, F4, M24, AD24, AD25, AD26	NC	Keep these Open

Functional Description

The Intersil TW5866 supports H.264 base-line profile main stream encoding for up to 8 channel of D1 or 16 channels of CIF video content plus encoding of secondary stream in ¼ or 1/16 size of each of the main stream channels. In H.264 decoding, TW5866 supports up to 8 channels of D1 channel decoding. TW5866 also supports motion JPEG encoding. The encoded bitstream are available through the PCI / asynchronous host interface. When both encoding / decoding are on, TW5866 can support streams up to 4 channels of D1 stream in full duplex.

There are 8 video decoders embedded in TW5866 to support up to 8 analog video CVBS inputs. In addition, there are 2 ITU-R BT. 656 digital ports to support up to 2 external TW2866 video decoder chips. The digital input interface runs up to 108 MHz to carry up to 4 channels of video streams in byte-interleaved format. Alternatively, there are 3 ITU-R BT. 1120 interfaces. The first two ports are used for external HD video sources, while the third one is dedicated for TW5866 cascade mux purpose. In total, there are 16 SD or 2 HD video channels received by the TW5866 codec, with 8 in analog format, and 8 SD or 2 HD in digital format.

TW5866 supports 2 ITU-R BT. 656 output ports for preview purpose to an external display chip. The preview ports runs up to 108 MHz also, to support total of 8 D1 channel output for the 8 on-chip video decoders. The preview ports support byte-interleaved BT. 656 format as TW2866. In addition, the preview video can also be available through the PCI interface for PC-card application.

For each of the external SD video input channels, there is a set of alert detection module generating the motion / blind / night detection alert signal for external CPU. There are also 3 downscalers to downscale D1 video into Half D1 (360x240) / CIF (360x120) and QCIF (180x120) size. For the HD channels, the downscalers are used to support downscale of original picture into either ½ in horizontal direction, ½ in both horizontal and vertical directions, or ¼ in horizontal and ½ in vertical directions. Each of these picture sizes can be flexibly selected into the preview output ports, the H.264 encoder engine, the motion JPEG engine, or the PCI preview channel.

CVBS Video Input

FORMATS

The TW5866 has 8 on-chip video decoders with build-in automatic standard discrimination circuitry. The circuit uses burst-phase, burst-frequency and frame rate to identify NTSC, PAL or SECAM color signals. The standards that can be identified are NTSC (M), NTSC (4.43), PAL (B, D, G, H, I), PAL (M), PAL (N), PAL (60) and SECAM (M). Each standard can be included or excluded in the standard recognition process by software control. The exceptions are the base standard NTSC and PAL, which are always enabled. The identified standard is indicated by the Standard Selection (SDT) register. Automatic standard detection can be overridden by software controlled standard selection.

TW5866 supports all common video formats as shown in Table 1.

TABLE 1. VIDEO INPUT FORMATS SUPPORTED BY THE TW5866

FORMAT	LINES	FIELDS	FSC	COUNTRY
NTSC-M	525	60	3.579545 MHz	U.S., many others
NTSC-Japan (1)	525	60	3.579545 MHz	Japan
PAL-B, G, N	625	50	4.433619 MHz	Many
PAL-D	625	50	4.433619 MHz	China
PAL-H	625	50	4.433619 MHz	Belgium
PAL-I	625	50	4.433619 MHz	Great Britain, others
PAL-M	525	60	3.575612 MHz	Brazil
PAL-CN	625	50	3.582056 MHz	Argentina
SECAM	625	50	4.406MHz 4.250MHz	France, Eastern Europe, Middle East, Russia
PAL-60	525	60	4.433619 MHz	China
NTSC (4.43)	525	60	4.433619 MHz	Transcoding

NOTE: :

1. . NTSC-Japan has 0 IRE setup.

The analog front-end converts analog video signals to the required digital format. There are six analog front-end channels. Three channels are dedicated to analog video support. Every channel contains analog anti-aliasing filter, clamping circuit and 10-bit ADCs. It allows the support of CVBS, S-video and YPbPr component input signals for main or sub display. The other three channels are dedicated to YPbPr component video or RGB input support. Every channel contains the analog clamping circuit, variable gain amplifier and high speed ADCs. It allows three separate inputs to be connected simultaneously. A built-in line locked PLL is used to generate the sampling clock for various inputs.

ANALOG FRONT-END

The TW5866 contains four 10-bit ADC (Analog to Digital Converters) to digitize the analog video inputs. The ADC can be put into power-down mode by the VADCn_PD register at 0xEC9. The TW5866 also contains an anti-aliasing filter to prevent out-of-band frequency in analog video input signal. So there is no need of external components in analog input pin except ac coupling capacitor and termination resistor. Figure 5 shows the frequency response of the anti-aliasing filter.

DECIMATION FILTER

The digitized composite video data are over-sampled to simplify the design of analog filter. The decimation filter is required to achieve optimum performance and prevent high frequency components from being aliased back into the video image when down-sampled. Figure 6 shows the characteristic of the decimation filter.

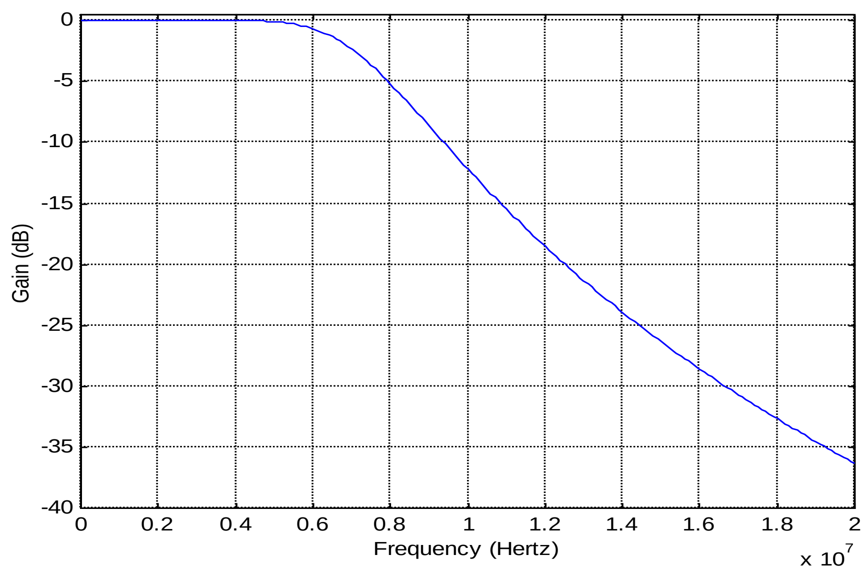


FIGURE 5. THE FREQUENCY RESPONSE OF THE VIDEO INPUT ANTI-ALIAS FILTER

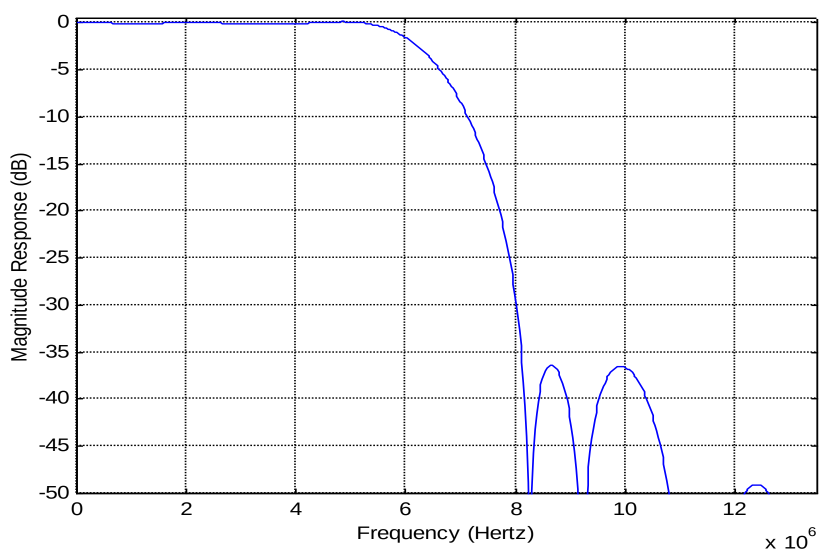


FIGURE 6. THE CHARACTERISTIC OF DECIMATION FILTER

AGC AND CLAMPING

All four analog channels have built-in clamping circuit that restores the signal DC level. The Y channel restores the back porch of the digitized video to a level of 60. This operation is automatic through internal feedback loop. The Automatic Gain Control (AGC) of the Y channel adjusts input gain so that the sync tip is at a desired level. Programmable white peak protection logic is included to prevent saturation in the case of abnormal signal proportion between sync and white peak level.

SYNC PROCESSING

The sync processor of TW5866 detects horizontal synchronization and vertical synchronization signals in the composite video or in the Y signal of an S-video or component signal. The processor contains a digital phase-locked-loop and decision logic to achieve reliable sync detection in stable signal as well as in unstable signals such as those from VCR fast forward or backward.

The vertical sync separator detects the vertical synchronization pattern in the input video signals. In addition, the actual sync determination is controlled by a detection window to provide more reliable synchronization. An option is available to provide faster responses for certain applications. The field status is determined at vertical synchronization time. The field logic can also be controlled to toggle automatically while tracking the input

Y/C SEPARATION

The color-decoding block contains the luminance / chrominance separation for the composite video signal and multi-standard color demodulation. For NTSC and PAL standard signals, the luminance/chrominance separation can be done either by comb filter or notch/band-pass filter combination. For SECAM standard signals, adaptive notch/band-pass filter is used. The default selection for NTSC/PAL is comb filter. In the case of comb filter, the TW5866 separates luminance (Y) and chrominance (C) of a NTSC/PAL composite video signal using a proprietary 4H adaptive comb filter. The filter uses a four-line buffer. Adaptive logic combines the upper-comb and the lower-comb results based on the signal changes among the previous, current and next lines. This technique leads to excellent Y/C separation with small cross luminance and cross color at both horizontal and vertical edges

Due to the line buffer used in the comb filter, there are always two lines processing delay at the output except for the component input mode which has only one line delay. If the notch/band-pass filters is selected, the characteristic of the filters of luminance notch filter is shown in Figure 7 for both NTSC and PAL system.

COLOR DECODING

Chrominance Demodulation

The color demodulation for NTSC and PAL standard is done by first quadrature mixing the chrominance signal to the base band. A low-pass filter is then used to remove carrier signal and yield chrominance components. The low-pass filter characteristic can be selected for optimized transient color performance. For the PAL system, the PAL ID or the burst phase switching is identified to aid the PAL color demodulation.

For SECAM, the color information is FM modulated onto different carrier. The demodulation process therefore consists of FM demodulator and de-emphasis filter. During the FM demodulation, the chrominance carrier frequency is identified and used to control the SECAM color demodulation.

The sub-carrier signal for use in the color demodulator is generated by direct digital synthesis PLL that locks onto the input sub-carrier reference (color burst). This arrangement allows any sub-standard of NTSC and PAL to be demodulated easily with single crystal frequency.

Figure 8 and Figure 9 show the frequency response of Chrominance Band-Pass and Low-Pass Filter Curves.

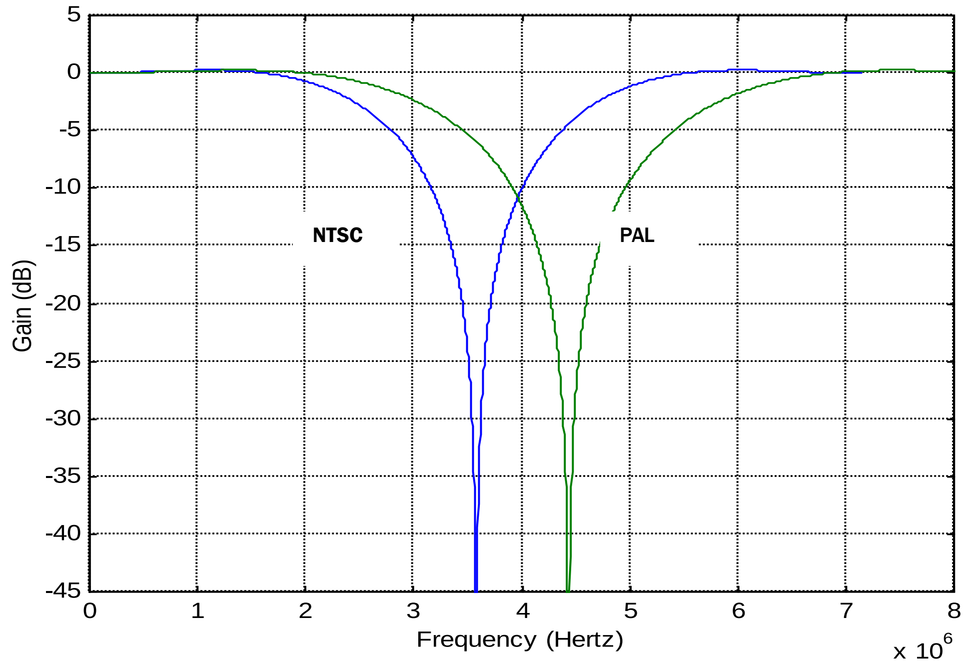


FIGURE 7. THE CHARACTERISTICS OF LUMINANCE NOTCH FILTER FOR NTSC AND PAL

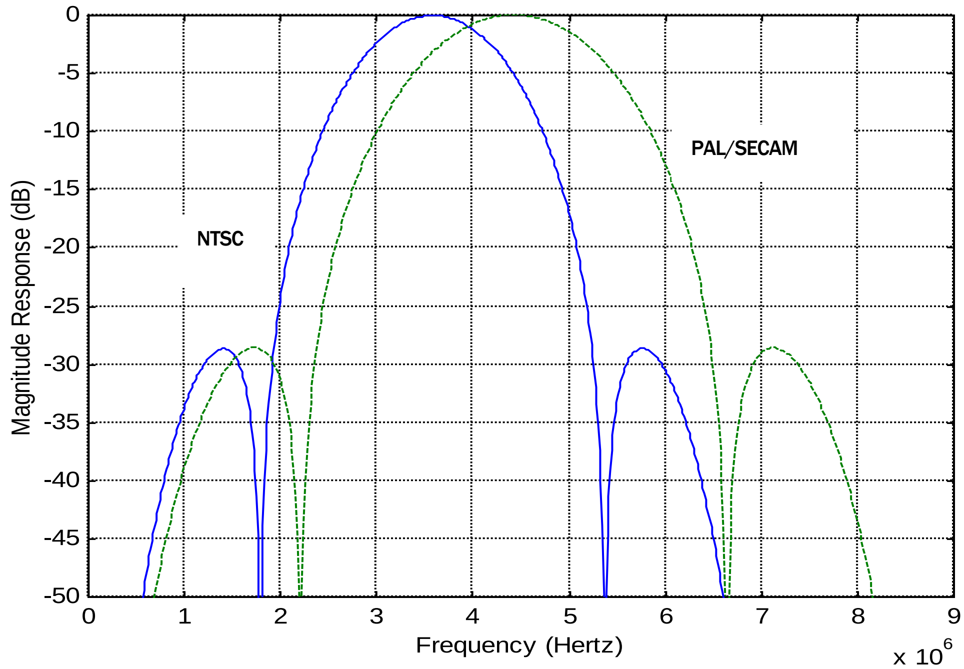


FIGURE 8. THE CHARACTERISTICS OF CHROMINANCE BAND-PASS FILTER FOR NTSC PAL

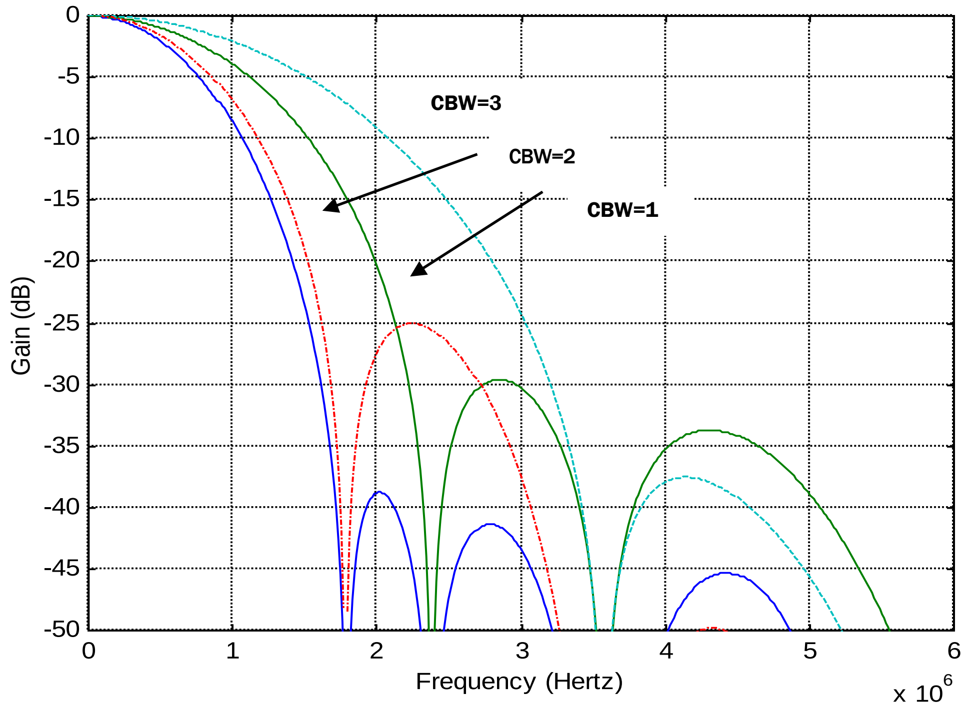


FIGURE 9 THE CHARACTERISTICS OF CHROMINANCE LOW-PASS FILTER CURVES

ACC (AUTOMATIC COLOR GAIN CONTROL)

The Automatic Chrominance Gain Control (ACC) compensates the reduced amplitudes caused by high-frequency loss in video signal. In the NTSC/PAL standard, the color reference signal is the burst on the back porch. It is measured to control the chrominance output gain. The range of ACC control is –6db to +24db.

CHROMINANCE PROCESSING

Chrominance Gain, Offset and Hue Adjustment

When decoding NTSC signals, TW5866 can adjust the hue of the chrominance signal. The hue is defined as a phase shift of the subcarrier with respect to the burst. This phase shift of NTSC decoding can be programmed through a control register. For the PAL standard, the PAL delay line is provided to compensate any hue error; therefore, there is no hue adjustment available. The color saturation can be adjusted by changing the gain of Cb and Cr signals for all NTSC, PAL and SECAM formats. The Cb and Cr gain can be adjusted independently for flexibility.

CTI (Color Transient Improvement)

The TW5866 provides the Color Transient Improvement function to further enhance the image quality. The CTI enhance the color edge transient without any overshoot or under-shoot.

Luminance Processing

The TW5866 adjusts brightness by adding a programmable value (in register BRIGHTNESS) to the Y signal. It adjusts the picture contrast by changing the gain (in register CONTRAST) of the Y signal.

The TW5866 also provide programmable peaking function to further enhance the video sharpness. The peaking control has built-in coring function to prevent enhancement of noise.

Figure 10 shows the characteristics of the peaking filter for four different gain modes and different center frequencies.

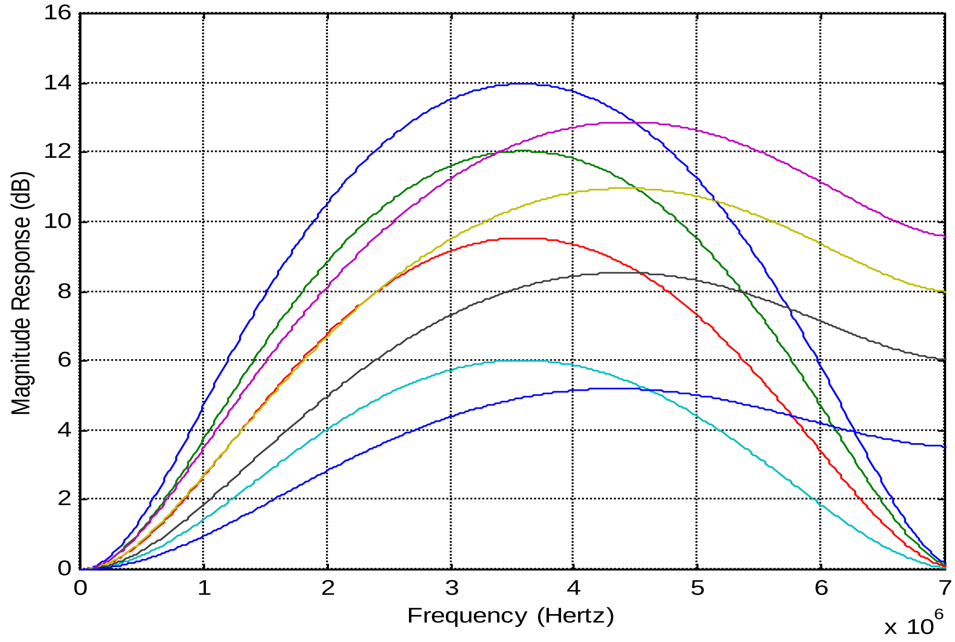


FIGURE 10. THE CHARACTERISTIC OF LUMINANCE PEAKING FILTER

ITU-R BT. 656 Digital Input

TW5866 supports 2 BT. 656 ports to connect up to 2 external video decoder chips.

TABLE 2. SD DIGITAL VIDEO INPUT PORT 1 SHARING

PORT #	DATA SIGNAL	CLOCK SIGNAL
1st BT.656	VD1_DATA	VD1_CLK
2nd BT.656	VD2_DATA	VD2_CLK

Each of the BT. 656 port runs at 108 MHz and supports 4 channels, in byte-interleaved format. In standard single channel ITU-R BT.656 format, SAV and EAV sequences are inserted into the data stream to indicate the active video time. It is noted that the number of active pixels per line is constant in this mode regardless of the actual incoming line length. The output timing is illustrated in Figure 11. The SAV and EAV sequences are shown in Table 3. An optional set of 656 SAV/EAV code sequence can be enabled to identify no-video status using the SAV_DETVID bit at 0x178 and 0x378.

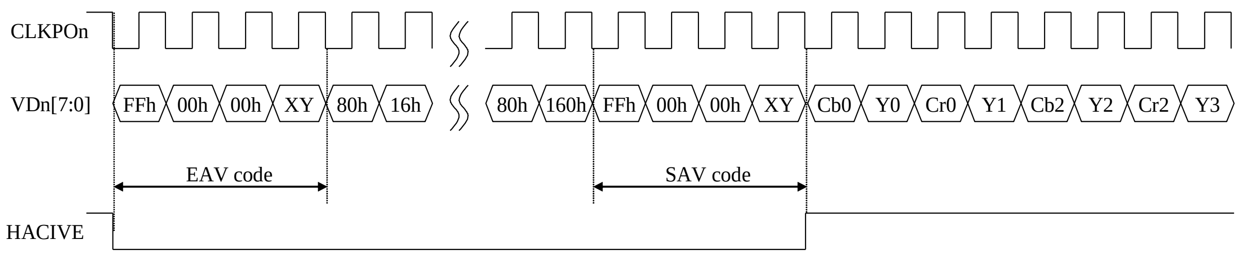


FIGURE 11. TIMING DIAGRAM OF ITU-R BT.656 FORMAT

TABLE 3. ITU-R BT.656 SAV AND EAV CODE SEQUENCE

CONDITION			656 FVH VALUE			SAV/EAV CODE SEQUENCE				
FIELD	V TIME	H TIME	F	V	H	FIRST	SECOND	THIRD	FOURTH NORMAL	FOURTH OPTION*
EVEN	Blank	EAV	1	1	1	0xFF	0x00	0x00	0xF1	0x71
EVEN	Blank	SAV	1	1	0	0xFF	0x00	0x00	0xEC	0x6C
EVEN	Active	EAV	1	0	1	0xFF	0x00	0x00	0xDA	0x5A
EVEN	Active	SAV	1	0	0	0xFF	0x00	0x00	0xC7	0x47
ODD	Blank	EAV	0	1	1	0xFF	0x00	0x00	0xB6	0x36
ODD	Blank	SAV	0	1	0	0xFF	0x00	0x00	0xAB	0x2B
ODD	Active	EAV	0	0	1	0xFF	0x00	0x00	0x9D	0x1D
ODD	Active	SAV	0	0	0	0xFF	0x00	0x00	0x80	0x00

NOTE: * OPTION INCLUDES VIDEO LOSS INFORMATION IN ITU-R BT.656

In order to reduce pin counts and support more channels, four channel of D1 (720x480 / 720x576) video stream are time-division-multiplexed into a multi-channel data format. With this, TW5866 implements a single 8 bit bus at 4 times the base clock rate of 27MHz while quadrupling the data rate on a single bus to meet the new requirement, individually, each channel data arrangement still retains the base band 27MHz ITU-R BT.656 specification. For interface that can accept the new 108MHz clock bus, only one single clock at 108MHz is required. Embedded timing (SAV-EAV) code and channel ID are inserted into each channel for de-multiplexing and separation of channel data.

Figure 12 depicts the temporal arrangement of the video data in 108MHz data rate. Each channel is byte level time-division multiplexed (TDM). Main clock is 108MHz clock. This bit stream can be de-multiplexed into 4 individual channels by sampling once in every 4 clock cycles, as shown in Figure 13. After de-multiplexing, the channel ID can be identified through the EAV/SAV code from Table 4 and Table 5.

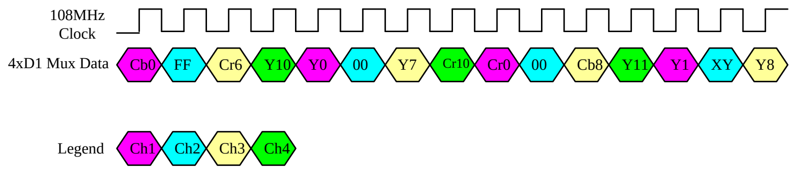


FIGURE 12. TIMING DIAGRAM OF 108MHZ 4 CH D1 TIME-DIVISION-MULTIPLEXED VIDEO DATA

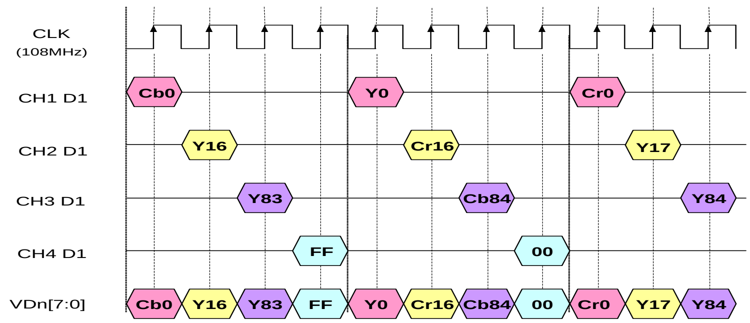


FIGURE 13. PIN OUTPUT TIMING OF 108MHZ 4 CH D1 TIME-DIVISION-MULTIPLEXED VIDEO DATA WITH 108MHZ CLOCK

TABLE 4. SPECIAL FORMAT OF ITU-R BT. 656 EMBEDDED TIMING CODE AND CHANNEL ID CODE WHEN VIDEO IS ACTIVE

CONDITION			656 FVH VALUE			SAV-EAV CODE						
									FOURTH			
FIELD	V-TIME	H-TIME	F	V	H	FIRST	SECOND	THIRD	CH1	CH2	CH3	CH4
EVEN	BLANK	EAV	1	1	1	0xFF	0x00	0x00	0xF0	0xF1	0xF2	0xF3
EVEN	BLANK	SAV	1	1	0	0xFF	0x00	0x00	0xE0	0xE1	0xE2	0xE3
EVEN	ACTIVE	EAV	1	0	1	0xFF	0x00	0x00	0xD0	0xD1	0xD2	0xD3
EVEN	ACTIVE	SAV	1	0	0	0xFF	0x00	0x00	0xC0	0xC1	0xC2	0xC3
ODD	BLANK	EAV	0	1	1	0xFF	0x00	0x00	0xB0	0xB1	0xB2	0xB3
ODD	BLANK	SAV	0	1	0	0xFF	0x00	0x00	0xA0	0xA1	0xA2	0xA3
ODD	ACTIVE	EAV	0	0	1	0xFF	0x00	0x00	0x90	0x91	0x92	0x93
ODD	ACTIVE	SAV	0	0	0	0xFF	0x00	0x00	0x80	0x81	0x82	0x83

TABLE 5. SPECIAL FORMAT OF ITU-R BT. 656 EMBEDDED TIMING CODE AND CHANNEL ID CODE WHEN VIDEO IS NOT ACTIVE

CONDITION			656 FVH VALUE			SAV-EAV CODE						
									FOURTH			
FIELD	V-TIME	H-TIME	F	V	H	FIRST	SECOND	THIRD	CH1	CH2	CH3	CH4
EVEN	BLANK	EAV	1	1	1	0xFF	0x00	0x00	0x70	0x71	0x72	0x73
EVEN	BLANK	SAV	1	1	0	0xFF	0x00	0x00	0x60	0x61	0x62	0x63
EVEN	ACTIVE	EAV	1	0	1	0xFF	0x00	0x00	0x50	0x51	0x52	0x53
EVEN	ACTIVE	SAV	1	0	0	0xFF	0x00	0x00	0x40	0x41	0x42	0x43
ODD	BLANK	EAV	0	1	1	0xFF	0x00	0x00	0x30	0x31	0x32	0x33
ODD	BLANK	SAV	0	1	0	0xFF	0x00	0x00	0x20	0x21	0x22	0x23
ODD	ACTIVE	EAV	0	0	1	0xFF	0x00	0x00	0x10	0x11	0x12	0x13
ODD	ACTIVE	SAV	0	0	0	0xFF	0x00	0x00	0x00	0x01	0x02	0x03

ITU-R BT. 1120 Video Input

TW5866 features three HD video input interfaces. It supports standard single channel BT. 1120 format in 16-bit of data with luminance and chrominance separated. The resolution supported includes H960 (960x480 / 960x576), 720p (1280x720), 1080i (1920x1080), and 4D1 (1440x960 / 1440 x 1152). Out of the three HD input ports, the first and the third HD input ports are used to take in external HD sources, while the second one is used as cascade input of multiple TW5866 devices.

The first HD input port is pin shared with two SD BT.656 input ports. The cascade HD input port is pin shared with the second HD playback output ports. The shared pin is as shown in the following tables.

TABLE 6. HD DIGITAL VIDEO INPUT PORT 1 SHARING

PORT #	DATA	CLOCK
1st BT.1120	{VD2_DATA, VD1_DATA}	VD1_CLK
2nd BT.1120	HD2_DATA	HD2_CLK
Cascade Input BT.1120	PB_HD2_DATA	PB_HD2_CLK

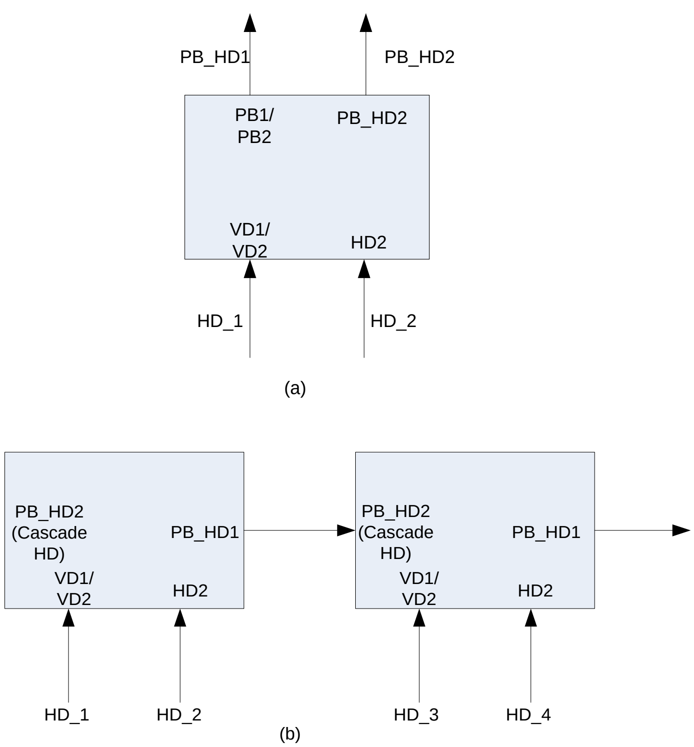


FIGURE 14. HD INTERFACES FOR (A) TWO HD INPUTS / TWO HD PLAYBACK, (B) HD CASCADE

ITU-R BT. 656 Preview Video Output

TW5866 provides two preview digital output interfaces in byte-interleaved format the same as TW2866, as shown in Figure 12. Each of the preview output can carry up to 4 channels of video streams from on-chip video decoders. The configuration of supported format / combination is shown in the Table 7 and Table 8.

TABLE 7. DIGITAL PREVIEW VIDEO OUTPUT PORT 1 CONFIGURATION

	PV1_SEL	PORT 1
108 MHz	0	Channel 1, 2, 3, 4
27 MHz	1	Channel 1
	2	Channel 2
	3	Channel 3
	4	Channel 4
	5	Channel 5
	6	Channel 6
	7	Channel 7
	8	Channel 8
54 MHz	9	Channel 1, 2
	10	Channel 3, 4
	11	Channel 5, 6
	12	Channel 7, 8

TABLE 8. DIGITAL PREVIEW VIDEO OUTPUT PORT 2 CONFIGURATION

	PV2_SEL	PORT 2
108 MHz	0	Channel 5, 6, 7, 8
27 MHz	1	Channel 5
	2	Channel 6
	3	Channel 7
	4	Channel 8
	5	Channel 1
	6	Channel 2
	7	Channel 3
	8	Channel 4
54 MHz	9	Channel 5, 6
	10	Channel 7, 8
	11	Channel 1, 2
	12	Channel 3, 4

ITU-R BT. 656 SD Playback Output

TW5866 features two BT. 656 output ports for playback of decoded H.264 as well as live captured video sources from either on-chip video decoder or external video chips through the digital video input ports. The BT. 656 PB ports support both byte-interleaved as well as frame/field interleaved format. Each of them can run at either of 27, 54 or 108 MHz.

BYTE-INTERLEAVED FORMAT

The BT. 656 ports supports byte-interleaved format to multiplex multiple D1 videos into one output port. The byte-interleaved video format is shown in Figure 12. Each of the D1 video is formed from either a single channel video, or quad-channel video of CIF picture size. The formed D1 picture can be either interlaced or progressive, depending on the original video source format. This is shown in Figure 15 and Figure 16. Multiple D1 picture is then byte-interleaved together to allow one BT. 656 port to carry 4 D1 of video throughput. Therefore, when running at 108 MHz, a BT. 656 playback output can carry either 4 single channel D1 video, or up to 16 channel of CIF video. With two BT. 656 output ports, the output can carry 8 D1 or 32 CIF video. Note that this number is an upper limit from the BT 656 interface itself. It does not include the limitation from H.264 decoder capability or DDR2 memory bandwidth.

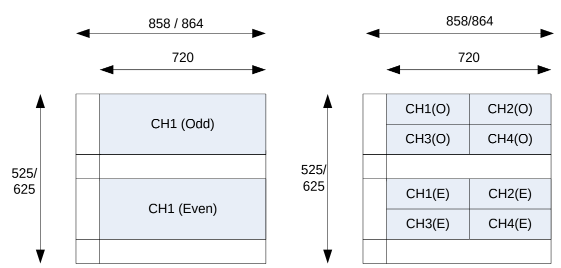


FIGURE 15. FORMED INTERLACED D1 PICTURE AS BYTE-INTERLEAVED SOURCE OF BT 656 PLAYBACK PORT

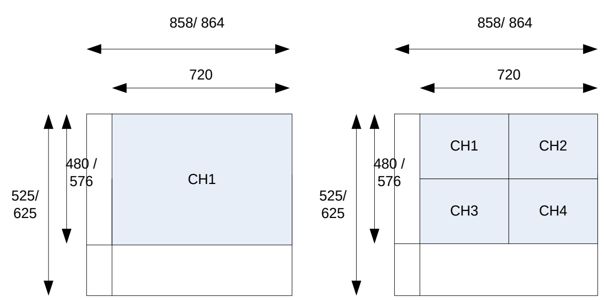


FIGURE 16. FORMED PROGRESSIVE D1 PICTURE AS BYTE-INTERLEAVED SOURCE OF BT 656 PLAYBACK PORT

FRAME/FIELD-INTERLEAVED FORMAT

The BT. 656 PB1 port also supports frame/field-interleaved format to interface with external display chips such as TW2880 or TW2851. When a frame/field–interleaved format is used, a channel ID field in VBI is used to identify the channel numbers associated with each field/frame. With this channel ID embedded, the channels can be different from field/frame to field/frame. There are several types supported in field/frame interleaving, as shown in Figure 17, Figure 18 and Figure 19. Note that in field interleaved mode, the channels can change from field to field. While in frame interleaved mode, the channels change from frame (2 fields) to frame.

Noted that the picture size of the sources for Type 0 and 1 can be D1 or HD1. The picture size of sources for Type 2 and 3 can be D1, HD1, CIF, or HCIF. The picture size of sources for Type 6 can be D1, HD1, or CIF.

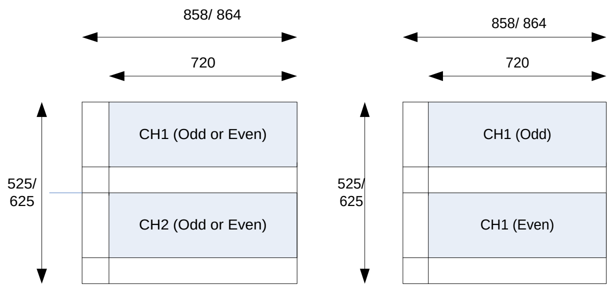


FIGURE 17. INTERLACED D1 FIELD INTERLEAVED: TYPE 0 (LEFT) AND FRAME INTERLEAVED: TYPE 1 (RIGHT)

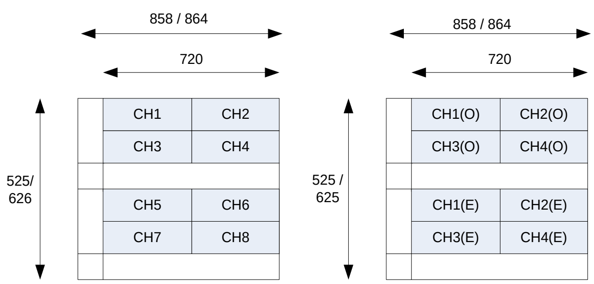


FIGURE 18. INTERLACED CIF FIELD INTERLEAVED: TYPE 2 (LEFT) AND FRAME INTERLEAVED: TYPE 3 (RIGHT)

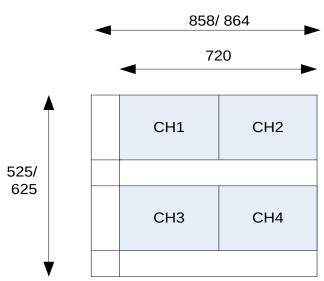


FIGURE 19. HALF D1 FIELD INTERLEAVED: TYPE 6

ITU-R BT. 1120 HD Playback Output

TW5866 has two BT. 1120 ports supporting two external HD displays. In this mode, there is no either byte or field/frame interleaved support. The only formats supported are either single channel or 4 channel of a quarter size of the original picture resolution in quad-windows format. There is no mixing of D1 / HD video resolutions supported in one picture.

There are three HD picture resolutions supported. The first is 4D1 (1440 x 960 / 1440 x 1152) at 54 MHz, shown in Figure 20. It supports 1, 4, and 16 windows of space mux from D1 sources. The second is 720P (1280x720) at 74.25 MHz, shown in Figure 21. It supports 1, 4 windows space mux from 720P sources. The third is 1080i (1920 x 1080) at 74.25 MHz, shown in Figure 22. It supports 1, 4 windows from 1080i sources.

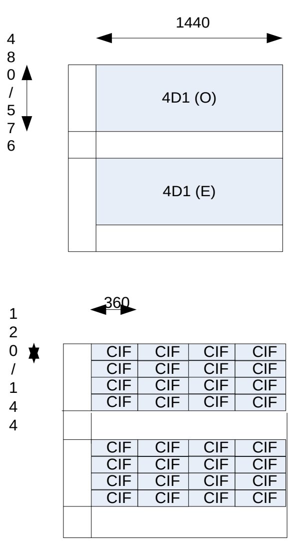


FIGURE 20. 4D1 OUTPUT FORMAT: SINGLE CHANNEL (LEFT), QUAD CHANNEL (RIGHT), AND 16 CHANNEL (BOTTOM)

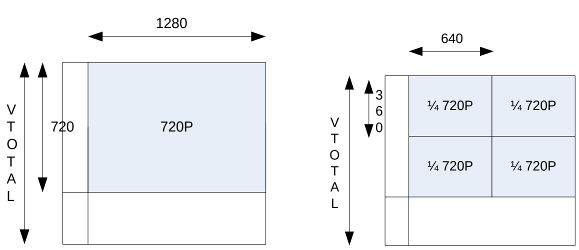


FIGURE 21. 720P OUTPUT FORMAT: SINGLE CHANNEL (LEFT) AND QUAD CHANNEL (RIGHT)

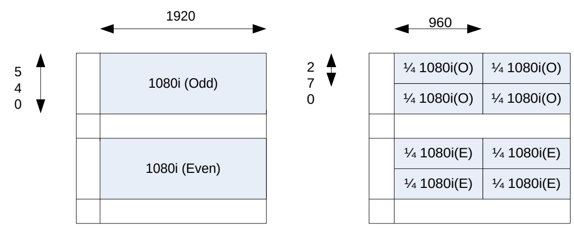


FIGURE 22. 1080I OUTPUT FORMAT: SINGLE CHANNEL (LEFT) AND QUAD CHANNEL (RIGHT)

TW5866 Cascade through BT. 1120

TW5866 supports a cascade feature to allow multiplexing of multiple channels across two TW5866 chips. When this feature is turned on, one of the PB BT.1120 output port is configured as the third BT. 1120 input port on the TW5866 to receive HD picture from previous TW5866 BT. 1120 output, and overlay with the channels in the current chip. Figure 23 shows cascade of two TW5866 to mux up to 16 channels of D1 video into a 4D1 resolution output, in 1, 4 or 16 windows. Figure 24 shows the cascade to support up to 4 HD channels in either 1 or 4 windows. Note that the mux feature of TW5866 is limited that the SD and HD channels cannot be mixed. Different HD resolutions (720P vs. 1080i) cannot be mixed either.

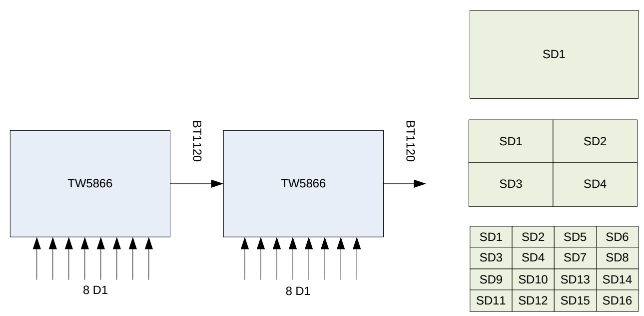


FIGURE 23. TWO TW5866 CASCADE TO SUPPORT 1 WINDOW OF 4X D1 RESOLUTION, 4 WINDOWS IN D1 OR 16 WINDOWS IN CIF

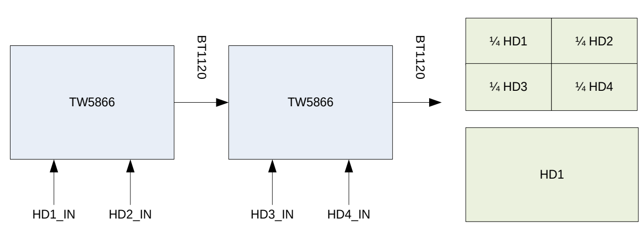


FIGURE 24. TWO TW5866 CASCADE TO SUPPORT SINGLE HD WINDOWS OR 4 WINDOWS IN ¼ HD

Pre-processing Module

Behind the on-chip video decoder and the digital BT.656 input ports are several pre-processing modules per channel such as the motion detection, downscalers, and channels selectors. The front-end pre-processing module prepares all the video streams into a format into a correct size that can be used by the backend modules such as line-interleaving preview module, H.264 encoding module, motion JPEG encoding modules, and the PCI preview module.

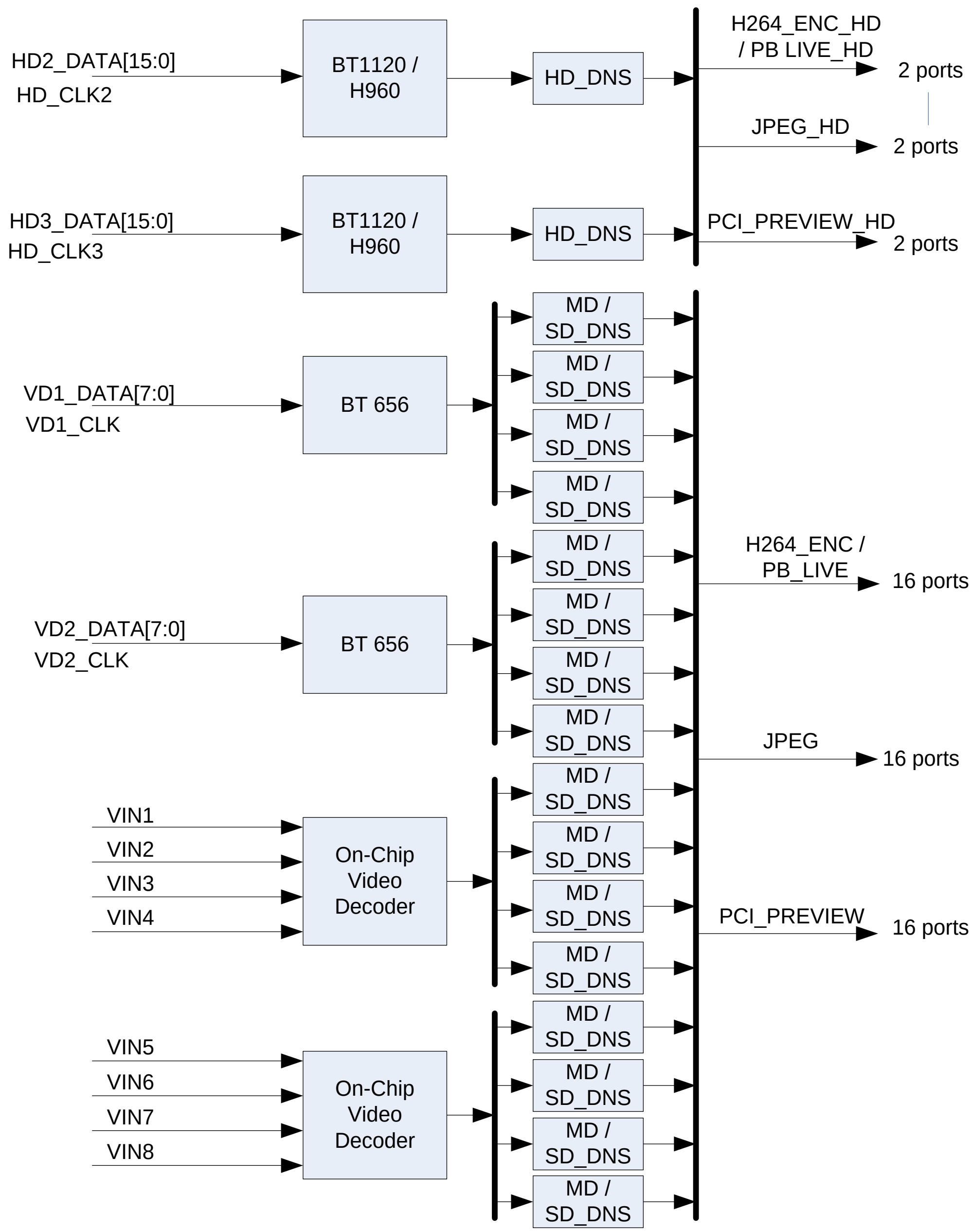


FIGURE 25. THE PRE-PROCESSING MODULE

Downscalers

The TW5866 has 18 sets of fixed downscalers, one for each incoming SD / HD channels, to downscale the D1 / HD picture size into one half horizontally, one quarter horizontally, and one half vertically. With these, the combination of picture size can be 720x240, 360x240, 360x120, 180x120 (NTSC), or 720x288, 360x288, 360x144, 180x144 (PAL) for SD, or similar corresponding size for the input HD pictures. These output pictures can be independently selected for each of the external digital preview port in line interleaved mode, the H.264 encoding input, the Motion JPEG encoding input, and the PCI bus preview input.

Motion Detection

The TW5866 supports a motion detector for each of the 16 SD and 2 HD input channels. The built-in motion detection algorithm uses the difference of luminance level between current and the reference field.

To detect motion properly according to situation needed, the TW5866 provides several sensitivity and velocity control parameters for each motion detector. The TW5866 supports manual strobe function to update motion detection so that it is more appropriate for user-defined motion sensitivity control.

When motion is detected in any video inputs, the TW5866 provides the interrupt request to host via the IRQ pin. Through which the host processor can read the motion information by accessing the motion status register.

Mask and Detection Region Selection

The motion detection algorithm utilizes the full screen video data and detects individual motion of pre-partitioned cells. In SD channels, there are 16x12 cells. The full screen for motion detection consists of 704 pixels and 240 lines for NTSC and 288 lines for PAL. Starting pixel in horizontal direction can be shifted from 0 to 15 pixels using the MD_PIXEL_OS register.

In HD, the full picture is partitioned into either 4 areas for 1080i/720p, or 2 areas for 960H. The motion detection of each area is also 16x12 cells, similar to the SD motion detection. Therefore the motion detection result is 4 sets of SD results in 1080i/720p, and 2 sets of SD results in 960H. The cell size in HD depends on the picture resolution. The cell size is set through the registers in 0x720 / 0x721 / 0x730 / 0x731. Just configure each area in the HD the same way as we configured for SD. To read the MD result from each quadrant of a HD channel, simply set the HD_RGR_MOTION_SEL at register 0x782 to select a channel/quadrant, then read the registers in 0x7A0 ~ 0x7B7.

Each cell can be masked via the MD_MASK registers. If the mask bit in specific cell is set, the related cell is ignored for motion detection. The MD_MASK register has different function for reading and writing mode. For writing mode, setting MD_MASK register to “1” inhibits the specific cell from detecting motion. For reading mode, the MD_MASK register provides the results of the motion detection.

Sensitivity Control

The motion detector has 4 sensitivity parameters to control threshold of motion detection such as the level sensitivity via the MD_LVSENS register, the spatial sensitivity via the MD_SPSENS and MD_CELSENS register, and the temporal sensitivity parameter via the MD_TMPSENS register.

Level Sensitivity

In built-in motion detection algorithm, the motion is detected when luminance level difference between current and reference field is greater than MD_LVSENS value. Motion detector is more sensitive for the smaller MD_LVSENS value and less sensitive for the larger. When the MD_LVSENS is too small, the motion detector may be weak in noise.

Spatial Sensitivity

The TW5866 uses 192 (16x12 for SD) or 768 (32x24 for HD) detection cells in full screen for motion detection. Each detection cell is composed of 44 pixels and 20 lines for NTSC, 24 lines for PAL, and variable lines for HD depending on HD resolution. Motion detection using only luminance level difference between two fields is very weak for pictures with spatial random noise. To remove the fake motion detected from the random noise, the TW5866 supports a spatial filter via the MD_SPSENS register which defines the number of detected cell to decide motion detection in full size image. The large MD_SPSENS value increases the immunity of spatial random noise.

Each detection cell has 4 sub-cells. The actual motion detection result of each cell comes from comparison of 4 sub-cells in it. The MD_CELSENS defines the number of detected sub-cell to decide motion detection in cell. That is, the large MD_CELSENS value increases the immunity of spatial random noise in detection cell.

Temporal Sensitivity

Similarly, temporal filter is used to remove the fake motion detection from the temporal random noise. The MD_TMPSENS regulates the number of taps in the temporal filter to control the temporal sensitivity so that the large MD_TMPSENS value increases the immunity of temporal random noise.

Velocity Control

A motion has various velocities. That is, in a fast motion an object appears and disappears rapidly between the adjacent fields while in a slow motion it is to the contrary.

As the built-in motion detection algorithm uses only the luminance level difference between two adjacent fields, a slow motion is harder to detect than a fast motion. To compensate this weakness, the current field is compared with a previous field up to 64-field time interval before. The MD_SPEED parameter adjusts the field interval in which the luminance level is compared. Thus, for detection of a fast motion a small value is needed and for a slow motion a large value is required. The parameter MD_SPEED value should be greater than MD_TMPSENS value.

Additionally, the TW5866 has 2 more parameters to control the selection of reference field. The MD_FLD register is a field selection parameter such as odd, even, any field or frame.

The MD_REFFLD register is used to control the updating period of reference field. For MD_REFFLD = “0”, the interval from current field to reference field is always same as the MD_SPEED. It means that the reference filed is always updated every field. The Figure 27 shows the relationship between current and reference field for motion detection when the MD_REFFLD is “0”.

The TW5866 can update the reference field only at the period of MD_SPEED when the MD_REFFLD is high. For this case, the TW5866 can detect a motion with sense of a various velocity. Figure 28 shows the relationship between current and reference field for motion detection when the MD_REFFLD = “1”.

The TW5866 also supports the manual detection timing control of the reference field/frame via the MD_STRB_EN and MD_STRB register. For MD_STRB_EN = “0”, the reference field/frame is automatically updated and reserved on every reference field/frame. For MD_STRB_EN = “1”, the reference field/frame is updated and reserved only when MD_STRB = “1”. In this mode, the interval between current and reference field/frame depends on user’s strobe timing. This mode is very useful for a specific purpose like non-periodical velocity control and very slow motion detection.

704 Pixels (44 Pixels/Cell)

240 Lines for 60Hz (20 Lines/Cell), 288 Lines for 50Hz (24 Lines/Cell)

MD_MASK0 [0]	MD_MASK0 [1]	MD_MASK0 [2]	MD_MASK0 [3]	MD_MASK0 [4]	MD_MASK0 [5]	MD_MASK0 [6]	MD_MASK0 [7]	MD_MASK0 [8]	MD_MASK0 [9]	MD_MASK0 [10]	MD_MASK0 [11]	MD_MASK0 [12]	MD_MASK0 [13]	MD_MASK0 [14]	MD_MASK0 [15]
MD_MASK1 [0]	MD_MASK1 [1]	MD_MASK1 [2]	MD_MASK1 [3]	MD_MASK1 [4]	MD_MASK1 [5]	MD_MASK1 [6]	MD_MASK1 [7]	MD_MASK1 [8]	MD_MASK1 [9]	MD_MASK1 [10]	MD_MASK1 [11]	MD_MASK1 [12]	MD_MASK1 [13]	MD_MASK1 [14]	MD_MASK1 [15]
MD_MASK2 [0]	MD_MASK2 [1]	MD_MASK2 [2]	MD_MASK2 [3]	MD_MASK2 [4]	MD_MASK2 [5]	MD_MASK2 [6]	MD_MASK2 [7]	MD_MASK2 [8]	MD_MASK2 [9]	MD_MASK2 [10]	MD_MASK2 [11]	MD_MASK2 [12]	MD_MASK2 [13]	MD_MASK2 [14]	MD_MASK2 [15]
MD_MASK3 [0]	MD_MASK3 [1]	MD_MASK3 [2]	MD_MASK3 [3]	MD_MASK3 [4]	MD_MASK3 [5]	MD_MASK3 [6]	MD_MASK3 [7]	MD_MASK3 [8]	MD_MASK3 [9]	MD_MASK3 [10]	MD_MASK3 [11]	MD_MASK3 [12]	MD_MASK3 [13]	MD_MASK3 [14]	MD_MASK3 [15]
MD_MASK4 [0]	MD_MASK4 [1]	MD_MASK4 [2]	MD_MASK4 [3]	MD_MASK4 [4]	MD_MASK4 [5]	MD_MASK4 [6]	MD_MASK4 [7]	MD_MASK4 [8]	MD_MASK4 [9]	MD_MASK4 [10]	MD_MASK4 [11]	MD_MASK4 [12]	MD_MASK4 [13]	MD_MASK4 [14]	MD_MASK4 [15]
MD_MASK5 [0]	MD_MASK5 [1]	MD_MASK5 [2]	MD_MASK5 [3]	MD_MASK5 [4]	MD_MASK5 [5]	MD_MASK5 [6]	MD_MASK5 [7]	MD_MASK5 [8]	MD_MASK5 [9]	MD_MASK5 [10]	MD_MASK5 [11]	MD_MASK5 [12]	MD_MASK5 [13]	MD_MASK5 [14]	MD_MASK5 [15]
MD_MASK6 [0]	MD_MASK6 [1]	MD_MASK6 [2]	MD_MASK6 [3]	MD_MASK6 [4]	MD_MASK6 [5]	MD_MASK6 [6]	MD_MASK6 [7]	MD_MASK6 [8]	MD_MASK6 [9]	MD_MASK6 [10]	MD_MASK6 [11]	MD_MASK6 [12]	MD_MASK6 [13]	MD_MASK6 [14]	MD_MASK6 [15]
MD_MASK7 [0]	MD_MASK7 [1]	MD_MASK7 [2]	MD_MASK7 [3]	MD_MASK7 [4]	MD_MASK7 [5]	MD_MASK7 [6]	MD_MASK7 [7]	MD_MASK7 [8]	MD_MASK7 [9]	MD_MASK7 [10]	MD_MASK7 [11]	MD_MASK7 [12]	MD_MASK7 [13]	MD_MASK7 [14]	MD_MASK7 [15]
MD_MASK8 [0]	MD_MASK8 [1]	MD_MASK8 [2]	MD_MASK8 [3]	MD_MASK8 [4]	MD_MASK8 [5]	MD_MASK8 [6]	MD_MASK8 [7]	MD_MASK8 [8]	MD_MASK8 [9]	MD_MASK8 [10]	MD_MASK8 [11]	MD_MASK8 [12]	MD_MASK8 [13]	MD_MASK8 [14]	MD_MASK8 [15]
MD_MASK9 [0]	MD_MASK9 [1]	MD_MASK9 [2]	MD_MASK9 [3]	MD_MASK9 [4]	MD_MASK9 [5]	MD_MASK9 [6]	MD_MASK9 [7]	MD_MASK9 [8]	MD_MASK9 [9]	MD_MASK9 [10]	MD_MASK9 [11]	MD_MASK9 [12]	MD_MASK9 [13]	MD_MASK9 [14]	MD_MASK9 [15]
MD_MASK10 [0]	MD_MASK10 [1]	MD_MASK10 [2]	MD_MASK10 [3]	MD_MASK10 [4]	MD_MASK10 [5]	MD_MASK10 [6]	MD_MASK10 [7]	MD_MASK10 [8]	MD_MASK10 [9]	MD_MASK10 [10]	MD_MASK10 [11]	MD_MASK10 [12]	MD_MASK10 [13]	MD_MASK10 [14]	MD_MASK10 [15]
MD_MASK11 [0]	MD_MASK11 [1]	MD_MASK11 [2]	MD_MASK11 [3]	MD_MASK11 [4]	MD_MASK11 [5]	MD_MASK11 [6]	MD_MASK11 [7]	MD_MASK11 [8]	MD_MASK11 [9]	MD_MASK11 [10]	MD_MASK11 [11]	MD_MASK11 [12]	MD_MASK11 [13]	MD_MASK11 [14]	MD_MASK11 [15]

FIGURE 26. MOTION MASK AND DETECTION CELLS FOR D1 CASE

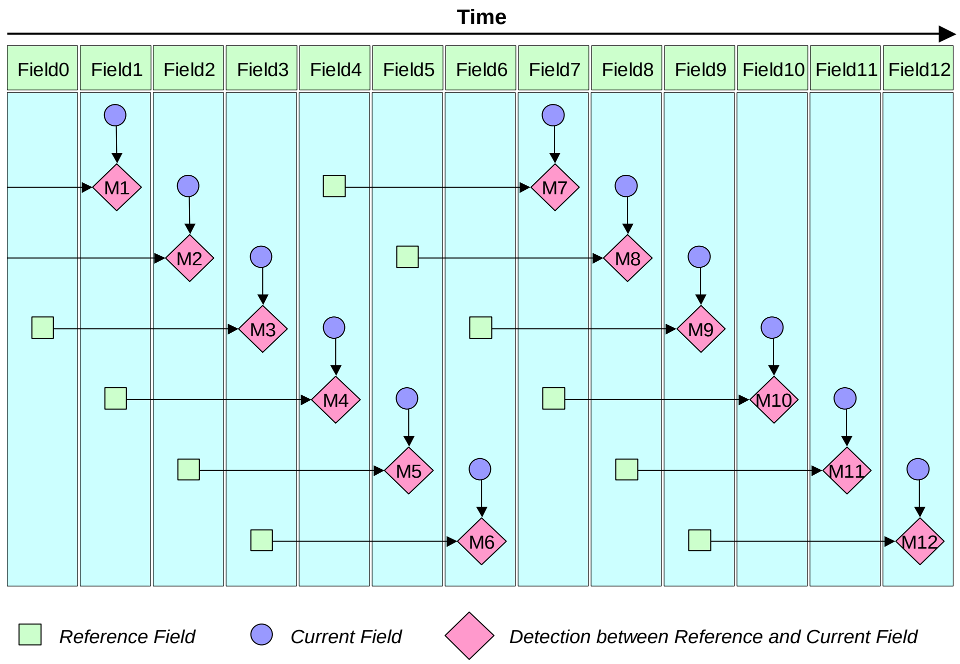


FIGURE 27. THE RELATIONSHIP BETWEEN CURRENT AND REFERENCE FIELD WHEN MD_REFFLD = “0”

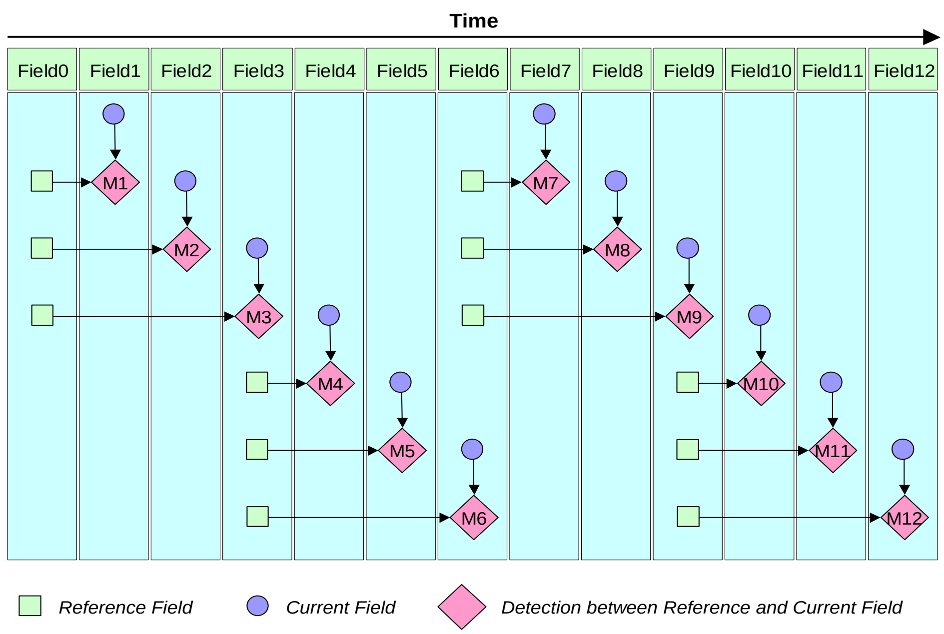


FIGURE 28. THE RELATIONSHIP BETWEEN CURRENT AND REFERENCE FIELD WHEN MD_REFFLD = “1”

Blind Detection

The TW5866 supports a blind detection for each of the 16 video inputs and generated an interrupt to the host when a blind condition is detected. A blind condition is detected when a camera is shaded / blocked by some unknown object and the video level in wide area of a field is almost equal to average video level of the field.

The TW5866 has two sensitivity parameters to detect blind input such as the level sensitivity via the BD_LVSENS register and spatial sensitivity via the BD_CELSENS register.

The TW5866 uses total 768 (30x224) cells in full screen for SD blind detection. The BD_LVSENS parameter controls the threshold of level between cell and field average. The BD_CELSENS parameter defines the number of cells to detect blind. For BD_CELSENS = “0”, the number of cell whose level is same as average of field should be over than 60% to detect blind, 70% for BD_CELSENS = “1”, 80% for BD_CELSENS = “2”, and 90% for BD_CELSENS = “3”. That is, the large value of BD_LVSENS and BD_CELSENS makes blind detector less sensitive. For HD case, the whole screen is treated as 4 SD areas, and the BD is detected individually.

The host can read blind detection information via MCU interrupt. When blind input is detected in any video inputs, the host processor can read the information by accessing the INTERRUPT_VECT registers. This status information is updated in the vertical blank period of each input.

Night Detection

The TW5866 supports night detection for each of the 16 video inputs and generates an interrupt to the host when a night condition is detected. If an average of a field video level is very low, this input is interpreted as night. Otherwise, the input is treated as day.

The TW5866 has two sensitivity parameters to detect night input such as the level sensitivity via the ND_LVSENS register and the temporal sensitivity via the ND_TMPSENS register. The ND_LVSENS parameter controls threshold level of day and night. The ND_TMPSENS parameter regulates the number of taps in the temporal low pass filter to control the temporal sensitivity. The large value of ND_LVSENS and ND_TMPSENS makes night detector less sensitive.

The host can read night detection information via the MCU interrupt. When night input is detected in any video inputs, the TW5866 provides the interrupt request to host via the IRQ pin. The host processor can read the information of night detection by accessing the INTERRUPT_VECT register. This status information is updated in the vertical blank period of each input.

H.264 Encoding Channel Capture

The TW5866 supports up to 16 channels of SD and 2 channels of HD real-time / non-real-time video for encoding simultaneously. Each of the 16 channels can be configured to capture picture size of either half D1 (720x288 / 720x240) or CIF (360x288 / 360x240), HD (1920x540, 1280x720), quarter HD (960x540, 640x360), H960 (960x240 / 960x288), quarter H960 (480x240 / 480x288), etc.

The capture module can be configured to capture both fields (odd and even) or just single field. For a full D1 / HD compression, both fields should be captured. For quarter D1 / HD compression, however, only a single field needs to be captured in order to support a frame size of 360x288 / 360x240 / 960x540 / 480x240 / 480x288.

There are 4 separate SD DDR write paths embedded in the H.264 capture module. The selection of channels in each path is as shown in Figure 29.

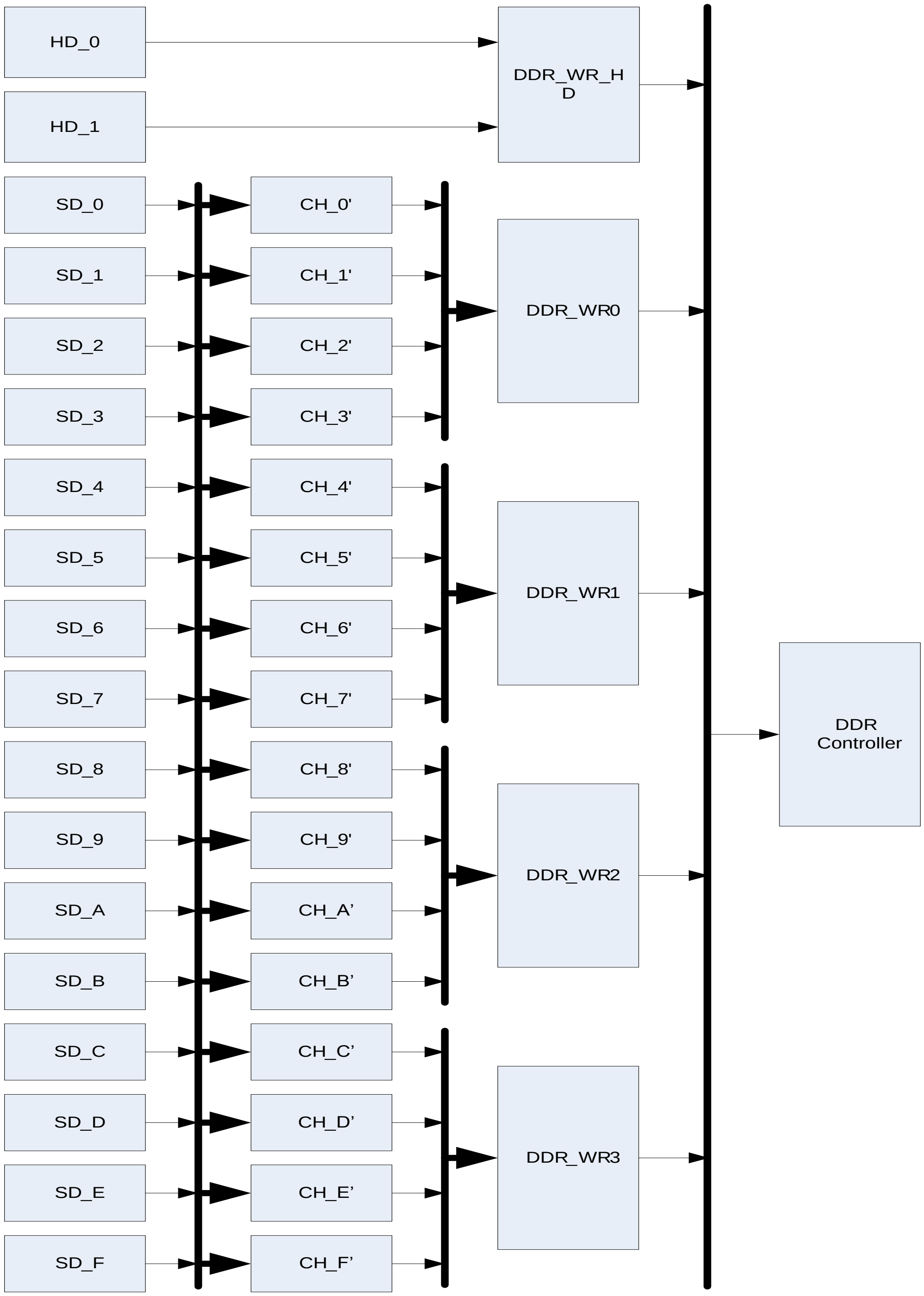


FIGURE 29. H.264 ENCODING CAPTURE PATH CHANNEL SELECTION

In the first stage (CH_0' ~ CH_F'), one channel out of the 16 incoming channels (CH_0 ~ CH_F) is selected. Every 4 channels of the first stage channels are grouped into one DDR write path. In order to encode 4 D1 + 4 CIF (4 CIF is 704 pixels wide where 4 CIF are 4 separate CIF (360x240) images) in H.264, the module will only captures up to 4 channels of real-time D1 video streams. Each DDR write path captures 1 channel of real-time D1 video. The secondary stream is automatically generated from the main stream by downscaling ½ in each of the horizontal and vertical direction. In order to support 16 D1 non-real-time encoding, the module captures all 16 channels in D1 resolution while sub-sampling at time domain. The sub-sampling rate is controlled by the external MCU through register settings.

Note that although each video channel can be individually configured with either D1 or Half D1 size, the total peak throughput of each DDR write path should not exceed 2 D1 channel bandwidth, except on the first write path where 1D1+3CIF can be supported. The higher peak bandwidth on the first write path allows TW5866 to support 1D1+15CIF channel configuration. Due to the peak bandwidth limitation on the write path, the selection of channels merged into the same DDR write path has to be carefully selected.

The HD channel capture is separate from SD capture.

MJPEG Encoding Channel Capture

TW5866 MJPEG engine is designed to support a low frame rate picture capture operation. When encoding multiple channels, it is time multiplexed between channels.

At least 1 F/S for each of 16 channels is supported in TW5866

>= 25 F/S overall encoding capability

At any time a maximum number of two frames can be captured simultaneously into DDR buffer for JPEG encoding

The TW5866 motion JPEG encoder supports two separate internal capture paths. Each capture path can select one channel out of any of the 16 incoming video channel at any instance of time. With this time sharing mechanism, the MJPEG module can support up to 1 D1 frame per second for each of the 16 channels.

The MJPEG capture modules select various picture sizes independently from channel to channel. The supported sizes are D1 (720x288 / 720x240) or CIF (360x288 / 360x240), HD (1920x540, 1280x720), quarter HD (960x540, 640x360), H960 (960x240 / 960x288), quarter H960 (480x240 / 480x288), etc. The capture module can be configured to capture either both odd and even fields, or only a single field out of a frame. Again, the HD picture capture is independent of SD paths.

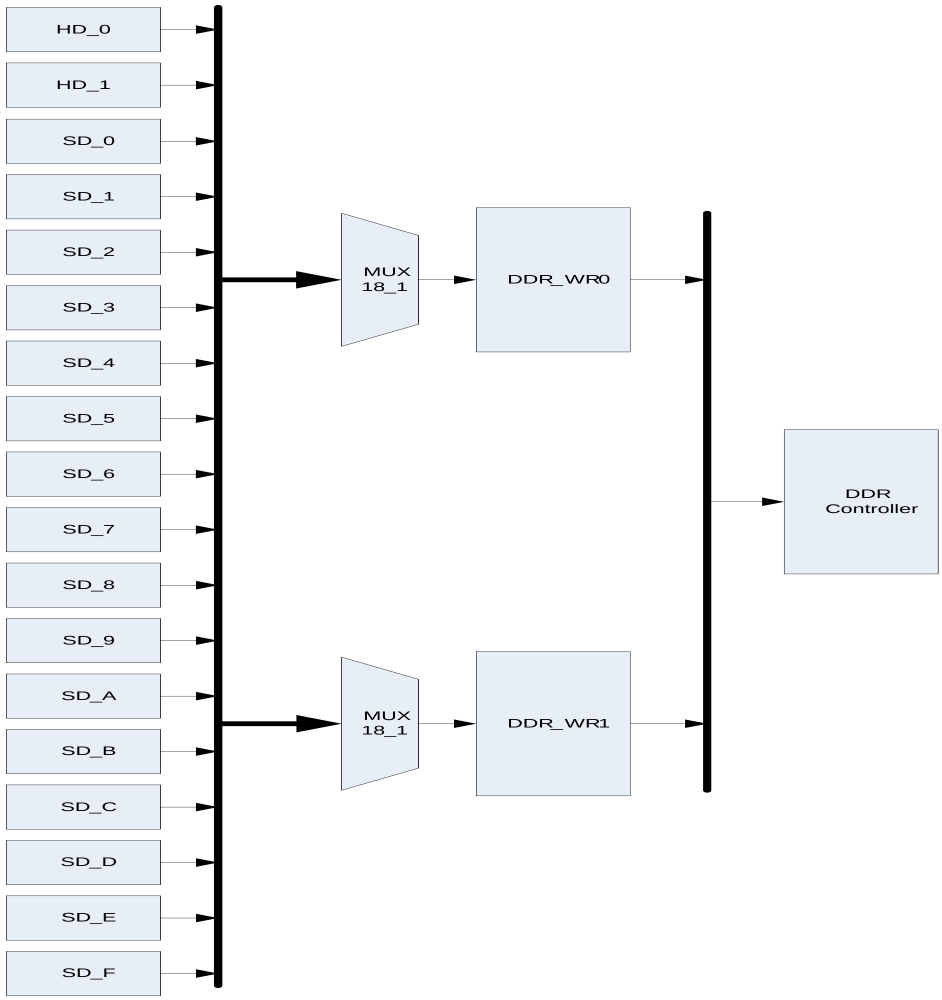


FIGURE 30. MJPEG ENCODING CAPTURE PATH CHANNEL SELECTION

PCI Preview Channel Selection

The PCI preview function is designed specifically for PC host application. PCI preview feature in TW5866 supports the following configuration.

- 8D1
- 2 720P
- 1 1080i
- 16 CIF / QCIF

All original video data in preview is sent from TW5866 to PC host in push mode. The maximum preview data being sent through PCI bus to PC host is bounded by the PCI bus bandwidth. The TW5866 SD PCI preview path supports 8 internal buffers BUF_0 ~ BUF_7 for sending the preview pictures onto the PCI bus. Each of the buffers is shared among any 4 channels selected out of 16 video channels. This is shown in Figure 31. At the input, there are total of 16 channels, from SD_0 through SD_F. Each of the first stage channel section output SD_0' through SD_F' can select one channel out of any of the 16 incoming channels. The second stage channel selection for input to BUF_0 selects one channel from SD_0' ~ SD_1' for D1 / CIF case, and SD_0' ~ SD_3' for QCIF case. BUF_1 with input from SD_2' ~ SD_3' for D1 / CIF case. Similarly with BUF_2/BUF_3, BUF_4/BUF5, or BUF_6/BUF_7. Each Buffer has a limitation of supporting up to 1 D1 channel, 2 CIF channels, or 4 QCIF channels.

The PCI preview path input pictures of D1, Half D1, CIF, and Half CIF for each individual channels. Since there are limitations on sharing the internal buffers, all channels going to the same buffer have to be of the same picture size, either CIF or QCIF.

The preview HD buffer is separate from SD buffers.

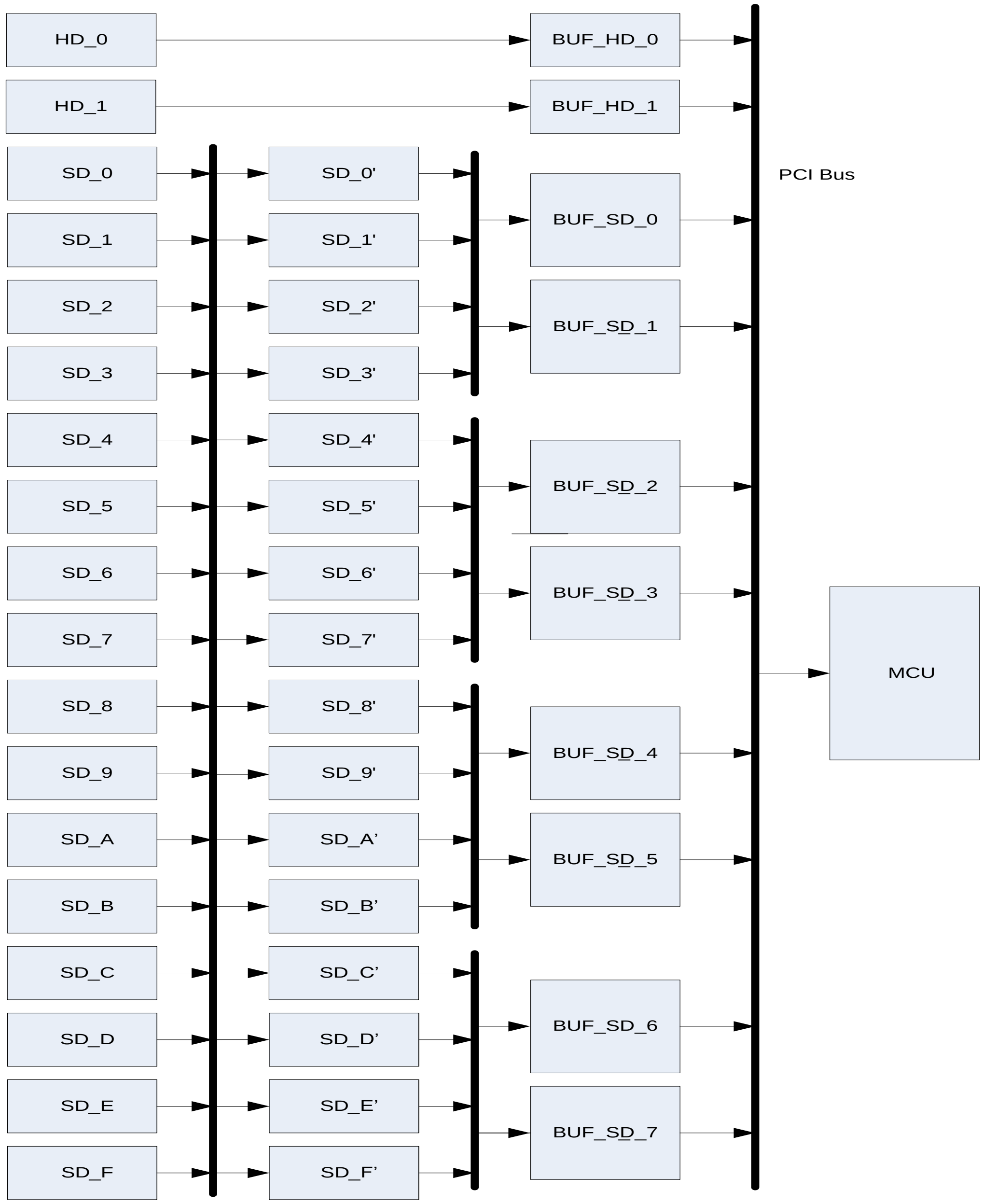


FIGURE 31. PCI PREVIEW PATH CHANNEL SELECTION

H.264 Encoding Module

DE-INTERLACERS

The TW5866 de-interlacer sitting right before H.264 encoder is an enhanced cost efficient de-interfacer that performs adaptive field weaving or 2D de-interlacing depending on the content motion. The de-interlacer works on a channel by channel base. Each of the channels can be independently controlled.

OSDS

The TW5866 supports pre-encoding OSD function which overlays fonts/graphics onto the video before H.264 encoding is performed. The OSD overlays onto each channel of video independently. For each channel, up to 8 windows are supported. Additionally, in order to support good quality in both main and secondary stream, two different sets of fonts can be overlaid onto the main / secondary streams independently.

H.264 ENCODERS

TW5866 has a build-in baseline H.264 encoder capable of encoding up to 9D1 in real-time. The H.264 encoder performance is summarized as the following:

- H.264 Baseline @ Level 3 encoding, without arbitrary slice ordering (ASO), flexible MB ordering (FMO), and redundant picture
- One slice per frame
- Bitrates from 64 kbps to 10 mbps
- Up to 9 D1 encoding at 30 frames per second (NTSC) or 25 frame per second (PAL)
- Support VBR / CBR
- Configurable IDR/I Interval
- Support intra-mode (16x16 and 4x4)
- Support variable block size (16x16, 16x8, and 8x8)
- Motion vector granularity at full-pel, ½ pel, and ¼ pel
- Motion vector range [-256, +255.75]
- In-loop deblocking filter
- CAVLC entropy coding
- Collect video analytic information to MPU
- Same channel dual-stream encoding (D1/CIF, D1/QCIF, or CIF/QCIF)

The typical configuration for multichannel encoding is given here as examples:

- 8 D1 main streams and 8 CIF/QCIF second streams
- 16 CIF main streams and 16 QCIF second streams
- 16 D1 sub-frame rate encoding with aggregated total encoding frames <=125 F/S
- N channel D1 and (16-N) channel CIF.

Note that when TW5866 is encoding more than 8 physical channels, it needs additional TW2866 equivalent video decoder.

H.264 CODED STREAM

TW5866 generates H.264 standard compliant base-line profile bitstream, decodable by 3rd party standard compliant decoder. TW5866 H.264 bitstream contains progressive I-frame and P-frame information, without arbitrary slice ordering, flexible MB-ordering and redundant picture feature supports.

TW5866 bitstream follows H.264 standard byte stream format by constructed from the NAL (Network Abstraction Layer) unit stream format in decoding order and prefixing each NAL unit with a start code prefix (0x00000001). For each NAL bitstream unit, zero-valued bits or zero-valued bytes are padded in the end of I-frame and P-frame payload data to form an unit of multiple of 4-byte in length.

The NAL unit stream format can be extracted from the byte stream format by searching for the location of the unique start code prefix pattern within this stream of bytes.

In TW5866 bitstream, a SPS (Sequence Parameter Set) and a PPS (Picture Parameter Set) NAL unit are proceeded each IDR (Instantaneous Decoding Refresh)-frame NAL. The following tables describe NAL unit, SPS and PPS syntax in tabular form.

TABLE 9. TW5866 NAL UNIT SYNTAX

NAL UNIT	VALUE(HEX)	BIT NUMBER
NalUnitStartCodePrefix	0x00000001	16
forbiden_zero_bit	0	1
nal_ref_idc	0x02	2
nal_unit_type	nal_unit_type_value	5
NAL payload		Variable
rbsp_trailing_bits( )		Insert zero-valued bit(s) to 32-bit aligned

TABLE 10 TW5866 SPS RBSP SYNTAX

SPS_PARAMETER_SET_RBSP (NAL_UNIT_TYPE=7)	VALUE(HEX)	BIT NUMBER
profile_idc	0x42	8
constraint_set0_flag	0	1
constraint_set1_flag	0	1
constraint_set2_flag	0	1
reserved_zero_5bits	0	5
level_idc	0x1E	8
seq_parameter_set_id	0	ue(v)
log2_max_frame_bun_minus4	0x0B	ue(v)
pic_order_cnt_type	0	ue(v)
log2_max_pic_order_cnt_lsb_minus4	0x0B	ue(v)
num_ref_frames	0x01	ue(v)
gaps_in_frame_num_value_allowed_flag	0	1
pic_width_in_mbs_minus1	(picWidth/16) -1)	ue(v)
pic_heigh_in_map_units_minus1	(picHeight/16) -1)	ue(v)
frame_mbs_only_flag	0x01	1
direct_8x8_inference_flag	0	1
frame_cropping_flag	0	1
vui_parameter_present_flag	0	1
rbsp_trailing_bits		Insert zero-valued bit(s) to 32-bit aligned

Audio A/D and D/A CODEC

The audio A/D and D/A codec of the TW5866 are composed of two sets of 5-channel audio codec as used in TW2866. Each of the two sets consists of 5 analog audio inputs, 1 Digital-to-Analog converter, audio mixer, digital serial audio interface and audio detector shown in Figure 32. The two sets are cascaded together into a 10-channel solution, shown in Figure 33.

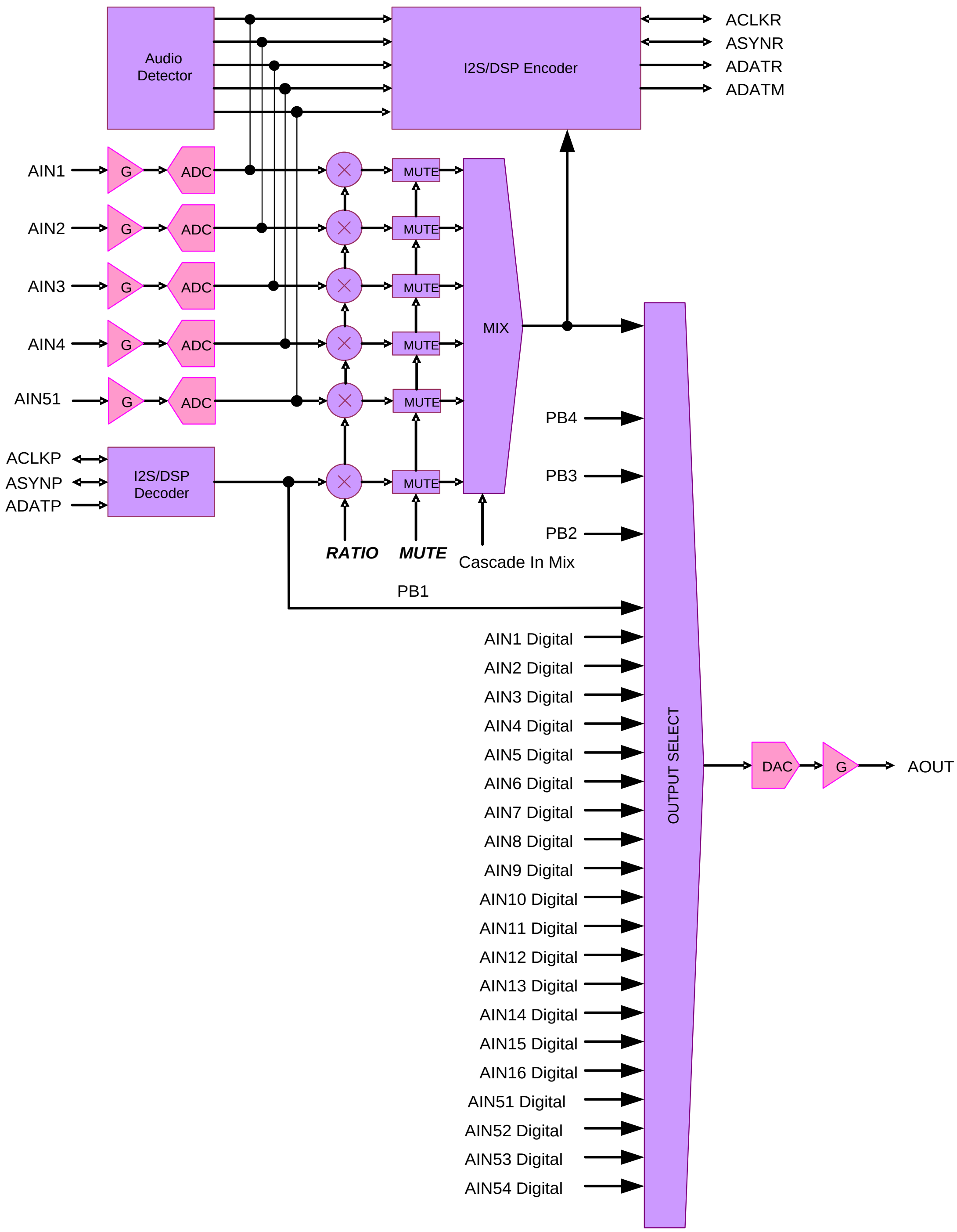


FIGURE 32.5-CHANNEL AUDIO CODEC UNITS IN TW2866

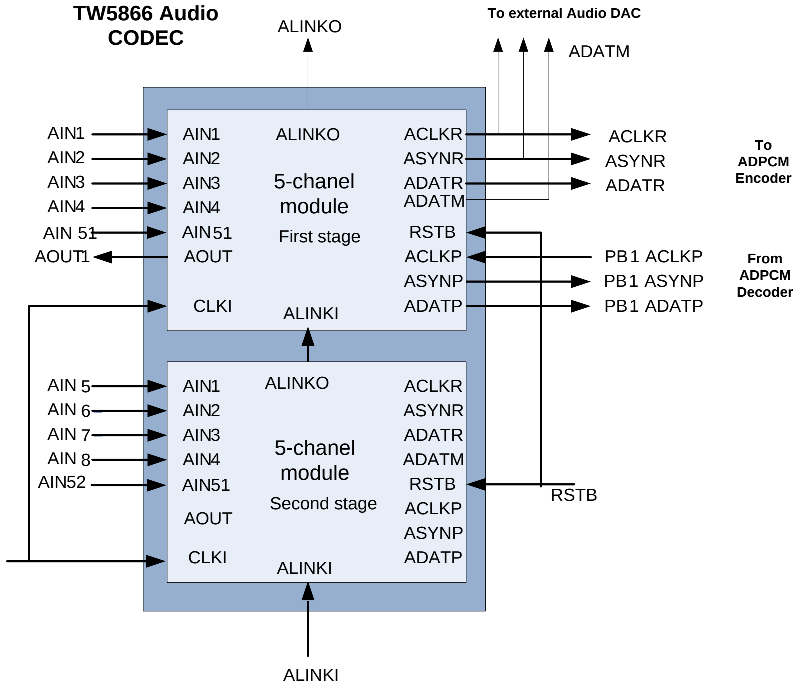


FIGURE 33. 10-CHANNEL AUDIO CODEC UNITS IN TW5866 CONSISTING OF TWO 5-CHANNEL AUDIO CODECS

The level of analog audio input signal AIN1 ~ AIN8, AIN51, AIN52 can be adjusted respectively by internal programmable gain amplifiers that are defined via the AADCGAIN1 ~ AADCGAIN8, AADCGAIN51, AADCGAIN52 registers (0xECD ~ 0xED2) and then sampled by each Analog-to-Digital converters. Figure 34 shows the audio decimation filter response. Audio playback channels from ADPCM decoder are fed into the internal ACLKP, ASYNP and ADATP interfaces. To record audio data, the TW5866 audio codec module provides the digital serial audio output via the ACLKR, ASYNR and ADATR port, and feed into the on-chip ADPCM audio encoding module.

The TW5866 can mix all of audio inputs including analog audio signal and digital audio data according to the predefined mixing ratio for each audio via the MIX_RATIO1 ~ MIX_RATIO8, MIX_RATIO51, MIX_RATIO52 and MIX_RATIOP registers. This mixing audio output can be provided through the analog and digital interfaces. The embedded audio Digital-to-Analog converter supports the analog mixing audio output whose level can be controlled by programmable gain amplifier via the A_DAC_AOGAIN register at 0xECB. The ADATM pin supports the digital mixing audio output and its digital serial audio timings are provided through the ACLKR and ASYNR ports that are shared with the digital serial audio record timing pins.

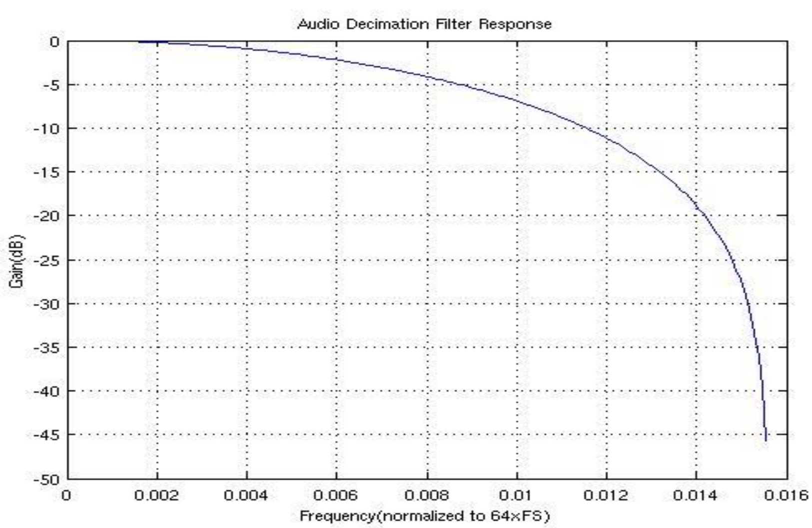
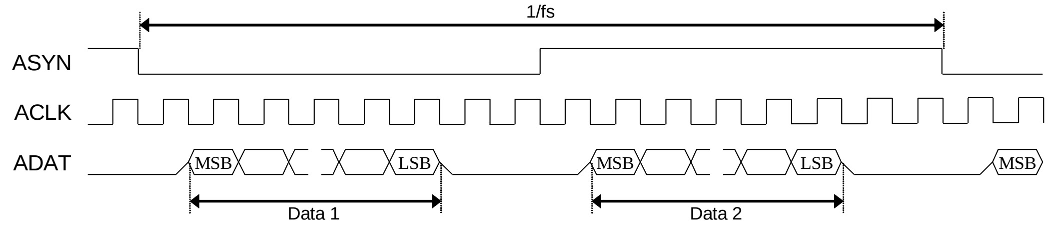
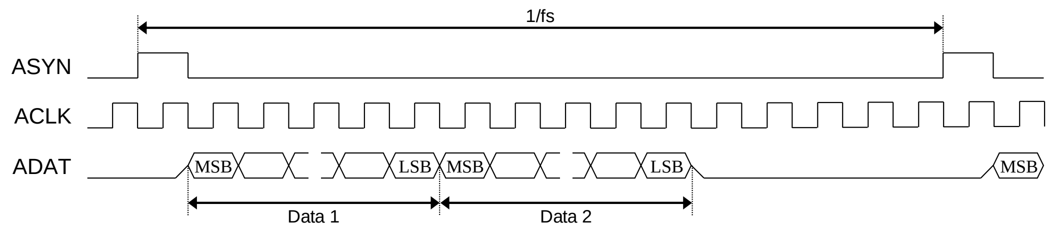


FIGURE 34. AUDIO DECIMATION FILTER RESPONSE



(A) I2S FORMAT



(B) DSP FORMAT

FIGURE 35. TIMING CHART OF SERIAL AUDIO INTERFACE

Serial Audio Interface

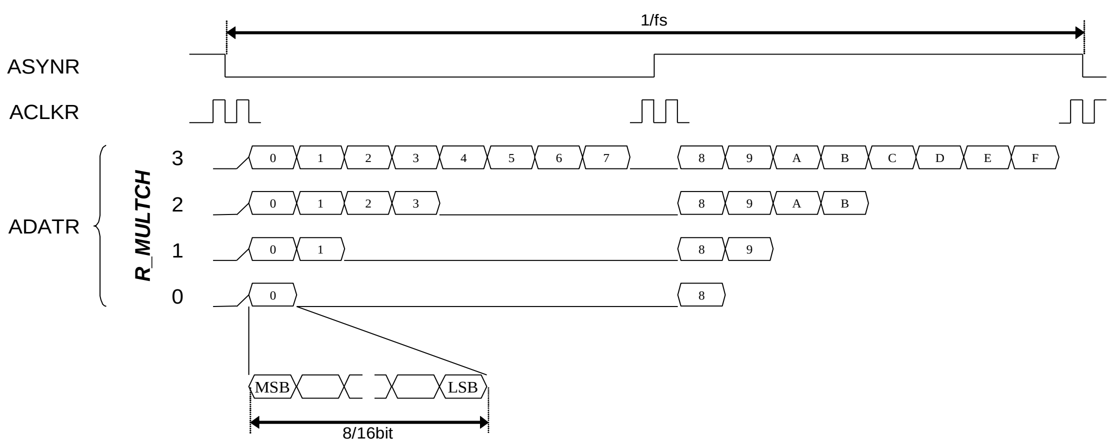
There are 3 kinds of digital serial audio interfaces in the TW5866, the first is a recording output, the second is a mixing output and the third is a playback input. These 3 digital serial audio interfaces follow a standard I2S or DSP interface as shown in Figure 35.

Playback Input

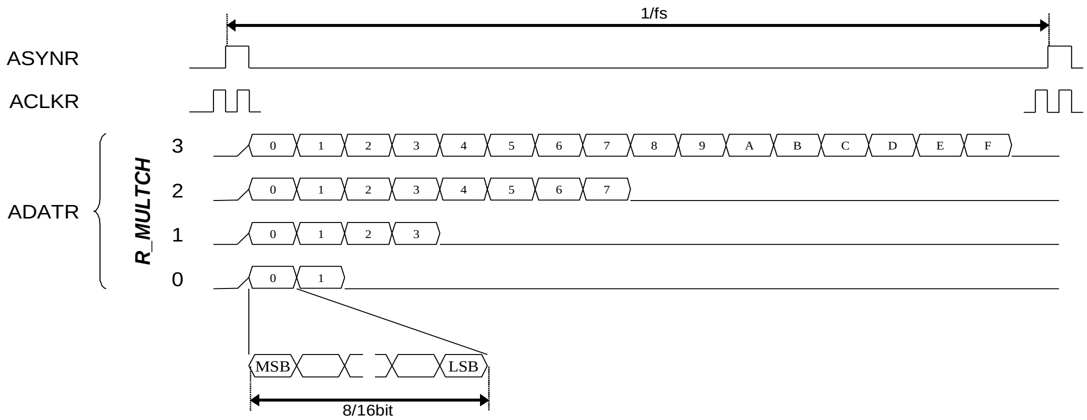
The serial interface using the ACLKP, ASYNP and ADATP pins accepts the digital serial audio data for the playback purpose. The ACLKP and ASYNP pins can be operated as master or slave mode. For master mode, these pins work as output pin and generate the standard audio clock and synchronizing signal. For slave mode, these pins are input mode and accept the standard audio clock and synchronizing signal. The ADATP pin is always input mode regardless of operating mode. In order to use the on-chip ADPCM decoder, the playback port has to run at the master mode. One of audio data in left or right channel should be selected for playback audio by the PB_LRSEL.

Record Output

To record audio data, the TW5866 provides the digital serial audio data through the ACLKR, ASYNR and ADATR ports. Sampling frequency comes from 256 x fs, 320 x fs, or 384 x fs audio system clock setting. Even though the standard I2S and DSP format can have only 2 audio data on left and right channel, the TW5866 can provide an extended I2S and DSP format which can have 16-channel audio data through ADATR pin. The R_MULTCH defines the number of audio data to be recorded by the ADATR pin. ASYNR signal is always fs frequency rate. One ASYNR period is always equal to 256 x ACLKR clock length with AIN5MD=0. Figure 36 shows the digital serial audio data organization for multi-channel audio.



(A) I2S FORMAT



(B) DSP FORMAT

FIGURE 36. TIMING CHART OF SERIAL AUDIO INTERFACE

The following table shows the sequence of audio data to be recorded for each mode of the R_MULTCH register. The sequences of 0 ~ F do not mean actual audio channel number but represent sequence only. The actual audio channel should be assigned to sequence 0 ~ F by the R_SEQ_0 ~ R_SEQ_F register. When the ADATM pin is used for record via the R_ADATM register, the audio sequence of ADATM is showed also in Table 11.

TABLE 11 DIGITAL PREVIEW VIDEO OUTPUT PORT 1 CONFIGURATION

(a) I2S Format

R_MULTCH	Pin	Left Channel								Right Channel							
0	ADATR	0								8							
	ADATM	F								7							
1	ADATR	0	1							8	9						
	ADATM	F	E							7	6						
2	ADATR	0	1	2	3					8	9	A	B				
	ADATM	F	E	D	C					7	6	5	4				
3	ADATR	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
	ADATM	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0

(b) DSP Format

R_MULTCH	Pin	Left/Right Channel															
0	ADATR	0	1														
	ADATM	F	E														
1	ADATR	0	1	2	3												
	ADATM	F	E	D	C												
2	ADATR	0	1	2	3	4	5	6	7								
	ADATM	F	E	D	C	B	A	9	8								
3	ADATR	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
	ADATM	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0

Mix Output

The digital serial audio data on the ADATM pin has 2 different audio data which are mixing audio and playback audio. The mixing digital serial audio data is the same as analog mixing output. The sampling frequency, bit width and number of audio for the ADATM pin are same as the ADATR pin because the ACLKR and ASYNR pins are shared with the ADATR and ADATM pins.

Audio Multi-Chip Cascade

TW5866 can up to 20 channel audio data (AIN5MD = 1) or 16 channel audio data (AIN5MD = 0) on ACLKR / ASYNR / ADATR to the back-end ADPCM module simultaneously. Therefore, 2 TW5866 chips or one TW5866 with two external TW2866 can be connected together. ALINKI pin is the audio cascade serial input, and ALINKO pin is the audio cascade serial output.

When AIN5MD= 0, each stage chip can accept 8 analog audio signals so that two cascaded chips will be 16-channel audio controller. In this case the first stage chip provides 16ch digital serial audio data for record, even though the first stage chip has only 1 digital serial audio data pin ADATR for record. Also the first stage chip can also output 16 channels mixing audio data at the ADATM output. The last stage chip accepts the digital serial audio data from on-chip ADPCM decoder for playback. The digital playback data can be converted to analog signal by Digital-to-Analog Converter in the last stage chip.

In Multi-Chip Audio operation mode, one same Oscillator clock source (27 MHz) needs to be connected to all TW5866 XTI or TW2866 CLKI pins.

If one TW5866 uses AIN5MD=1, all other cascaded TW5866 / TW2866 chips must set up AIN5MD=1 also. Generally, 8 audio input mode (AIN5MD=0) are most used in this cascade system.

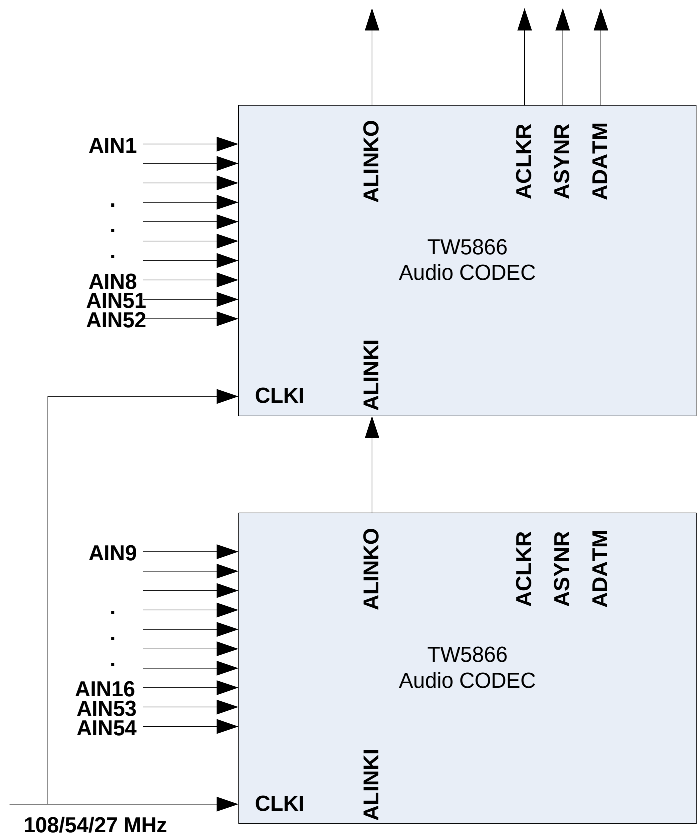


FIGURE 37. CASCADE OF TWO TW5866 TO SUPPORT 20 CHANNEL AUDIO

Audio Clock Generation

TW5866 has built-in field locked audio clock generator for use in video capture applications. The circuitry will generate the same predefined number of audio sample clocks per field to ensure synchronous playback of video and audio after digital recording or compression. The audio clock is digitally synthesized from the crystal clock input. The master audio clock frequency is programmable through ACKN and ACKI register based following two equations.

AUDIO MASTER CLOCK PER FIELD

ACKN = round (F AMCLK / F field)

AUDIO MASTER CLOCK NOMINAL INCREMENT

ACKI = round (F AMCLK / F 27MHz * 2^23)

Following table provides setting example of some common used audio frequency assuming Video Decoder system clock frequency of 27MHz. If ACLKRMASTER register bit is set to 1, following AMCLK is used as audio system clock inside TW5866.

If Slave Playback-in lock mode is required, ACKN=00100hex and PBREFEN=1 needs to be set up. The number of AMCLK clock per one ASYNP input cycle is locked (fixed) to 256 in this mode.

AMCLK (Freq) = 256 x ASYNP (Freq)

TABLE 12 AUDIO FREQUENCY 256XFS MODE: AIN5MD = 0, AFS384 = 0

AMCLK(MHz)	FIELD[Hz]	ACKN [dec]	ACKN [hex]	ACKI [dec]	ACKI [hex]
256 x 48 KHz					
12.288	50	245760	3-C0-00	3817749	3A-41-15
12.288	59.94	205005	3-20-CD	3817749	3A-41-15
256 x 44.1KHz					
11.2896	50	225792	3-72-00	3507556	35-85-65
11.2896	59.94	188348	2-DF-BC	3507556	35-85-65
256 x 32 KHz					
8.192	50	163840	2-80-00	2545166	26-D6-0E
8.192	59.94	136670	2-15-DE	2545166	26-D6-0E
256 x 16 KHz					
4.096	50	81920	1-40-00	1272583	13-6B-07
4.096	59.94	68335	1-0A-EF	1272583	13-6B-07
256 x 8 KHz					
2.048	50	40960	A0-00	636291	9-B5-83
2.048	59.94	34168	85-78	636291	9-B5-83

TABLE 13 AUDIO FREQUENCY 320XFS MODE: AIN5MD = 1, AFS384 = 0, 44.1/48 KHZ NOT SUPPORTED

AMCLK(MHz)	FIELD[Hz]	ACKN [dec]	ACKN [hex]	ACKI [dec]	ACKI [hex]
320 x 32 KHz					
10.24	50	204800	3-20-00	3181457	30-8B-91
10.24	59.94	170838	2-9B-56	3181457	30-8B-91
320x16 KHz					
5.12	50	102400	1-90-00	1590729	18-45-C9
5.12	59.94	85419	1-4D-AB	1590729	18-45-C9
320 x 8 KHz					
2.56	50	51200	C8-00	795364	C-22-E4
2.56	59.94	42709	A6-D5	795364	C-22-E4

TABLE 14 AUDIO FREQUENCY 384XFS MODE: AIN5MD = 0, AFS384 = 1, 44.1/48 KHZ NOT SUPPORTED

AMCLK(MHz)	FIELD[Hz]	ACKN [dec]	ACKN [hex]	ACKI [dec]	ACKI [hex]
384 x 32 KHz					
12.288	50	245760	3-C0-00	3817749	3A-41-15
12.288	59.94	205005	3-20-CD	3817749	3A-41-15
384x16 KHz					
6.144	50	122880	1-E0-00	1908874	1D-20-8A
6.144	59.94	102503	1-90-67	1908874	1D-20-8A
384 x 8 KHz					
3.072	50	61440	F0-00	954437	E-90-45
3.072	59.94	51251	C8-33	954437	E-90-45

TABLE 15 AUDIO FREQUENCY AUTO SETUP

AFAUTO	AFMD	ACKG module ACKI control input value
1	0	8kHz mode value by each AIN5MD/AFS384 case.
1	1	16kHz mode value by each AIN5MD/AFS384 case.
1	2	32kHz mode value by each AIN5MD/AFS384 case.
1	3	44.1kHz mode value by each AIN5MD/AFS384 case.
1	4	48kHz mode value by each AIN5MD/AFS384 case.
0	X	ACKI register set up ACKI control input value.

Audio Clock Auto Setup

If ACLKRMASTER=1 audio clock master mode is selected, and AFAUTO register is set to “1”,TW5866 set up ACKI register by AFMD register value automatically. ACKI control input in audio clock generation (ACKG) block is automatically set up to the required value by the condition of AIN5MD and AFS384 register value.

Digital Audio Encoding / Decoding

TW5866 provides a simple ADPCM G.726 hardware CODEC, mainly for speech coding purpose. It is used to map a series of 8-bit u-law (or a-low) PCM samples into a series of 4-bit ADPCM samples.

The ADPCM encoder takes the I2S format audio samples from the on-chip front-end audio analog decoder as well as the off-chip audio input through the I2S input ports. The ADPCM encoder is capable of encoding 17 audio channels simultaneously.

The ADPCM decoder decodes the 4-bit samples back into the I2S format, and drives the on-chip audio DAC to drive the external speaker or pre-amplifier for playback purpose. The decoder can decode only 1 audio channel at a time.

Host Interfaces

TW5866 supports two types of host interfaces, through which external processors control and interact with TW5866 for configuration and data transfer. One is through the standard asynchronous memory bus interface, and the other is through the PCI interface working at either the target or the initiator mode, depending on the operation. While using as a PC card, the PCI interface is always used. In an embedded system, either asynchronous host interface or the PCI interface can be used. TW5866 has the same registers map for these two interfaces so that the firmware on embedded platform does not need to differentiate which interface is in use except the bus control modules in TW5866 driver.

These two interfaces share some common I/O pins, and can only be used exclusively. The interrupt signal is also shared for both PCI and the asynchronous interface.

The host interface supports several modes: single read / write access, burst read / write access, DDR burst read / write, and PCI initiator write access.

PCI Interface

The PCI module in TW5866 will work both as an initiator and target. It is an initiator when it is sending the preview, H.264 and audio coded streams to host PC. It is in target mode when PC host is configuring the registers and programming the chip. The PCI interface supports both 33MHz and 66MHz operation.

SINGLE READ / WRITE

Similar to the asynchronous host interface, the TW5866 PCI interface supports the single read/write operation. The address space mapping and the entire indirect access / DDR memory page are used the same way as the asynchronous host interface. Similarly to the asynchronous host interface, the single R/W access runs in the PCI target mode, which makes the TW5866 a slave device to the external MCU.

TARGET BURST READ / WRITE

The PCI target burst read of TW5866 allows the external MCU to burst read a whole block of data of a continuous address space from TW5866. This target burst read function is only used to access the TW5866 on-chip double buffer A. The double buffer A is only used for DMA movement between the external DDRs and TW5866.

In order to burst read a space of an external DDR memory, a DMA operation is started to read data from external DDR into the double buffer A. The MCU then issues target burst read operation to read data from the double buffer A into the MCU.

A DMA write operation to the external DDR is supported. The MCU burst write into the buffer A, then a DMA write operation is started to write the data in double buffer A into the external DDR.

MASTER BURST WRITE

The TW5866 PCI interface can act as a PCI initiator to burst write a block of data automatically into the memory space of the external MCU. This master burst write function is used by several modules – H.264 encoder, the audio ADPCM encoder, JPEG encoder, and the PCI preview module. When this mode is used, the bitstream or data sent by each module does not go through the external DDR. They are sent from each module into a buffer for each path, and push into the external MCU memory space.

Asynchronous Interface

In addition to the PCI host interface, TW5866 also support commonly used Asynchronous Interface. The most commonly used ARM and PPC processors are supported. The data width is 32bit.

Asynchronous host interface only supports single access read and write operation. Using this interface, the TW5866 is always slave to the external MCU. The MCU issue single word read/write operation to access all registers / memory space inside the address map.

The address space of this asynchronous host interface is the same as the PCI interface. It includes all the on-chip registers, a page of space mapped for the external DDR, and an indirect access mechanism to read/write the registers at the front-end video / audio decoder registers and external preview multiplexing control registers.

The external DDRs are mapped into a page of address space through a page select register. Each page is 512 Kbytes. The page select register select a page area in either of the external DDRs such that accessing to this address space is equivalent to access the external DDR directly.

Although the asynchronous host interface only supports single word read / writes operation, a block move is possible as long as the external MCU has a DMA controller to access a block of address space continuously though multiple single access automatically.

External DRAM Interface

TW5866 uses two external DDR SDRAMs for various functions. The memory controller of the TW5866 supports 16bit data width up to 333 MHz clock rate. The memory capacity is 512 Mbytes. The capacity used depends on the feature used on TW5866. If the TW5866 is used for 4 D1 / 16 CIF configuration, and minimum capacity of 256 Mbytes can be used. If, however, a 16 non-real-time D1 configuration is used, a much bigger video frame buffer is needed. At this time DDR of 4 Bytes of memory is needed.

When the chip is powered up, the CPU is responsible for setting all the on-chip configuration registers for DDR memory configuration. Once the registers are set, the CPU releases the software reset signal, then the DDR memory controller initializes the DDR memory configuration using the parameters in the registers. After the initialization is done, the DDR memory is ready for use. After the initialization, the memory controller does the memory refresh automatically.

Register Descriptions

0x0000 ~ 0x3FFF: H.264 Codec Control

Address	[15:0]
0x0000	H264REV

H264REV The Version register for H264 core (Read Only)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x0004	RESERVED							
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	H264_sub_version							

H264_sub_version Sub version of H264 (Read only)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x000C	RESERVED			MAS_SLICE_END	RESERVED			VLC_SLICE_END
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	START_NSLICE	RESERVED						

VLC_SLICE_END VLC Slice End Flag (Read Only)

MAS_SLICE_END Master Slice End Flag (Read Only)

START_NSLICE Host CPU to start a new slice

Address	[15:0]
0x0010	ENC_BUF_PTR_REC[15:0]
0x004C	ENC_BUF_PTR_REC[31:16]

ENC_BUF_PTR_REC Last Encoded Frame Buffer Pointer of channel 0 ~ 15. Two bit each channel.

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x0018			DSP_MB_QP					
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	DSP_LPF_OFFSET							

DSP_MB_QP H264 QP Value for codec

DSP_LPF_OFFSET H264 LPF_OFFSET (Default 0)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x001C	HD1_MAP_MD	CIF_MAP_MD	Reserved					DSP_CODEC_MODE
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
						MV_FLAG_VLD	MV_VECT_VLD	VLC_VLD

DSP_CODEC_MODE	0	Encode (Default)
	1	Decode
CIF_MAP_MD	0	4CIF in 1 MB
	1	1CIF in 1 MB
HD1_MAP_MD	0	2 half D1 in 1 MB
	1	1 half D1 in 1 MB
VLC_VLD	VLC Stream valid	
	0	Invalid
	1	Valid
MV_VECT_VLD	MV Vector Valid	
	0	Invalid
	1	Valid
MV_FLAG_VLD	MV Flag Valid	
	0	Invalid
	1	Valid

Address	[15:0]
0x0028	SEN_EN_CH

SEN_EN_CH[n] Original frame capture enable for channel 0 ~ 15

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x002C		DSP_FLW_CNTL	Reserved	DSP_MB_WAIT	DSP_CODEC_CHN			
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
					DSP_MB_DELAY			

DSP_CODEC_CHN The ID for channel selected for H264 encoding / decoding operation

DSP_MB_WAIT Control for MB delay. See description below.

DSP_FLW_CNTL VLC Flow Control Enable

- 0 Disable
- 1 Enable

DSP_MB_DELAY If DSP_MB_WAIT == 0, the MB delay is

DSP_MB_DELAY * 16

If DSP_MB_WAIT == 1, the MB delay is

DSP_MB_DELAY * 128

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x0030	DDR_PAGE_CNT[7:0]							
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	DDR_MODE	DDR_AB_SEL	DDR_BRST_EN					DDR_PAGE_CNT[8]

DDR_PAGE_CNT DDR single access page number

DDR_BRST_EN DDR-DPR burst read enable

- 1 Enable
- 0 Disable

DDR_AB_SEL DDR A/B Select as HOST access

Always set to 0

DDR_MODE DDR Access Mode Select

- 0 Single R/W Access (Host <-> DDR)
- 1 Burst R/W Access (Host <-> on-chip buffer)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x0034	Reserved				SENIF_SKIP	Reserved		
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	Reserved							

SENIF_SKIP Senif free running mode

0 Senif pointer adjust by SW(default)

1 Senif free running

Address	[15:0]
0x0038	SENIF_ORG_FRM_PTR [15:0]
0x003C	SENIF_ORG_FRM_PTR [31:16]

SENIF_ORG_FRM_PTR The Original Frame Capture Buffer Pointer for channel 0 ~ 15. Two bit for each channel.

Address	[15:0]
0x0010	ENC_BUF_PTR_REC[15:0]
0x004C	ENC_BUF_PTR_REC[31:16]

ENC_BUF_PTR_REC Last Encoded Frame Buffer Pointer of channel 0 ~ 15. Two bit each channel.

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x0050	FRAME_DELAY_VALUE[7:0]							
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
					FRAME_DELAY_ENB	FRAME_DELAY_VALUE[10:8]		

FRAME_DELAY_VALUE Frame end delay value

FRAME_DELAY_ENB Frame delay Enable

1 Enable

0 Disable (default)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x0060	CH3_MV_PTR		CH2_MV_PTR		CH1_MV_PTR		CH0_MV_PTR	
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	CH7_MV_PTR		CH6_MV_PTR		CH5_MV_PTR		CH4_MV_PTR	
0x0064	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
	CHB_MV_PTR		CHA_MV_PTR		CH9_MV_PTR		CH8_MV_PTR	
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	CHF_MV_PTR		CHE_MV_PTR		CHD_MV_PTR		CHC_MV_PTR	

CHn_MV_PTR **Current MV Flag Status Pointer for channel n. (Read only)**

Address	[15:0]
0x0068	RST_MV_PTR

RST_MV_PTR[n] **Reset Current MV Flag Status Pointer for Channel n.**

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x0070	ENC_I4x4_WIN_DELAY[7:0]							
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	ENC_I4x4_WIN_DELAY[15:8]							

ENC_I4x4_WIN_DELAY **Intra4x4 win delay in encode mode**

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x0074	DEC_I4x4_WIN_DELAY[7:0]							
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	DEC_I4x4_WIN_DELAY[15:8]							

DEC_I4x4_WIN_DELAY **Intra4x4 win delay in decode mode**

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x0200	DSP_DWN_Y		DSP_DWN_X		Reserved	DI_MD	DI_EN	Reserved
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	Reserved							DUAL_STR

DI_EN Deinterlacer Enable (1 to enable)

DI_MD De-interlacer Mode

1 Shuffled frame

0 Normal Un-Shuffled Frames

DSP_DWN_X Down scale original frame in X direction

11: Un-used

10: down-sample to ¼

01: down-sample to ½

00: down-sample disabled

DSP_DWN_Y Down scale original frame in Y direction

11: Un-used

10: down-sample to ¼

01: down-sample to ½

00: down-sample disabled

DUAL_STR 1 Dual Stream

0 Single Stream

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x0204	DSP_WIN_SIZE[3:0]				DSP_REF_FRM			
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
							DSP_WIN_SIZE[5:4]	

DSP_REF_FRM Number of reference frames (Default 1)

DSP_WIN_SIZE Window size

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x0208	DSP_SKIP_OFEN	DSP_SKIP_OFFSET						
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
		RESERVED						

DSP_SKIP_OFEN   Skip Offset Enable bit

0   DSP_SKIP_OFFSET value is not used (default 8)

1   DSP_SKIP_OFFSET value is used in HW

DSP_SKIP_OFFSET   Skip mode cost offset (default 8)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x020C		SRCH_OPT		SKIP_EN	INTRA_EN	ME_EN	HPEL_EN	QPEL_EN

QPEL_EN   Enable quarter pel search mode

HPEL_EN   Enable half pel search mode

ME_EN   Enable motion search mode

INTRA_EN   Enable Intra mode

SKIP_EN   Enable Skip Mode

SRCH_OPT   Search Option (Default 2'b01)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x0210						DSP_ENC_REF_PTR		
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
		DSP_REC_BUF_PTR						

DSP_ENC_REF_PTR   Reference Buffer Pointer for encoding

DSP_REC_BUF_PTR   Reconstruct Buffer pointer

Address	[15:0]
0x0214	DSP_REF_MVP_LAMBDA

DSP_REF_MVP_LAMBDA   Lambda Value for H264

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x0218		DSP_PIC_MAX_MB_Y						
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
		DSP_PIC_MAX_MB_X						

DSP_PIC_MAX_MB_Y The MB number in Y direction of a frame

DSP_PIC_MAX_MB_X The MB number in X direction of a frame

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x021C								
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
		DSP_ENC_ORG_PTR						

DSP_ENC_ORG_PTR The original frame pointer for encoding

Address	[15:0]
0x0220	DSP_OSD_ATTRI_BASE

DSP_OSD_ATTRI_BASE DDR base address of OSD rectangle attribute data

Address	[15:0]
0x0228	DSP_OSD_ENABLE

DSP_ OSD_ENABLE OSD enable bit for each channel

Address	[15:0]
0x0280 -0x02FC	ME_MV_VEC

0x0280 ~ 0x029C – Motion Vector for 1st 4x4 Block, e.g., 80 (X), 84 (Y)
0x02A0 ~ 0x02BC – Motion Vector for 2nd 4x4 Block, e.g., A0 (X), A4 (Y)
0x02C0 ~ 0x02DC – Motion Vector for 3rd 4x4 Block, e.g., C0 (X), C4 (Y)
0x02E0 ~ 0x02FC – Motion Vector for 4th 4x4 Block, e.g., E0 (X), E4 (Y)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x040C			DSP_I4x4_OffSet					
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]

DSP_I4x4_OffSet if (intra16x16_cost < (intra4x4_cost+dsp_i4x4_offset))
Intra_mode = intra16x16_mode
Else
Intra_mode = intra4x4_mode

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x0410		DSP_INTRA_MODE[2:0]						
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]

DSP_INTRA_MODE
0x5 Only 4x4
0x6 Only 16x16
0x7 16x16 & 4x4
Others Reserved

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x0414			DSP_I4x4_WEIGHT[5:0]					
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]

DSP_I4x4_WEIGHT WEIGHT Factor for I4x4 cost calculation
(QP dependent)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x0604	DSP_RESID_MODE_OFFSET							
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	RESERVED							

DSP_RESID_MODE_OFFSET Offset used to affect Intra/ME model decision
If (me_cost < intra_cost + dsp_resid_mode_offset)
Pred_Mode = me_mode
Else
Pred_mode = intra_mode

Address	[15:0]
0x0800--x09FF	QUAN_TABLE

QUAN_TABLE Quantization TABLE Values

Address	[15:0]
0x0Cn0	RT_CNTR_CHn_FRM0
0x0Cn4	RT_CNTR_CHn_FRM1
0x0Cn8	RT_CNTR_CHn_FRM2
0x0CnC	RT_CNTR_CHn_FRM3

RT_CNTR_CHn_FRM0	Real-time counter of frame 0 Channel n (n is from 0 to 15)
RT_CNTR_CHn_FRM1	Real-time counter of frame 1 Channel n (n is from 0 to 15)
RT_CNTR_CHn_FRM2	Real-time counter of frame 2 Channel n (n is from 0 to 15)
RT_CNTR_CHn_FRM3	Real-time counter of frame 3 Channel n (n is from 0 to 15)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x0D00				BUS1_D1		FRAME_1	PROG_1B	PROG_1A
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
				BUS2_D1		FRAME_2	PROG_2B	PROG_2A
0x0D04	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
				BUS3_D1		FRAME_3	PROG_3B	PROG_3A
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
				BUS4_D1		FRAME_4	PROG_4B	PROG_4A

PROG_nA	1	Progressive in part A on bus n
	0	Interlaced in part A on bus n
PROG_nB	1	Progressive in part B on bus n
	0	Interlaced in part B on bus n
FRAME_n	1	Frame Mode on bus n
	0	Field Mode on bus n
BUSn_D1	0	4CIF on bus n
	1	1D1 + 3 CIF on bus n
	3	2D1 on bus n

Note: there are two attributes in one bus (part A and part B)

For example: 1 2D1 in one bus, then part A is D1 mode, part B is D1 mode

2 1D1 + 3CIF in one bus, then part A is D1 mode, part B is CIF mode.

3 4CIF in one bus, then part A is CIF mode, part B is CIF mode

Address	[15:0]
0x0D08	SENIF_HOR_MIR
0x0D0C	SENIF_VER_MIR

SENIF_HOR_MIR[n] 1 Horizontal Mirror for channel n
0 Normal

SENIF_VER_MIR[n] 1 Vertical Mirror for channel n
0 Normal

Address	[9:0]
0x0D10	FRAME_WIDTH_BUS0_A
0x0D14	FRAME_WIDTH_BUS0_B
0x0D18	FRAME_HEIGHT_BUS0_A
0x0D1C	FRAME_HEIGHT_BUS0_B
0x0D20	FRAME_WIDTH_BUS1_A
0x0D24	FRAME_WIDTH_BUS1_B
0x0D28	FRAME_HEIGHT_BUS1_A
0x0D2C	FRAME_HEIGHT_BUS1_B
0x0D30	FRAME_WIDTH_BUS2_A
0x0D34	FRAME_WIDTH_BUS2_B
0x0D38	FRAME_HEIGHT_BUS2_A
0x0D3C	FRAME_HEIGHT_BUS2_B
0x0D40	FRAME_WIDTH_BUS3_A
0x0D44	FRAME_WIDTH_BUS3_B
0x0D48	FRAME_HEIGHT_BUS3_A
0x0D4C	FRAME_HEIGHT_BUS3_B

FRAME_WIDTH_BUSn_A 0x15F: 4 CIF
0x2CF: 1 D1 + 3 CIF
0x2CF: 2 D1

FRAME_WIDTH_BUSn_B 0x15F: 4 CIF
0x2CF: 1 D1 + 3 CIF
0x2CF: 2 D1

FRAME_HEIGHT_BUSn_A 0x11F: 4CIF (PAL)
0x23F: 1D1 + 3CIF (PAL)
0x23F: 2 D1 (PAL)

0x0EF: 4CIF (NTSC)
0x1DF: 1D1 + 3CIF (NTSC)
0x1DF: 2 D1 (NTSC)

FRAME_HEIGHT_BUSn_B 0x11F: 4CIF (PAL)
0x23F: 1D1 + 3CIF (PAL)
0x23F: 2 D1 (PAL)

0x0EF: 4CIF (NTSC)
0x1DF: 1D1 + 3CIF (NTSC)
0x1DF: 2 D1 (NTSC)

Address	[15:0]
0x0D50	FULL_HALF_FLAG

FULL_HALF_FLAG 1 The bus mapped channel n Full D1
0 The bus mapped channel n Half D1

Address	[15:0]
0x0D54	PART_A_B_MODE_SEL

PART_A_B_MODE_SEL[n] 0: Channel[n] select part A on one bus
1: Channel[n] select part B on one bus

Note: this is used only when 2D1 in one bus: If PART_A_B_MODE_SEL[3:2] = 2'b10 && channel 2 mapped to bus1 && channel 3 mapped to bus3, Then channel[2] select part A attribute in bus1, channel[3] select part B attribute in bus3.

VLCE REGISTERS

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x1000	VLC_ADD03_EN	VLC_STR_SWAP	VLC_SLICE_QP[5:0]					
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	VLC_PCI_SEL	VLC_FLOW_CNTL	RESERVED	VLC_BIT_ALIGN				
	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
	ENC_MD_EN	RESERVED			VLCE_HD_EN	RESERVED		VLC_HEAD_NO03
	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]
	RESERVED							

VLC_SLICE_QP — QP initial value of this slice.

VLC_STR_SWAP — Swap encode bit stream when send to SW.

VLC_ADD03_EN — Enable or disable hardware insert 0x03 header into bitstream

VLC_BIT_ALIGN — Bit number consumed by SW when SW encode slice header.

VLC_FLOW_CNTL — Enable monitoring the bit stream overflow status, set to 1.

VLC_PCI_SEL — 1 Use PCI interface to send
0 Others

VLC_HEAD_NO03 — Force HW insert 0x03 function ignore insert 0x03 for slice header.

VLCE_HD_EN — Enable HW encoder slice header.

ENC_MD_EN — Enable sends out Meta data information through PCI bus.

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x1004	SILICE_BIT_LEN[7:0]							
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	SLICE_BIT_LEN[15:8]							
	[23]	[22]	[21]	[20]	[18]	[18]	[17]	[16]
	SLICE_BIT_LEN[23:16]							
	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]
	SLICE_BIT_LEN[31:24]							

SLICE_BIT_LEN — Total bit number consumed by current slice.

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x1008	RES_BIT_LEN[7:0]							
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	RES_BIT_LEN[15:8]							
	[23]	[22]	[21]	[20]	[18]	[18]	[17]	[16]
	RES_BIT_LEN[23:16]							
	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]
	RES_BIT_LEN[31:24]							

RES_BIT_LEN Residual consumed bit stream length.

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x100C	VLC_RES_STREAM_LEN[3:0]				VLC_BUF_OFLW	END_SLICE	BK1_FUL	BK0_FUL
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	RESERVED	VLC_RES_STREAM_LEN[10:4]						
	[23]	[22]	[21]	[20	[18]	[18]	[17]	[16]
	RESERVED							
	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]
	DSP_OV_DBG	VLCE_END_DBG	RESERVED					

BK0_FUL VLC encoder stream buffer bank 0 full

BK1_FUL VLC encoder stream buffer bank 1 full

END_SLICE VLC encoder end slice

VLC_BUF_OFLW VLC encoder stream buffer overflow flag

VLC_RES_STREAM_LEN Last stream packet length at end slice

VLCE_END_DBG Debug flag of vlc encode end slice

DSP_OV_DBG Debug flag of stream buffer overflow flag

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x1010	COEFF_NUM_SLICE[7:0]							
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	COEFF_NUM_SLICE[15;8]							
	[23]	[22]	[21]	[20]	[18]	[18]	[17]	[16]
	COEFF_NUM_SLICE[23:16]							
	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]
	COEFF_NUM_SLICE[31:24]							

COEFF_NUM_SLICE Total non-zero coeff number within current slice.

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x1014	RESERVED							VLC_INT
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	RESERVED		VLC_ENC_MB_X_DBG[6:0]					
	[23]	[22]	[21]	[20]	[18]	[18]	[17]	[16]
	RESERVED		VLC_ENC_MB_Y_DBG[6:0]					
	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]
	RESERVED							

VLC_INT VLC encoder interrupt flag

VLC_ENC_MB_X_DBG VLC encoded MB numbers at x direction

VLC_ENC_MB_Y_DBG VLC encoded MB numbers at y direction

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x1018	VLC_STREAM_CRC[7:0]							
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	VLC_STREAM_CRC[15:8]							
	[23]	[22]	[21]	[20]	[18]	[18]	[17]	[16]
	VLC_STREAM_CRC[23:16]							
	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]
	VLC_STREAM_CRC[31:24]							

VLC_STREAM_CRC CRC value for vlc encode stream, debug only.

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x101C	RESERVED						VLC_BT_MODE	MPI_RW_LUT
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	RESERVED			VLC_HEAD_LEN[4:0]				
	[23]	[22]	[21]	[20]	[18]	[18]	[17]	[16]
	VLC_HEAD_DATA[7:0]							
	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]
	VLC_HEAD_DATA[15:8]							

MPI_RW_LUT Switch between SW access look-up table and VLC encoder stream buffer

VLC_BT_MODE Enable the burst mode when SW read VLC stream buffer through PCI bus

VLC_HEAD_LEN SW download slice head length

VLC_HEAD_DATA SW download slice head data

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x1020	Ch3_ms_pty_reg		Ch1_ms_pty_reg		Ch1_ms_pty_reg		Ch0_ms_pty_reg	
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	Ch7_ms_pty_reg		Ch6_ms_pty_reg		Ch5_ms_pty_reg		Ch4_ms_pty_reg	
	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
	Ch11_ms_pty_reg		Ch10_ms_pty_reg		Ch9_ms_pty_reg		Ch8_ms_pty_reg	
	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]
	Ch15_ms_pty_reg		Ch14_ms_pty_reg		Ch13_ms_pty_reg		Ch12_ms_pty_reg	

Chn_ms_pty_reg Channel 0~ 15 main stream priority setting register. Default 0x55555555

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x1024	Ch3_ss_pty_reg		Ch1_ss_pty_reg		Ch1_ss_pty_reg		Ch0_ss_pty_reg	
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	Ch7_ss_pty_reg		Ch6_ss_pty_reg		Ch5_ss_pty_reg		Ch4_ss_pty_reg	
	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
	Ch11_ss_pty_reg		Ch10_ss_pty_reg		Ch9_ss_pty_reg		Ch8_ss_pty_reg	
	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]
	Ch15_ss_pty_reg		Ch14_ss_pty_reg		Ch13_ss_pty_reg		Ch12_ss_pty_reg	

Chn_ss_pty_reg Channel 0~ 15 sub-stream priority setting register. Default 0x55555555

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x1028	cur_frm_gop							
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	enc_frm_type							
	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
			dsp_hdmas_qp_ini					
	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]
	RESERVED							

cur_frm_gop Current frame GOP setting register

enc_frm_type Current frame type in encode mode

0	I frame
1	IDR frame
2	P frame
3	reserved

dsp_hdmas_qp_ini initial QP value

NOTE: **: FOR ADDRESS 0X2000 – 0X3FFF:**
When set MPI_RW_LUT to 1, and vlce is idle (no processing any encoder task), SW can read back look-up table.
When set MPI_RW_LUT to 0, SW can read back vlc encoder stream.

VLCD REGISTERS

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x1000	VLC_DECODED_PKG_NUM		VLC_DEC_NAL_PKG_NUM		RESERVED			VLC_HD_EN
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	VLC_HD_SLICE_TYPE		VLC_HD_SLICE_QP					
	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
	RESERVED			VLC_ERR_INT_EN	VLC_STR_SWP	VLC_DEC03_EN	RESERVED	VLC_INT_EN
	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]
	RESERVED							

VLC_HD_EN Enable vlc decoder slice header

VLC_DEC_NAL_PKG_NUM Slice package number need decode

VLC_DECODED_PKG_NUM Vlc decoded slice package number

VLC_HD_SLICE_QP Vlc decoded slice initial QP

VLC_HD_SLICE_TYPE Vlc decoded slice type

VLC_INT_EN Enable vlc decoder asserts interrupt flag

VLC_DEC03_EN Enable HW delete 0x03 in the bit stream

VLC_STR_SWP Enable or disable the swap of SW download bit stream

VLC_ERR_INT_EN Enable the assertion of vlcd interrupt flag when the HW decoder detects a bit stream error.

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x1004	RESERVED		VLC_ERR	0	VLC_END_SLICE	VLC_INT_FLAG	BK1_EMPTY	BK0_EMPTY
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	RESERVED							
	[23]	[22]	[21]	[20]	[18]	[18]	[17]	[16]
	RESERVED							VLC_ERR_BUS[0]
	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]
	VLC_ERR_BUS[8:1]							

BK0_EMPTY Bank 0 empty of vlcd stream buffer

BK1_EMPTY Bank 1 empty of vlcd stream buffer

VLC_INT_FLAG Vlcd interrupt flag

VLC_END_SLICE Vlcd end slice flag

VLC_ERR Vlcd detects a bit stream

VLC_ERR_BUS Vlcd detects error location, debug only

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x1008	VLC_BIT_ALIGN						VLC_REF_PIC_NUM_L0	
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	VLC_SW_SLICE_TYPE		VLC_SW_SLICE_QP					
	[23]	[22]	[21]	[20]	[18]	[18]	[17]	[16]
	VLC_SW_INI_MB_Y[5:0]						RESERVED	
	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]
	VLC_SW_INI_MB_X[6:0]							VLC_SW_INI_MB_Y[6]

VLC_REF_PIC_NUM_L0 Maximal reference frame number of back search

VLC_BIT_ALIGN SW decodes slice header consumed bit number

VLC_SW_SLICE_QP SW decodes slice initial QP

VLC_SW_SLICE_TYPE SW decodes slice type

VLC_SW_INI_MB_Y SW decodes initial start MB number of y- coordinates

VLC_SW_INI_MB_X SW decodes initial start MB number of x- coordinates

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x100C	RESERVED							VLCD_STR_END
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	RESERVED							
	[23]	[22]	[21]	[20]	[18]	[18]	[17]	[16]
	RESERVED							
	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]
	RESERVED							

VLCD_STR_END SW notes vlcd HW that the download of bit stream for this slice ended

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x1018	VLC_DEC_MB_X_DBG[7:0]							
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	VLC_DEC_MB_Y_DBG[7:0]							
	[23]	[22]	[21]	[20]	[18]	[18]	[17]	[16]
	Reserved							
	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]
	Reserved							

VLC_DEC_MB_X_DBG Vlc decoded MB numbers at x-coordinates, debug only.

VLC_DEC_MB_Y_DBG Vlc decoded MB numbers at y-coordinates, debug only.

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x101C	VLC_DEC_MB_X_DBG[6:0]							VLC_RW_LUT
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	VLC_RD_STR_EN	VLC_DEC_MB_Y_DBG[6:0]						
	[23]	[22]	[21]	[20]	[18]	[18]	[17]	[16]
	HEAD_DECODE_FRAME_NUM[7:0]							
	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]
	HEAD_DECODE_FRAME_NUM[15:8]							

VLC_RW_LUT Switch between SW r/w vlcd look-up table or vlcd stream buffer

VLC_DEC_MB_X_DBG Whole H264 core processed MB number at x-coordinates, debug only

VLC_DEC_MB_Y_DBG Whole H264 core processed MB number at y-coordinates, debug only

VLC_RD_STR_EN SW read out the bit stream for debug purpose

HEAD_DECODE_FRAME_NUM frame number decoded from slice header

NOTE: : **FOR ADDRESS 0X2000 – 0X3FFF:**

When set MPI_RW_LUT to 1, and vlcd is idle (no processing any decoder task), SW can read back look-up table.

When set MPI_RW_LUT to 0, set VLC_RD_STR_EN to 1 and vlcd is idle (no processing any decoder task), SW can read back vlc decoder stream for debug purpose

0x4000 ~ 0x4074: Audio ADPCM

Address	[31:0]
0x4000	RTC_1ms_ counter

RTC_1ms_counter — RTC_1ms_counter = Realtime clk/1000

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x4004						enc_adpcm_enb	org_data_enb	dec_adpcm_enb

dec_adpcm_enb — ADPCM decoder enable

0 Enable

1 Disable

org_data_enb — ADPCM input data enable

1 Enable

0 Disable

enc_adpcm_enb — ADPCM encoder enable

1 Enable

0 Disable

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x4008	AUD_ORG_CH_EN[7:0]							
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	AUD_ORG_CH_EN [15:8]							
	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
					AUD_ORG_CH_EN [19:16]			
	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]
	AUD_MODE							

AUD_ORG_CH_EN — Record path PCM Audio enable bit for each channel

AUD_MODE

0 Asynchronous Mode or PCI target mode

1 PCI Initiator Mode

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x400C	AUD_ADPCM_CH_EN[7:0]							
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	AUD_ADPCM_CH_EN [15:8]							
	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
	AUD_SAMPLE_RATE[3:0]				AUD_TYPE[1:0]		AD_BIT_MODE	SPK_ADPCM_EN
	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]
		TEST_ADLOOP_EN	TESTLOOP_EN	TESTLOOP_CHID				

AUD_ADPCM_CH_EN Record path ADPCM audio channel enable, one bit for each

SPK_ADPCM_EN Speaker path ADPCM audio channel enable

AD_BIT_MODE
0 16bit
1 8bit

AUD_TYPE
0 PCM
3 ADPCM
Others Reserved

AUD_SAMPLE_RATE
0 8K
1 16K

TESTLOOP_CHID Channel ID used to select audio channel (0 to 16) for loopback

TESTLOOP_EN Reserved

TEST_ADLOOP_EN
1 Enable AD Loopback Test
0 Disable AD Loopback Test

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x4014	Ch1_soft_reset	Ch0_soft_reset	ADPCM_DEC_EN		DA1_BIT_MODE	DA1_MUTE	DA0_BIT_MODE	DA0_MUTE
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
					Ch1_soft_hand_play	Ch0_soft_hand_play	Ch1_stand_play	Ch0_stand_play

DAn_Mute Audio DA mute
0 Disable
1 Enable

DAn_BIT_MODE
0 16 bit mode
1 8 bit mode

ADPCM_DEC_EN ADPCM decoder channel enable
0 Disable
1 Enable

Ch0_soft_reset software refresh audio ch0 ddr buf data 1'b1
Ch1_soft_reset software refresh audio ch1 ddr buf data 1'b1

Ch0_stand_play	ch0 Playback path Followed by the ddr buf number output
Ch1_stand_play	ch1 Playback path Followed by the ddr buf number output
Ch0_soft_hand_play	ch0 audio playback follows mandatory rule
Ch1_soft_hand_play	ch1 audio playback follows mandatory rule

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x4018				PC_BLOCK_ADPCM_RD_NO				

PC_BLOCK_ADPCM_RD_NO	The channel number (0 ~ 16) of current completed transfer block, when transferring ADPCM audio.

Address	[29:0]
0x401C	ADPCM_ENC_WR_PTR[29:0]
0x4020	ADPCM_ENC_WR_PTR[50:30]

ADPCM_ENC_WR_PTR ADPCM Encoding Write Pointer for channel 0 ~ 16, 3 bits each. (Note that even though the total audio input is 10 channels each TW5866. The total audio channel supported is at maximum of 17 channels.)

Address	[29:0]
0x4024	ADPCM_ENC_RD_PTR[29:0]
0x4028	ADPCM_ENC_RD_PTR[50:30]

ADPCM_ENC_RD_PTR ADPCM Encoding Read Pointer for channel 0 ~ 16, 3 bits each. (Note that even though the total audio input is 10 channels each TW5866. The total audio channel supported is at maximum of 17 channels.)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x402c	ADPCM_DEC_RD_PTR0[7:0]							
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	ADPCM_DEC_RD_PTR1[7:0]							
	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
	ADPCM_DEC_WR_PTR0[7:0]							
	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]
	ADPCM_DEC_WR_PTR1[7:0]							

ADPCM_DEC_RD_PTRn audio decoder read pointer n (n= 0 or 1)

ADPCM_DEC_WR_PTRn **audio decoder write pointer n (n = 0 or 1)**

Address	[31:0]							
0x4030	AD_ORIG_WR_PTR[31:0]							
0x4034	AD_ORIG_WR_PTR[63:32]							
0x4038								AD_ORIG_WR_PTR[67:64]

AD_ORIG_WR_PTR **Audio original buffer write pointer for channel 0 ~ 16. 4 bits each. (Note that even though the total audio input is 10 channels each TW5866. The total audio channel supported is at maximum of 17 channels.)**

Address	[31:0]							
0x403C	AD_ORIG_RD_PTR[31:0]							
0x4040	AD_ORIG_RD_PTR[63:32]							
0x4044								AD_ORIG_RD_PTR[67:64]

AD_ORIG_RD_PTR Audio original buffer read pointer for channel 0 ~ 16, 4-bit each. Note that although the total audio input is 10 channels per TW5866, the total audio channels number supported is 17 maximum.

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x4048				PC_BLOCK_ORIG_RD_NO				

PC_BLOCK_ORIG_RD_NO **the channel number (from 0 to 16) of current transfer-finished block, when transferring original audio block to PC.**

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x404C	PCI_DATA_SEL:[7:0]							
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	PCI_DATA_SEL[15:8]							
	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
							PCI_AUD_FRM_EN	PCI_FLOW_EN
	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]

PCI_DATA_SEL — The register is applicable to PCI initiator mode only. Used to select PCM (0) or ADPCM (1) audio data sent to PC. One bit for each channel

PCI_FLOW_EN — Audio flow control mode selection bit.

0 Flow control disabled. TW5866 continuously sends audio frame to PC (initiator mode)

1 Flow control enabled

PCI_AUD_FRM_EN — When PCI_FLOW_EN is set, PCI need to toggle this bit to send an audio frame to PC. One toggle to send one frame.

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x4050					Ch1_aud_off_flag	Ch0_aud_off_flag	Ch1_dec_error flag	Ch0_dec_error flag

Ch0_dec_error_flag — Ch0 decode audio stream error flag (read only)

Ch1_dec_error_flag — Ch1 decode audio stream error flag (read only)

Ch0_aud_off_flag — Ch0 No Audio (read only)

1 No audio

0 Has audio

Ch1_aud_off_flag — Ch1 No Audio (read only)

1 No audio

0 Has audio

Address	[31:0]
0x4064	Audio_chn_map[31:0]
0x4068	Audio_chn_map[63:32]
0x406c	Audio_chn_map[95:64]
0x4070	Audio_chn_map[127:96]
0x4074	Audio_chn_map[159:128]

Audio_chn_map — Audio Channel Map for channel 0 ~ 19, 8 bits each channel. Note that out of the 20 channels, only maximum of 17 channels are usable.

0x8100 ~ 0x813C: VD_VP_VJ_HD

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x8100	RESERVED						H264_ENC_EN[1:0]	
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	RESERVED						H264_ENC_STA	

H264_ENC_EN H264 encoder path channel enable, each bit for each HD channel

H264_ENC_STA H264 encoder path enabled status(read only)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x8104	RESERVED				H264_CH0_Y_DOWN	H264_CH0_PROG	Reserved	
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	RESERVED				H264_CH1_Y_DOWN	H264_CH1_PROG	Reserved	

H264_CH0_PROG CH0 for H264 encoder path is progressive image.
1'b1: CH0 input is progressive image.
1'b0: CH0 input is interleaving image.

H264_CH1_PROG CH1 for H264 encoder path is progressive image.
1'b1: CH1 input is progressive image.
1'b0: CH1 input is interleaving image.

H264_CH0_Y_DOWN CH0 do y-direction 1/2 downscale for H264 encoder path.
1'b1: Do y-direction 1/2 downscale.
1'b0: Don't do y-direction 1/2 downscale.

H264_CH1_Y_DOWN CH1 do y-direction 1/2 downscale for H264 encoder path.
1'b1: Do y-direction 1/2 downscale.
1'b0: Don't do y-direction 1/2 downscale.

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x8108	RESERVED			SWITCH_EN	RESERVED		PREV_EN	
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	RESERVED						PREV_STA	

PREV_EN Preview path channel enable.

SWITCH_EN enable 2 HD channel switching output, only 1 channel output active at one time. Frame rate ration of the two channels can be controlled by "SWITCH_CTRL" 0x0C.

PREV_STA Preview path enabled status.

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x810C	RESERVED				PREV_CH0_Y_DOWN	PREV_CH0_PROG	Reserved	
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	SWITCH_CTRL				PREV_CH1_Y_DOWN	PREV_CH1_PROG	Reserved	

PREV_CHn_PROG CHn for preview path is progressive image.
1'b1: CH0 input is progressive image.
1'b0: CH0 input is interleaving image.

PREV_CHn_Y_DOWN CHn do y-direction 1/2 downscale for preview path.
1'b1: Do y-direction 1/2 downscale.
1'b0: Don't do y-direction 1/2 downscale.

SWITCH_CTRL 4'h0: 1 frame ch0 then 1 frame ch1

4'h1-2:1	4'h2-3:1	4'h3-4:1	4'h4-5:1
4'h5-6:1	4'h6-7:1	4'h7-8:1	4'h8-1:2
4'h9-1:3	4'ha-1:4	4'hb-1:5	4'hc-1:6
4'hd-1:7	4'he-1:8	4'hf: reserved	

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x8110	RESERVED						JPEG_EN	
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	RESERVED						JPEG_STA	

JPEG_EN JPEG path channel enable.

JPEG_STA JPEG path enabled status.

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x8114	RESERVED				JPEG_CH0_Y_DOWN	JPEG_CH0_PROG	Reserved	
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	RESERVED				JPEG_CH1_Y_DOWN	JPEG_CH1_PROG	Reserved	

JPEG_CHn_PROG CHn for JPEG encoder path is progressive image.
1'b1: CH0 input is progressive image.
1'b0: CH0 input is interleaving image.

JPEG_CHn_Y_DOWN CHn do y-direction 1/2 downscale for JPEG encoder path.
1'b1: Do y-direction 1/2 downscale.
1'b0: Don't do y-direction 1/2 downscale.

<table>
<tr><th>Address</th><th>[7]</th><th>[6]</th><th>[5]</th><th>[4]</th><th>[3]</th><th>[2]</th><th>[1]</th><th>[0]</th></tr>
<tr><td rowspan="3">0x8118</td><td colspan="8">DBG_CH_X_NUM[7:0]</td></tr>
<tr><td>[15]</td><td>[14]</td><td>[13]</td><td>[12]</td><td>[11]</td><td>[10]</td><td>[9]</td><td>[8]</td></tr>
<tr><td colspan="3">DBG_CH_SEL</td><td>XY_CHANGE</td><td colspan="4">DBG_CH_X_NUM[11:8]</td></tr>
</table>

DBG_CH_X_NUM **Debug channel x-direction pixel number.**

XY_CHANGE **Debug channel x/y number changed.**

DBG_CH_SEL **Debug channel select.**

3'h0 **select H264 encoder channel_0.**
3'h1 **select H264 encoder channel_1.**
3'h2 **select preview path channel_0.**
3'h3 **select preview path channel_1.**
3'h4 **select JPEG path channel_0.**
3'h5 **select JPEG path channel_1.**

<table>
<tr><th>Address</th><th>[7]</th><th>[6]</th><th>[5]</th><th>[4]</th><th>[3]</th><th>[2]</th><th>[1]</th><th>[0]</th></tr>
<tr><td rowspan="3">0x811C</td><td colspan="8">DBG_CH_Y_NUM[7:0]</td></tr>
<tr><td>[15]</td><td>[14]</td><td>[13]</td><td>[12]</td><td>[11]</td><td>[10]</td><td>[9]</td><td>[8]</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">DBG_CH_Y_NUM[12:8]</td></tr>
</table>

DBG_CH_Y_NUM **Debug channel y-direction line number.**

0x8200 ~ 0x849C: Senif_HD

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x8200	FRAM_FLAG_HD		PROG_FLAG_HD		VER_MIR_FLAG_HD		HOR_MIR_FLAG_HD	
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	RESERVED	SKIP_FLAG_HD	CHN_EN_HD		CHN_VLD_FLAG_HD		FULL_FLAG_HD	
	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
	RESERVED							
	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]
	RESERVED							

HOR_MIR_FLAG_HD[n]	1	Horizontal Mirror for HD channel n, HD channel n from 0 to 1	
		0	Normal
VER_MIR_FLAG_HD[n]	1	Vertical Mirror for HD channel n	
		0	Normal
PROG_FLAG_HD[n]		1	Progressive in HD channel n
		0	Interlaced in HD channel n
FRAM_FLAG_HD[n]		1	Frame mode in HD channel n
		0	Field Mode in HD channel n
FULL_FLAG_HD[n]		1	Full mode in HD channel n
		0	Vertical half down sample in HD channel n
CHN_VLD_FLAG_HD[n]	0→1 rising edge activates inner frame_cnt for HD channel n		
CHN_EN_HD[n]		1	Enable HD channel n capture
		0	Disable HD channel n capture
SKIP_FLAG_HD		1	Keep capture ignoring encoder state
		0	Capture HD original frame without collision with encoder

Address	[10:0]
0x8204	FRAM_WIDTH_HD_CH0
	[31:11]
	RESERVED

FRAM_WIDTH_HD_CH0 0x780 1080i
0x500 720P
0x3c0 960

Address	[10:0]
0x8208	FRAM_HEIGHT_HD_CH0
	[31:11]
	RESERVED

FRAM_ HEIGHT _HD_CH0 0x438 1080i
0x2D0 720P
0x240 960

Address	[10:0]
0x820c	FRAM_WIDTH_HD_CH1
	[31:11]
	RESERVED

FRAM_WIDTH_HD_CH1 0x780 1080i
0x500 720P
0x3c0 960

Address	[10:0]
0x8210	FRAM_HEIGHT_HD_CH1
	[31:11]
	RESERVED

FRAM_ HEIGHT _HD_CH1 0x438 1080i
0x2D0 720P
0x240 960

Address	[7:4]	[3:0]
0x8214	HD_CH1_MAP_ID	HD_CH0_MAP_ID
	[31:8]	
	RESERVED	

HD_CHn_MAP_ID HD Channel n map to the intra Channel ID,
Intra Channel id is from 0 to 15

Address	[31:4]	[3:2]	[1:0]
0x8240	RESERVED	HD_CH1_FRAM_PTR	HD_CH0_FRAM_PTR

HD_CHn_FRAM_PTR HD Channel n FRAME POINTER NUMBER

Address	[15:0]
0x8280	RT_CNTR_HD_CH0_FRM0
0x8284	RT_CNTR_HD_CH0_FRM1
0x8488	RT_CNTR_HD_CH0_FRM2
0x848C	RT_CNTR_HD_CH0_FRM3
0x8290	RT_CNTR_HD_CH1_FRM0
0x8294	RT_CNTR_HD_CH1_FRM1
0x8498	RT_CNTR_HD_CH1_FRM2
0x849C	RT_CNTR_HD_CH1_FRM3

RT_CNTR_HD_CHn_FRMm n = 0, 1, m = 0 ~ 3

Real Time Counter for HD channel 0, 1 for frame buffer 0 ~ 3.

0x8800 ~ 0x883C: Interrupt

Address	[15:0]
0x8800	TRIGER_MODE_L
0x8804	TRIGER_MODE_H
0x8808	INTR_ENABLE_L
0x880C	INTR_ENABLE _H
0x8810	INTR_CLR_L
0x8814	INTR_CLR_H
0x8818	INTR_ASSERT_L
0x881C	INTR_ASSERT_H

TRIGER_MODE_L — Trigger mode of interrupt source 0 ~ 15 (default 0)
- 1 Edge trigger mode
- 0 Level trigger mode

TRIGER_MODE_H — Trigger mode of interrupt source 16 ~ 31 (default 0)
- 1 Edge trigger mode
- 0 Level trigger mode

INTR_ENABLE_L — Enable of interrupt source 0 ~ 15 (default 0)
- 1 Enable interrupt
- 0 Disable interrupt

INTR_ENABLE_H — Enable of interrupt source 16 ~ 31 (default 0)
- 1 Enable interrupt
- 0 Disable interrupt

INTR_CLR_L — Clear interrupt command of interrupt source 0 ~ 15(default 0)
- 1 Clear interrupt
- 0 Not clear interrupt

INTR_CLR_H — Clear interrupt command of interrupt source 16 ~ 31(default 0)
- 1 Clear interrupt
- 0 Not clear interrupt

INTR_ASSERT_L — Assertion of interrupt source 0 ~ 15(default 16'hFFFF)
- 1 High level or pos-edge is assertion
- 0 Low level or neg-edge is assertion

INTR_ASSERT_H — Assertion of interrupt source 16 ~ 31(default 16'hFFFF)
- 1 High level or pos-edge is assertion
- 0 Low level or neg-edge is assertion

Address	[0]
0x8820	INTR_OUT_LEVEL

INTR_OUT_LEVEL — Output level of interrupt (default 1'h1)
1 Interrupt output is high assertion
0 Interrupt output is low assertion

Address	[15:0]
0x8838	INTR_STATUS_L
0x883C	INTR_STATUS_H

INTR_STATUS_L — Status of interrupt source 0 ~ 15 (Read only)
1 With interrupt
0 No interrupt
Bit [0]: VLC 4k RAM interrupt
Bit [1]: BURST DDR RAM interrupt
Bit [2]: MV DSP interrupt
Bit [3]: video lost interrupt
Bit [4]: gpio 0 interrupt
Bit [5]: gpio 1 interrupt
Bit [6]: gpio 2 interrupt
Bit [7]: gpio 3 interrupt
Bit [8]: gpio 4 interrupt
Bit [9]: gpio 5 interrupt
Bit [10]: gpio 6 interrupt
Bit [11]: gpio 7 interrupt
Bit [12]: JPEG interrupt
Bit [13:15]: Reserved

INTR_STATUS_H — Status of interrupt source 16 ~ 31 (Read only)
1 With interrupt
0 No interrupt
Bit [0]: Reserved
Bit [1]: VLC done interrupt
Bit [2]: Reserved
Bit [3]: AD Vsync interrupt
Bit [4]: Preview eof interrupt
Bit [5]: Preview overflow interrupt
Bit [6]: Timer interrupt
Bit [7]: Reserved
Bit [8]: Audio eof interrupt
Bit [9]: I2C done interrupt
Bit [10]: AD interrupt
Bit [11]: Grab interrupt
Bit [12]: HD preview interrupt
Bit [13]: Reserved
Bit [14]: PCI PERR_O interrupt
Bit [15]: PCI SERR_O interrupt

Address	[15:8]	[7:0]
0x9800	GPIO_DATA_OUT_EN	GPIO_DATA_OUT

GPIO_DATA_OUT	GPIO [7:0] data out	
GPIO_DATA_OUT_EN	GPIO [7:0] data output enable	
	1	GPIO output enable
	0	GPIO input enable (default)

NOTE: WHEN USING GPIO AS INTERRUPTS, SET THE RELATED GPIO_DATA_OUT_EN BIT TO 0, AND THEN REFER TO 8800 ~ 883C FOR CONTROL INTERRUPTS.

0x9000 ~ 0x920C: Video Capture (VIF)

Address	[15:0]
0x9000	H264EN_CH_STATUS

H264EN_CH_STATUS[n] Status of Vsync synchronized H264EN_CH_EN (Read Only)
1 Channel Enabled
0 Channel Disabled

Address	[15:0]
0x9004	H264EN_CH_EN

H264EN_CH_EN[n] H264 Encoding Path Enable for channel n
1 Channel Enabled
0 Channel Disabled

Address	[15:0]
0x9008	H264EN_CH_DNS

H264EN_CH_DNS[n] H264 Encoding Path Downscale Video Decoder Input for channel n
1 Downscale Y to 1/2
0 Does not downscale

Address	[15:0]
0x900C	H264EN_CH_PROG

H264EN_CH_PROG[n] H264 Encoding Path channel n is progressive
1 Progressive (Not valid for TW5864)
0 Interlaced (TW5864 default)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x9010					H264EN_BUS_MAX_CH			

H264EN_BUS_MAX_CH[n] H264 Encoding Path maximum number of channel on BUS n
0 Max 4 channels
1 Max 2 channels

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x9014	H264EN_RATE_MAX_LINE_1[2:0]			H264EN_RATE_MAX_LINE_0				
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
							H264EN_RATE_MAX_LINE_1[4:3]	
Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x9018	H264EN_RATE_MAX_LINE_3[2:0]			H264EN_RATE_MAX_LINE_2				
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
							H264EN_RATE_MAX_LINE_3[4:3]	

H264EN_RATE_MAX_LINE_n H264 Encoding path Rate Mapping Maximum Line Number on Bus n

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x9020	H264EN_CH3_FMT		H264EN_CH2_FMT		H264EN_CH1_FMT		H264EN_CH0_FMT	
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	H264EN_CH7_FMT		H264EN_CH6_FMT		H264EN_CH5_FMT		H264EN_CH4_FMT	
Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x9024	H264EN_CH3_FMT		H264EN_CH2_FMT		H264EN_CH1_FMT		H264EN_CH0_FMT	
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	H264EN_CH7_FMT		H264EN_CH6_FMT		H264EN_CH5_FMT		H264EN_CH4_FMT	

H264EN_CHn_FMT H264 Encoding Path Format configuration of Channel n

00 D1 (For D1 and hD1 frame)

01 (Reserved)

10 (Reserved)

11 D1 with ½ size in X (for CIF frame)

Note: To used with 0x9008 register to configure the frame size

Address	[15:0]
0x9100	H264EN_RATE_CNTL_BUS0_CH0[15:0]
0x9104	H264EN_RATE_CNTL_BUS0_CH0[31:16]
0x9108	H264EN_RATE_CNTL_BUS0_CH1[15:0]
0x910C	H264EN_RATE_CNTL_BUS0_CH1[31:16]
0x9110	H264EN_RATE_CNTL_BUS0_CH2[15:0]
0x9114	H264EN_RATE_CNTL_BUS0_CH2[31:16]
0x9118	H264EN_RATE_CNTL_BUS0_CH3[15:0]
0x911C	H264EN_RATE_CNTL_BUS0_CH3[31:16]
0x9120	H264EN_RATE_CNTL_BUS1_CH0[15:0]
0x9124	H264EN_RATE_CNTL_BUS1_CH0[31:16]
0x9128	H264EN_RATE_CNTL_BUS1_CH1[15:0]
0x912C	H264EN_RATE_CNTL_BUS1_CH1[31:16]
0x9130	H264EN_RATE_CNTL_BUS1_CH2[15:0]
0x9134	H264EN_RATE_CNTL_BUS1_CH2[31:16]
0x9138	H264EN_RATE_CNTL_BUS1_CH3[15:0]
0x913C	H264EN_RATE_CNTL_BUS1_CH3[31:16]
0x9140	H264EN_RATE_CNTL_BUS2_CH0[15:0]
0x9144	H264EN_RATE_CNTL_BUS2_CH0[31:16]
0x9148	H264EN_RATE_CNTL_BUS2_CH1[15:0]
0x914C	H264EN_RATE_CNTL_BUS2_CH1[31:16]
0x9150	H264EN_RATE_CNTL_BUS2_CH2[15:0]
0x9154	H264EN_RATE_CNTL_BUS2_CH2[31:16]
0x9158	H264EN_RATE_CNTL_BUS2_CH3[15:0]
0x915C	H264EN_RATE_CNTL_BUS2_CH3[31:16]
0x9160	H264EN_RATE_CNTL_BUS3_CH0[15:0]
0x9164	H264EN_RATE_CNTL_BUS3_CH0[31:16]
0x9168	H264EN_RATE_CNTL_BUS3_CH1[15:0]
0x916C	H264EN_RATE_CNTL_BUS3_CH1[31:16]
0x9170	H264EN_RATE_CNTL_BUS3_CH2[15:0]
0x9174	H264EN_RATE_CNTL_BUS3_CH2[31:16]
0x9178	H264EN_RATE_CNTL_BUS3_CH3[15:0]
0x917C	H264EN_RATE_CNTL_BUS3_CH3[31:16]

H264EN_RATE_CNTL_BUSm_CHn	**H264 Encoding Path BUS m Rate Control for Channel n**

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x9200	H264EN_BUS0_MAP_CH1				H264EN_BUS0_MAP_CH0			
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	H264EN_BUS0_MAP_CH3				H264EN_BUS0_MAP_CH2			
Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x9204	H264EN_BUS1_MAP_CH1				H264EN_BUS1_MAP_CH0			
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	H264EN_BUS1_MAP_CH3				H264EN_BUS1_MAP_CH2			
Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x9208	H264EN_BUS2_MAP_CH1				H264EN_BUS2_MAP_CH0			
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	H264EN_BUS2_MAP_CH3				H264EN_BUS2_MAP_CH2			
Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x920C	H264EN_BUS3_MAP_CH1				H264EN_BUS3_MAP_CH0			
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	H264EN_BUS3_MAP_CH3				H264EN_BUS3_MAP_CH2			

H264EN_BUSm_MAP_CHn — The16-to-1 MUX configuration register for each encoding channel (total of 16 channels). Four bits for each channel.

0x9800: GPIO

Address	[15:8]	[7:0]
0x9800	GPIO_DATA_OUT_EN	GPIO_DATA_OUT

GPIO_DATA_OUT — GPIO[7:0] data out

GPIO_DATA_OUT_EN — GPIO[7:0] data output enable
- 1 GPIO output enable
- 0 GPIO input enable (default)

NOTE: WHEN USING GPIO AS INTERRUPTS, SHOULD SET THE RELATED GPIO_DATA_OUT_EN BIT TO 0, AND THEN PREFER TO 8800 ~ 883C TO CONTROL INTERRUPT .

0xA000 ~ 0xA098: DDR2 Control

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xA000	wr_recovery				cas_latency			
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	RESERVED						rtt_value	

cas_latency DDR CAS latency (default 5)

wr_recovery DDR write recovery (default is 5)

rtt_value DDR On-Die Termination value (default is 1)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xA004	RESERVED				t_wr_max			
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	t_rfc_max							

t_wr_max DDR write recovery Min value (default 5)

t_rfc_max Refresh to Active or to Refresh interval (default is 0x50)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xA008	t_mrd_max							
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	t_rp_max							
	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]

t_mrd_max load mode cycle time (default 2)

t_rp_max Precharge period (default is 0x7)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xA00C	ddr_ref_cntr_max[7:0]							
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	ddr_ref_cntr_max[15:8]							

ddr_ref_cntr_max auto-refresh period (default 0x93B)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xA010	RESERVED			wr_to_rd_lat_max				
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	RESERVED			rd_to_wr_lat_max				

wr_to_rd_lat_max Write to Read delay Min delay (default 5)

rd_to_wr_lat_max Read to Write delay Min delay (default 0xa)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xA014	RESERVED			t_rtp_max				
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	RESERVED				t_rcd_max			

t_rtp_max Internal Read to Precharge Min delay (default 5)

t_rcd_max Active to Read/Write Min delay (default 0xa)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xA018	t_ras_max				t_rrd_max			
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	no_ref_enb	RESERVED						

t_rrd_max DDR active to active delay (default 3)

t_ras_max DDR active to precharge delay (default is 0xe)

no_ref_enb not force auto-refresh happen ever 7.8us (default is 0)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xA01C				ddr_info				
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	RESERVED							

ddr_info Capability of DDR2 on board (default 8)

1: 256Mb DDR2
2: 512Mb DDR2
4: 1Gb DDR2
8: 2Gb DDR2
10: 4Gb DDR2

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xA024								dfi_ complete
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	RESERVED							

dfi_complete | dfi complete
1 dfi initiate complete
0 dfi initiate not complete

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xA03C	RESERVED					opb2_start	opb1_start	opb0_start
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	RESERVED							

opb0_start | Start OPB Bus0 self-test (default 0)
1 start OPB bus0 self test

opb1_start | Start OPB Bus1 self-test (default 0)
1 start OPB bus1 self test

opb2_start | Start OPB Bus2 self-test (default 0)
1 start OPB bus2 self test

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xA040	RESERVED		opb0_data_mode		RESERVED			opb0_rw
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	opb0_mas_m	opb0_single_m	RESERVED			opb0_test_bank		

opb0_rw | Inner OPB Bus0 write/read command flag (default 0)
1 write command
0 read command

opb0_data_mode | Inner OPB Bus0 test sequence (default 0)
0 32'hAAAA5555
1 32'hFFFFFFFF
2 32'hA5A55A5A
3 Increase sequence

opb0_test_bank | Start bank of self test (default 0)

opb0_single_m | Inner OPB Bus0 single mode
1 single read/write
0 burst read/write

opb0_mas_m | Inner OPB Bus0 master mode
1 Inner OPB Bus0 self test mode enable
0 Inner OPB Bus0 self test mode disable

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xA044	opb0_burst_cntr_max							
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	RESERVED							

opb0_burst_cntr_max Length of each burst (default 0)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xA048	opb0_ddr_proc_cntr_max[7:0]							
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	opb0_ddr_proc_cntr_max[15:8]							
Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xA04C	opb0_ddr_proc_cntr_max[23:16]							
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	RESERVED						opb0_ddr_proc_cntr_max[25:24]	

opb0_burst_cntr_max Set the maximum burst number of opb0 in self-test (default 0)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xA054	opb0_rd_err_cntr[7:0]							
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	opb0_rd_err_cntr[15:8]							
Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xA058	opb0_rd_err_cntr[23:16]							
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	opb0_err_flag	opb0_end	RESERVED				opb0_rd_err_cntr[25:24]	

opb0_rd_err_cntr Count of read error (read only)

opb0_end OPB0 self test end flag (read only)

opb0_err_flag OPB0 read error flag (read only)

<table>
<tr><th>Address</th><th>[7]</th><th>[6]</th><th>[5]</th><th>[4]</th><th>[3]</th><th>[2]</th><th>[1]</th><th>[0]</th></tr>
<tr><td rowspan="4">0xA060</td><td colspan="2">RESERVED</td><td colspan="2">opb1_data_mode</td><td colspan="3">RESERVED</td><td>opb1_rw</td></tr>
<tr><td>[15]</td><td>[14]</td><td>[13]</td><td>[12]</td><td>[11]</td><td>[10]</td><td>[9]</td><td>[8]</td></tr>
<tr><td>opb1_mas_m</td><td>opb1_single_m</td><td colspan="3">RESERVED</td><td colspan="3">opb1_test_bank</td></tr>
</table>

opb1_rw	Inner OPB BUS1 write/read command flag (default 0)	
	1	write command
	0	read command
opb1_data_mode	Inner OPB BUS1 test sequence (default 0)	
	0	32'hAAAA5555
	1	32'hFFFFFFFF
	2	32'hA5A55A5A
	3	Increase sequence
opb1_test_bank	Start bank of self test (default 0)	
opb1_single_m	Inner OPB BUS1 single mode	
	1	single read/write
	0	burst read/write
opb1_mas_m	Inner OPB BUS1 master mode	
	1	Inner OPB BUS1 self test mode enable
	0	Inner OPB BUS1 self test mode disable

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xA064	opb1_burst_cntr_max							
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	RESERVED							

opb1_burst_cntr_max Length of each burst (default 0)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xA068	opb1_ddr_proc_cntr_max[7:0]							
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	opb1_ddr_proc_cntr_max[15:8]							
Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xA06C	opb1_ddr_proc_cntr_max[23:16]							
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	RESERVED						opb1_ddr_proc_cntr_max[25:24]	

opb1_burst_cntr_max Set the maximum burst number of opb1 in self-test (default 0)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xA074	opb1_rd_err_cntr[7:0]							
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	opb1_rd_err_cntr[15:8]							
Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xA078	opb1_rd_err_cntr[23:16]							
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	opb1_err_flag	opb1_end	RESERVED				opb1_rd_err_cntr[25:24]	

opb1_rd_err_cntr Count of read error (read only)

opb1_end opb1 self test end flag (read only)

opb1_err_flag opb1 read error flag (read only)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xA080	RESERVED		opb2_data_mode		RESERVED			opb2_rw
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	opb2_mas_m	opb2_single_m	RESERVED			opb2_test_bank		

opb2_rw — Inner OPB BUS2 write/read command flag (default 0)
- 1 write command
- 0 read command

opb2_data_mode — Inner OPB BUS2 test sequence (default 0)
- 0 32'hAAAA5555
- 1 32'hFFFFFFFF
- 2 32'hA5A55A5A
- 3 Increase sequence

opb2_test_bank — Start bank of self test (default 0)

opb2_single_m — Inner OPB BUS2 single mode
- 1 single read/write
- 0 burst read/write

opb2_mas_m — Inner OPB BUS2 master mode
- 1 Inner OPB Bus2 self test mode enable
- 0 Inner OPB Bus2 self test mode disable

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xA084	opb2_burst_cntr_max							
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	RESERVED							

opb2_burst_cntr_max — Length of each burst (default 0)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xA088	opb2_ddr_proc_cntr_max[7:0]							
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	opb2_ddr_proc_cntr_max[15:8]							
Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xA08C	opb2_ddr_proc_cntr_max[23:16]							
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	RESERVED						opb2_ddr_proc_cntr_max[25:24]	

opb2_burst_cntr_max — Set the maximum burst number of opb2 in self-test (default 0)

<table>
<tr><th>Address</th><th>[7]</th><th>[6]</th><th>[5]</th><th>[4]</th><th>[3]</th><th>[2]</th><th>[1]</th><th>[0]</th></tr>
<tr><td rowspan="3">0xA094</td><td colspan="8">opb2_rd_err_cntr[7:0]</td></tr>
<tr><td>[15]</td><td>[14]</td><td>[13]</td><td>[12]</td><td>[11]</td><td>[10]</td><td>[9]</td><td>[8]</td></tr>
<tr><td colspan="8">opb2_rd_err_cntr[15:8]</td></tr>
<tr><th>Address</th><th>[7]</th><th>[6]</th><th>[5]</th><th>[4]</th><th>[3]</th><th>[2]</th><th>[1]</th><th>[0]</th></tr>
<tr><td rowspan="3">0xA098</td><td colspan="8">opb2_rd_err_cntr[23:16]</td></tr>
<tr><td>[15]</td><td>[14]</td><td>[13]</td><td>[12]</td><td>[11]</td><td>[10]</td><td>[9]</td><td>[8]</td></tr>
<tr><td>opb2_err_flag</td><td>opb2_end</td><td colspan="4">RESERVED</td><td colspan="2">opb2_rd_err_cntr[25:24]</td></tr>
</table>

opb2_rd_err_cntr	Count of read error (read only)
opb2_end	opb2 self test end flag (read only)
opb2_err_flag	opb2 read error flag (read only)

0xA800 ~ 0xABFC: Playback Control

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xA8n0					Ch_n_wr_ptr		Ch_n_rd_ptr	

Ch_n_wr_ptr Current write pointer of playback frame buffer (read only)

Ch_n_rd_ptr Current read pointer of playback frame buffer (read only)

NOTE: CPU USES THESE TWO POINTERS TO DECIDE WHETHER THE FRAME BUFFER IS EMPTY, AND THEN WRITES A NEW BUFFER NUMBER INTO 0XA8N4 TO NOTIFY HARDWARE.

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xA8n4	Ch_n_buffer_number0							
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	Ch_n_buffer_number1							
	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
	Ch_n_buffer_number2							
	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]
	Ch_n_buffer_number3							

Ch_n_buffer_numberX The rebuild frame to be play, 0~255

NOTE: AFTER AN INTERRUPT IS RECEIVED, THE SOFTWARE READS OUT THE WR_PTR AND RD_PRT, THEN COMPARES THESE TWO POINTERS, ESTIMATES WHETHER THERE ARE EMPTY BUFFER TO BE DISPLAYED. IF YES, THE SOFTWARE WRITES VALID BUFFER NUMBER. HARDWARE LOGIC CHANGES THE WR_PTR AND RD_PTR AFTER TRANSFERRING THE CORRESPONDING FRAME. THERE ARE TOTAL OF 16 GROUPS OF THIS, ONE FOR EACH CHANNEL.

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xA8n8	Ch_n_length						Ch_n_dir	Ch_n_dma_en
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	Ch_n_start_add							

Ch_n_dma_en: DMA mode enable

Ch_n_dir: display direction

1: ascending, the next buffer number is current frame number + 1

0: descending

Ch_n_length: DMA operation length, the maximum is 64

Ch_n_start_add: DMA operation start address

NOTE: THIS IS ANOTHER DMA CONFIGURATION METHOD USED BY SOFTWARE WHEN THERE ARE MANY FRAME TO BE DISPLAYED AND WE ONLY WANT TO ACTIVATE ONE TIME. IF THE SOFTWARE ENABLES THIS MODE, IT WILL OVER RULE THE OTHER COMMUNICATION METHOD. TO USE THIS CONFIGURATION METHOD, THE DIRECTION, LENGTH AND START ADDRESS SHOULD BE SET TO VALID VALUES BEFORE SETTING DMA ENABLE BIT. THERE ARE TOTAL OF 16 GROUPS OF THIS CONFIGURATION REGISTERS, ONE FOR EACH CHANNEL.

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xA900				sync_enb0	au_sync_chn_id0			
				sync_enb1	au_sync_chn_id1			

sync_enb0: Synchronization enable bit with audio 0

1 enable sync

0 disable sync

au_sync_chn_id0: Synchronization which channel with audio 0

sync_enb1: Synchronization enable bit with audio 1

1 enable sync

0 disable sync

au_sync_chn_id1: Synchronization which channel with audio 1

Notes: Software setting of each of these registers needs to synchronize with the corresponding channel audio

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xA904	4_block_in_hd[1:0]		plbk_out_en		output_mode_1		output_mode_0	
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	RESERVED						progressive_twll_mode	
	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
	RESERVED							
	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]
	RESERVED							

output_mode_n bus n SD or HD mode configuration (default 0)

2'b00 SD mode, include 27M D1, 54/108M byte/frame interleave.

2'b01 HD mode, include 720p, 1080i, 54M BT.1120.

plbk_out_en[n] Enable or disable play back on bus n (default 0)

1'b1 enable

1'b0 disable

4_block_in_hd[n] One or four windows when HD on bus n, configure only when HD mode. (Default 0)

1'b1 four windows

1'b0 one window

progressive_twll_mode [n] Only odd field in SD configuration on bus n (default 0)

1'b1 enable

1'b0 disable

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xA908	RESERVED			cascade_en	mux_pos			

	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	RESERVED			ntsc_pal	bt656_mode			
	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
	RESERVED							
	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]
	output_bus1_by_bus0	RESERVED			cascade_by_bus1	RESERVED		

mux_pos[n] cascade output source select for window n (default 0)

1'b1 cascade input

1'b0 local play back output

cascade_en: cascade enable (default 0)

1'b1 enable

1'b0 disable

ntsc_pal Cascade format in NTSC/PAL (default 0)

1'b0 PAL

1'b1 NTSC

bt656_mode: cascade format configuration (default 0)

4'h0 single SD in one bus

4'h1 2-byte interleave

4'h2 reserved.

4'h3 4-byte interleave

4'h4 reserved

4'h5 1080i

4'h6 720p

4'h7 Techwell HD (4*D1)

Others reserved

cascade_by_bus1: select cascade input source (default 0)

1'b1 select bus 1

1'b0 select outside cascade in

output_bus1_by_bus0: send bus1 by bus0 output pins when test mode (default 0)

1'b1 enable

1'b0 disable

<table>
<tr><th>Address</th><th>[7]</th><th>[6]</th><th>[5]</th><th>[4]</th><th>[3]</th><th>[2]</th><th>[1]</th><th>[0]</th></tr>
<tr><td rowspan="8">0xA910</td><td colspan="4">frame_interleave_mode_1</td><td colspan="4">frame_interleave_mode_0</td></tr>
<tr><td>[15]</td><td>[14]</td><td>[13]</td><td>[12]</td><td>[11]</td><td>[10]</td><td>[9]</td><td>[8]</td></tr>
<tr><td colspan="4">channel_valid_flag_1</td><td colspan="4">channel_valid_flag_0</td></tr>
<tr><td>[23]</td><td>[22]</td><td>[21]</td><td>[20]</td><td>[19]</td><td>[18]</td><td>[17]</td><td>[16]</td></tr>
<tr><td colspan="4">format_4_to_1_1</td><td colspan="4">format_4_to_1_0</td></tr>
<tr><td>[31]</td><td>[30]</td><td>[29]</td><td>[28]</td><td>[27]</td><td>[26]</td><td>[25]</td><td>[24]</td></tr>
<tr><td colspan="8">background_u</td></tr>
</table>

frame_interleave_mode_n — bus n frame interleave mode and channel number configuration (default 0)

[3:2] frame interleave mode
- 2'b00 no interleave
- 2'b01 byte interleave
- 2'b10 frame interleave

[1:0] interleave channel number
- 2'b00 1 channel
- 2'b01 2 channels
- 2'b10 3 channels
- 2'b11 4 channels

channel_valid_flag_n [m]bus n channel m valid flag when byte interleave (Default 0)
- 1'b1 valid
- 1'b0 not valid

format_4_to_1_n[m] — bus n window m format select when 4 windows in HD (default 0)
- 1'b1 D1 (put D1 to HD)
- 1'b0 normal format

background_u — background setting: u (default 0)

<table>
<tr><th>Address</th><th>[7]</th><th>[6]</th><th>[5]</th><th>[4]</th><th>[3]</th><th>[2]</th><th>[1]</th><th>[0]</th></tr>
<tr><td rowspan="8">0xA914</td><td colspan="8">background_v</td></tr>
<tr><td>[15]</td><td>[14]</td><td>[13]</td><td>[12]</td><td>[11]</td><td>[10]</td><td>[9]</td><td>[8]</td></tr>
<tr><td colspan="8">background_y</td></tr>
<tr><td>[23]</td><td>[22]</td><td>[21]</td><td>[20]</td><td>[19]</td><td>[18]</td><td>[17]</td><td>[16]</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td>[31]</td><td>[30]</td><td>[29]</td><td>[28]</td><td>[27]</td><td>[26]</td><td>[25]</td><td>[24]</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
</table>

background_v — background setting: v (default 0)

background_y — background setting: y (default 0)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xA918	y_avg_en_1	y_skip_1	y_avg_en_0	y_skip_0	RESERVED			
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	progressive/interlace							
	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
	RESERVED			CHID_repeat	len_256_512	frame_CHID_enb_ch0	byte_CHID_B_ch0	byte_CHID_A_ch0
	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]
	RESERVED		sav_eav_32_ctrl			frame_CHID_enb_ch1	byte CHID_B_ch1	byte CHID_A_ch1

y_skip_n — Downscaling ¼ using 4 or 2 rows average on bus n (average of row 0 & row 2) (Default 0)

- 1'b1 — 2 rows average
- 1'b0 — 4 rows average

y_avg_en_n — Downscaling enable or disable average on bus n (default 0)

- 1'b1 — enable
- 1'b0 — disable

progressive/interlace [4n+m] — Normal progressive/interleave mode select on bus n channel m (default 0)

- 1'b1 — interleave
- 1'b0 — progressive

byte_CHID_A_chN — bus N, CHID mode A enable when byte interleave. Add CHID to SAV/EAV bit [3:0] (default 0)

- 1'b0 — disable CHID insert
- 1'b1 — enable CHID insert

byte_CHID_B_chN — bus N, CHID mode B enable when byte interleave. Add CHID to HBI pixel bit [3:0] (default 0)

- 1'b0 — disable CHID insert
- 1'b1 — enable CHID insert

frame_CHID_enb_chN — bus N, frame CHID insert enable (default 0)

- 1'b0 — disable CHID insert
- 1'b1 — enable CHID insert

len_256_512: — CHID length select (default 0)

- 1'b0 — 256 bytes
- 1'b1 — 512 bytes

CHID repeat: — repeat current CHID to the whole row (default 0)

- 1'b0 — repeat disable
- 1'b1 — repeat enable

sav_eav_32_ctrl — SAV/EAV [3:2] configuration. (Default 0)

- [2] — register configuration enable

[1:0] register configuration value

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xA91C	RESERVED							p_n_mode
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	RESERVED							
	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
	RESERVED							
	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]
	RESERVED							

p_n_mode — for bus0 and bus1, pal or ntsc configuration
(Default 0)

1'b1 NTSC

1'b0 PAL

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xA920	RESERVED					sie_format_out_x		
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	RESERVED							
	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
	ch_enb_x							
	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]
	live_reb_sel_x							

sie_format_out_x: SIE output format (default 0)

3'b000 D1

3'b001 HD1

3'b010 CIF

3'b011 HCIF

ch_enb_x: For each SIE module, there are mostly 8 channels video stream input, this register is used to indicate each channel is valid or not for this SIE (default 0)

1'b1 valid

1'b0 not valid

live_reb_sel_x: For each SIE module, there are mostly 8 channels video stream input, this register is used to indicate each channel is live or rebuild frame for this SIE (default 0)

1'b1 rebuild frame

1'b0 live frame

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xA924	channel_sel_x[7:0]							
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	channel_sel_x[15:8]							
	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
	channel_sel_x[23:16]							
	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]
	channel_sel_x[31:24]							

channel_sel_x: The channel to be displayed in sub-window 0 ~ 7, 4 bit each window.

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xA928	scaler_cfg_x[7:0]							
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	scaler_cfg_x[15:8]							
	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
	scaler_cfg_x[23:16]							
	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]
	scaler_cfg_x[31:24]							

scaler_cfg_x: [3:2] X scaler
[1:0] Y scaler

2'b00 no down sample
2'b01 2x down sample
2'b10 4x down sample
2'b11 2x up sample (CIF to D1 or D1 to 4D1)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xA9F0	lostsync_intr_reg[7:0]							
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	lostsync_intr_reg[15:8]							

lostsync_intr_reg lost synchronization interrupt register

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xA9F4	single_intr_reg							
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	single_intr_en							

single_intr_reg one frame is display completed, this register is valid
single_intr_en single interrupt enable

NOTE: **BASED ON THE END SIGNAL SENT FROM BT.656 INTERFACE ENGINE, THIS MODULE UPDATES THE INTERRUPT STATUS REGISTER OF THE CORRESPONDING BT.656 CHANNEL.**

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xA9F8	dma_intr_reg[7:0]							
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	dma_intr_re g[15:8]							
	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
	dma_intr_en[7:0]							
	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]
	dma_intr_en[15:8]							

dma_intr_reg: DMA interrupt register
dma_intr_en: DMA interrupt enable

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xA9FC							intr_select	intr_enable

intr_enable interrupt enable

intr_select: select which interrupt is valid
0: single interrupt
1: DMA interrupt

Address	[31:0]
0xAA00	chid_cfg_ch0[31: 0]
0xAA04	chid_cfg_ch0[63:32]
0xAA08	chid_cfg_ch1[31: 0]
0xAA0C	chid_cfg_ch1[63:32]
0xAA10	chid_cfg_ch2[31: 0]
0xAA14	chid_cfg_ch2[63:32]
0xAA18	chid_cfg_ch3[31: 0]
0xAA1C	chid_cfg_ch3[63:32]
0xAA20	chid_cfg_ch4[31: 0]
0xAA24	chid_cfg_ch4[63:32]
0xAA28	chid_cfg_ch5[31: 0]
0xAA2C	chid_cfg_ch5[63:32]
0xAA30	chid_cfg_ch6[31: 0]
0xAA34	chid_cfg_ch6[63:32]
0xAA38	chid_cfg_ch7[31: 0]
0xAA3C	chid_cfg_ch7[63:32]
0xAA40	chid_cfg_ch8[31: 0]
0xAA44	chid_cfg_ch8[63:32]
0xAA48	chid_cfg_ch9[31: 0]
0xAA4C	chid_cfg_ch9[63:32]
0xAA50	chid_cfg_cha[31: 0]
0xAA54	chid_cfg_cha[63:32]
0xAA58	chid_cfg_chb[31: 0]
0xAA5C	chid_cfg_chb[63:32]
0xAA60	chid_cfg_chc[31: 0]
0xAA64	chid_cfg_chc[63:32]
0xAA68	chid_cfg_chd[31: 0]
0xAA6C	chid_cfg_chd[63:32]
0xAA70	chid_cfg_che[31: 0]
0xAA74	chid_cfg_che[63:32]
0xAA78	chid_cfg_chf[31: 0]
0xAA7C	chid_cfg_chf[63:32]

chid_cfg_chx:	[54]	chid_add_enable
	[53]	ddr_rd_enable
	[52:42]	chid col location
	[41:32]	chid line location
	[31:0]	ddr base address

NOTE: READ NEXT CHID FROM DDR WHEN (1) SYS_RESET FINISHES, AND (2) CURRENT CHID SENDS FINISH & CHID READ ENABLE

Address	[31:16]	[15:0]
0xAA80	len_valid_col_0	len_col_0
0xAA84	len_even_row_0	len_odd_row_0
0xAA88	len_odd_valid_row_0	len_odd_blank_row_0
0xAA8C	len_even_valid_row_0	len_even_blank_row_0
0xAA90	len_valid_col_1	len_col_1
0xAA94	len_even_row_1	len_odd_row_1
0xAA98	len_odd_valid_row_1	len_odd_blank_row_1
0xAA9C	len_even_valid_row_1	len_even_blank_row_1

len_col_0	PB0 total cycles per line (including blanking)
len_valid_col_0	PB0 valid cycles per line (SD: 1440, 1080P: 1920, etc.)
len_odd_row_0	PB0 total lines on odd field (including vertical blanking)
len_even_row_0	PB0 total lines on even field (including vertical blanking)
len_odd_blank_row_0	PB0 vertical blanking lines before odd field active lines
len_odd_valid_row_0	PB0 vertical odd field active lines
len_even_blank_row_0	PB0 vertical blanking lines before even field active lines
len_even_valid_row_0	PB0 vertical even field active lines
len_col_1	PB1 total cycles per line (including blanking)
len_valid_col_1	PB1 valid cycles per line (SD: 1440, 1080P: 1920, etc.)
len_odd_row_1	PB1 total lines on odd field (including vertical blanking)
len_even_row_1	PB1 total lines on even field (including vertical blanking)
len_odd_blank_row_1	PB1 vertical blanking lines before odd field active lines
len_odd_valid_row_1	PB1 vertical odd field active lines
len_even_blank_row_1	PB1 vertical blanking lines before even field active lines
len_even_valid_row_1	PB1 vertical even field active lines

Address	[31:16]	[15:0]
0xAAC0	Y_len_bus0_0[11:0]	X_len_ bus0_0[12:0]
0xAAC4	Y_st_ bus0_0[9:0]	X_st_ bus0_0 [9:0]
0xAAC8	Y_len_ bus0_1[11:0]	X_len_ bus0_1[12:0]
0xAACC	Y_st_ bus0_1 [9:0]	X_st_ bus0_1 [9:0]
0xAAD0	Y_len_ bus0_2[11:0]	X_len_ bus0_2[12:0]
0xAAD4	Y_st_ bus0_2 [9:0]	X_st_ bus0_2 [9:0]
0xAAD8	Y_len_ bus0_3[11:0]	X_len_ bus0_3[12:0]
0xAADC	Y_st_ bus0_3[9:0]	X_st_ bus0_3 [9:0]
0xAAE0	Y_len_bus1_0[11:0]	X_len_ bus1_0[12:0]
0xAAE4	Y_st_ bus1_0 [9:0]	X_st_ bus1_0 [9:0]
0xAAE8	Y_len_ bus1_1[11:0]	X_len_ bus1_1[12:0]
0xAAEC	Y_st_ bus1_1[9:0]	X_st_ bus1_1 [9:0]
0xAAF0	Y_len_ bus1_2[11:0]	X_len_ bus1_2[12:0]
0xAAF4	Y_st_ bus1_2 [9:0]	X_st_ bus1_2 [9:0]
0xAAF8	Y_len_ bus1_3[11:0]	X_len_ bus1_3[12:0]
0xAAFC	Y_st_ bus1_3 [9:0]	X_st_ bus1_3 [9:0]

In HD case, we may have 1 or 4 windows placed in one output bus. These registers set the parameters of each window. Addresses 0xAAC0 to 0xAADC are for bus0, and addresses 2E0 to 2FC are for bus1. In single window mode, only the registers of the first group are used.

X_len_busM_N	Set the horizontal active length of picture area in the current window N, bus M
Y_len_busM_N	Set the vertical active length of picture area in current window N, bus M
X_st_ busM_N	Set the starting horizontal location (in pixel) of valid picture in the window N, bus M
Y_st_ busM_N	Set the starting vertical location (in line) of valid picture in the window N, bus M

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xABE4	SD_CH3_ORG_PTR		SD_CH2_ORG_PTR		SD_CH1_ORG_PTR		SD_CH0_ORG_PTR	
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	SD_CH7_ORG_PTR		SD_CH6_ORG_PTR		SD_CH5_ORG_PTR		SD_CH4_ORG_PTR	
	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
	SD_CH11_ORG_PTR		SD_CH10_ORG_PTR		SD_CH9_ORG_PTR		SD_CH8_ORG_PTR	
	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]
	SD_CH15_ORG_PTR		SD_CH14_ORG_PTR		SD_CH13_ORG_PTR		SD_CH12_ORG_PTR	

SD_CHn_ORG_PTR	Input capture write pointer of channel n (n from 0 to 15) (Read only)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xABE8	ORG_DISP_CHN0_MAP							
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	ORG_DISP_CHN1_MAP							
	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
	ORG_DISP_CHN2_MAP							
	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]
	ORG_DISP_CHN3_MAP							
Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xABEC	ORG_DISP_CHN4_MAP							
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	ORG_DISP_CHN5_MAP							
	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
	ORG_DISP_CHN6_MAP							
	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]
	ORG_DISP_CHN7_MAP							
Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xABF0	ORG_DISP_CHN8_MAP							
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	ORG_DISP_CHN9_MAP							
	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
	ORG_DISP_CHN10_MAP							
	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]
	ORG_DISP_CHN11_MAP							
Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xABF4	ORG_DISP_CHN12_MAP							
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	ORG_DISP_CHN13_MAP							
	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
	ORG_DISP_CHN14_MAP							
	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]
	ORG_DISP_CHN15_MAP							

ORG_DISP_CHNn_MAP	Display re-mapping of each original channel (n from 0 to 15). (Read only)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xABF8				HD0_ORG_ENB	HD0_ORG_CHN_MAP[3:0]			
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
				HD1_ORG_ENB	HD1_ORG_CHN_MAP[3:0]			

HD0_ORG_ENB	HD channel 0 original image display enable(default 0)
HD0_ORG_CHN_MAP	HD channel 0 original image channel mapping Used to map HD channel 0 to 0 ~ 15 channel
HD1_ORG_ENB	HD channel 1 original image display enable(default 0)
HD1_ORG_CHN_MAP	HD channel 1 original image channel mapping Used to map HD channel 1 to 0 ~ 15 channel

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xABFC								video_ts_reg_in

video_ts_reg_in	Video timestamp input enable

0xB000 ~ 0xB028: Debug Control

Address	[15:0]
0xB000	Chip_ID

Chip_ID TW5866 Chip ID (Read only, default 5866)

Address	[15:0]
0xB004	Chip_sub_version

Chip_sub_version TW5866 sub version (read only, default F009)

Address	[11:0]
0xB010	ARB12_enable

ARB12_enable ARB12 clients enable

Bit [0] Audio data in request enable
Bit [1] Audio encode request enable
Bit [2] Audio decode request 0 enable
Bit [3] Audio decode request 1 enable
Bit [4] Reserved
Bit [5] H264 MVD request enable
Bit [6] SD mv_flag request enable
Bit [7] mux_core MD request enable
Bit [8] JPEG request enable
Bit [9] Reserved
Bit [10] HD mv_flag request enable
Bit [15:11] Reserved

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xB028						PLBK_CS_IN_SEL		

PLBK_CS_IN_SEL Playback cascade input select

3'b001: cascade input pin
3'b010: BT.1120 input channel 0
3'b100: BT.1120 input channel 1

0xC800 ~ 0xC804 -- JPEG Capture Register Map

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xC800	JPG_CAP_FMT_0		JPG_CAP_CH_0				JPG_BRST_CAP_0	JPG_SING_CAP_0
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
							JPG_DNS_0	JPG_PROG_0
Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xC804	JPG_CAP_FMT_1		JPG_CAP_CH_1				JPG_BRST_CAP_1	JPG_SING_CAP_1
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
							JPG_DNS_1	JPG_PROG_1

JPG_SING_CAP_n JPEG Path Command for Single capture for bus n
- 1 Start to capture next frame, de-activated when frame ends
- 0 No command

JPG_BRST_CAP_n JPEG Path Command for Burst capture for bus n
- 1 Start to capture frames until CPU set ENC command
- 0 No command

JPG_CAP_CH_n JPEG Path Capture channel Select for bus n

JPG_CAP_FMT_n JPEG Capture Path Format for bus n
- 00 D1 (For D1 frame)
- 01 CIF with ½ size in X (for QCIF frame mode)
- 10 (Reserved)
- 11 D1 with ½ size in X (for CIF frame)

JPG_DNS_n JPEG Capture Path Downscale Input for bus n
- 1 Downscale in Y to 1/2
- 0 Does not downscale

JPG_PROG_n JPEG Path channel n is progressive
- 1 Progressive (Not valid for TW5864B)
- 0 Interlaced (TW5864B default)

0xD000 ~ 0xD0FC: MJPEG Control

Address	[15:0]
0xD000	JPEG_QSCALE

JPEG_QSCALE   JPEG quantization scaling register.

The default value should be 16'h10

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xD004			JPG_NEWEST_BUF0		JPG_VLD_FRM0			
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	JPG_VLD_FRM_RES0							
	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
	JPG_VLD_FRM_CHID0[7:0]							
	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]
	JPG_VLD_FRM_CHID0[15:0]							

NOTE: THIS IS VALID FRAME INDICATION REGISTER. AFTER ONE FRAME OF PATH 0 IS STORED IN THE DDR, THE CORRESPONDING BIT OF THIS REGISTER BECOMES VALID. HARDWARE NOTIFIES NOW IT IS READY TO ENCODE THE FRAME IN DDR THROUGH THIS REGISTER. THIS IS A READ ONLY REGISTER.

JPG_VLD_FRM0   For every path, there are 4 buffers in DDR and every bit correspond to one buffer, and the order is bit 0 for buffer 0, bit 1 for buffer 1, and so on

JPG_NEWEST_BUF0   Most recent used buffer

JPG_VLD_FRM_RES0   Frame resolution, every buffer use 2 bits

00: D1

01: not used

10: CIF

11: HD1

JPG_VLD_FRM_CHID0   Channel ID, every buffer use 4 bits

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xD008			JPG_NEWEST_BUF1		JPG_VLD_FRM1			
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	JPG_VLD_FRM_RES1							
	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
	JPG_VLD_FRM_CHID1[7:0]							
	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]
	JPG_VLD_FRM_CHID1[15:0]							

NOTE: THIS IS A VALID FRAME INDICATION REGISTER USED FOR INDICATING THE PATH1 BUFFER STATUS.

JPG_VLD_FRM1 — For every path, there are 4 buffers in DDR and every bit correspond to one buffer, and the order is bit 0 for buffer 0, bit 1 for buffer 1, and so on

JPG_NEWEST_BUF1 — Which buffer is operated recently

JPG_VLD_FRM_RES1 — Frame resolution, every buffer use 2 bits

00: D1

01: not used

10: CIF

11: HD1

JPG_VLD_FRM_CHID1 — Channel ID, every buffer use 4 bits

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xD00C			HD_PATH1	HD_PATH0	BUFFER_SEL			ENCODE_EN

NOTE: THIS IS THE ENCODE INDICATION REGISTER. THROUGH THIS REGISTER, THE SOFTWARE KNOWS WHICH BUFFER IS ENCODED. PLEASE NOTE THAT HD_PATH0 AND HD_PATH1 CAN'T BE 1 AT THE SIMULTANEOUSLY. IF HD_PATH0 OR HD_PATH1 IS 1, BUFFER_SEL IS INVALID.

ENCODE_EN — Encode enable bit

BUFFER_SEL — Buffer select, 000-111 indicate all of the eight buffers of two paths. For example, 000 is buffer0 in path0, 001 is buffer1 in path0, and 111 are buffer3 in path1, and so on.

HD_PATH0 — Encode HD path0

HD_PATH1 — Encode HD path1

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xD010	ENCODE_COMP							

NOTE: **THROUGH POLLING THIS REGISTER, THE APPLICATION SOFTWARE KNOWS WHICH FRAME HAS BEEN ENCODED COMPLETELY. THIS REGISTER IS READ ONLY. FOR HD ENCODE, BIT [0] IS FOR HD PATH0 AND BIT [4] IS FOR HD PATH1.**

ENCODE_COMP	Encode complete

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xD014								CAP_ENABLE_0
0xD018								CAP_ENABLE_1

NOTE: **CHANNEL 0 CAPTURE ENABLE INDICATION REGISTER. APPLICATION SOFTWARE SHOULD WRITE 1 TO THIS BIT AFTER STARTING TO CAPTURE ONE FRAME USING REGISTER 0XC800**

CAP_ENABLE_n	Channel n capture enable indicate

Address	[31:0]
0xD01C	CAP_TIMEOUT_VALUE

NOTE: **THIS REGISTER IS THE MAXIMAL TIME INTERVAL BETWEEN CAPTURE REGISTER IS SET AND ONE FRAME HAS BEEN STORED IN THE DDR. USING THIS REGISTER TO ENHANCE SYSTEM ERROR-TOLERANCE. THE DEFAULT VALUE IS 0X80000000. NORMALLY APPLICATION SOFTWARE CAN SET THIS REGISTER TO 0X01000000, AND OTHER VALUE BASE ON DDR LOAD.**

CAP_TIMEOUT_VALUE	capture timeout register

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xD020	D1_MB_X							
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	D1_MB_Y							
	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
	HD1_MB_X							
	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]
	HD1_MB_Y							
0xD024	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
	CIF_MB_X							
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	CIF_MB_Y							

NOTE: **THESE REGISTERS DEFINE HOW LARGE FRAME WILL BE ENCODED. FOR EXAMPLE, THE FORMAT OF THE PAL MODE IN D1 RESOLUTION IS 720X576. THE D1_MB_X EQUALS TO 720/16, WHICH IS 45. THE D1_MB_Y EQUALS TO 576/16. THE DEFAULT VALUE OF HD1_MB_X, HD1_MB_Y, CIF_MB_X, AND CIF_MB_Y ARE 45, 18, 22, AND 18, CORRESPONDINGLY.**

D1_MB_X	how much macro block need be encoded in x axis for D1
D1_MB_Y	how much macro block need be encoded in y axis for D1
HD1_MB_X	how much macro block need be encoded in x axis for HD1
HD1_MB_Y	how much macro block need be encoded in y axis for HD1
CIF_MB_X	how much macro block need be encoded in x axis for CIF
CIF_MB_Y	how much macro block need be encoded in y axis for CIF

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xD028	D1_HD1_PIXEL_PER_LINE[7:0]							
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	D1_HD1_PIXEL_PER_LINE[9:8]							
	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
	CIF_PIXEL_PER_LINE[7:0]							
	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]
	CIF_PIXEL_PER_LINE[9:8]							
0xD02C	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
	D1_LINE_PER_FRAME[7:0]							
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	D1_LINE_PER_FRAME [9:8]							
	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
	CIF_HD1_LINE_PER_FRAME [7:0]							
	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]
	CIF_HD1_LINE_PER_FRAME[9:8]							

D1_HD1_PIXEL_PER_LINE pixel per line for d1 and hd1

CIF_PIXEL_PER_LINE pixel per line for cif

D1_LINE_PER_FRAME line per frame for d1

CIF_HD1_LINE_PER_FRAME line per frame for cif and hd1

Address	[31:0]
0xD040	JPG_LENGTH0
0xD044	JPG_LENGTH1
0xD048	JPG_LENGTH2
0xD04C	JPG_LENGTH3
0xD050	JPG_LENGTH4
0xD054	JPG_LENGTH5
0xD058	JPG_LENGTH6
0xD05C	JPG_LENGTH7

JPG_LENGTHx jpeg stream length registers. For HD, JPG_LENGTH0 is for HD path0 and JPG_LENGTH4 is for HD path1.

Address	[31:16]	[15:0]
0xD060	JPG_TIMESTAMP1	JPG_TIMESTAMP0
0xD064	JPG_TIMESTAMP3	JPG_TIMESTAMP2
0xD068	JPG_TIMESTAMP5	JPG_TIMESTAMP4
0xD06C	JPG_TIMESTAMP7	JPG_TIMESTAMP6

JPG_TIMESTAMPx Video timestamp, For HD, JPG_TIMESTAMP0 is for HD path0 and JPG_TIMESTAMP4 is for HD path1.

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xD078	RESERVED							GRAB_EN
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	RESERVED					PATH_NUM	BUFFER_BUM	
	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
	RESERVED						GRAB_RESOLUTION	
	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]
	RESERVED							

NOTE: **THIS REGISTER IS USED FOR GRABBING FUNCTIONALITY. BEFORE SETTING GRAB_EN TO START TO GRAB, THE VALID FRAME MUST BE STORED IN THE CORRESPONDING BUFFER.**

GRAB_EN grab enable

BUFFER_BUM grab in which buffer

PATH_BUM grab in which path

GRAB_RESOLUTION frame resolution

00 D1

01 HD

10 CIF

11 HD1

Address	[7:4]	[3]	[2]	[1]	[0]
0xD090		HD_FRAME_STORE_COMP_1	HD_FRAME_STORE_COMP_0	HD_CAP_1	HD_CAP_0

HD_CAP_0 capture HD one frame in path0

HD_CAP_1 capture HD one frame in path1

HD_FRAME_STORE_COMP_0 capture complete in path0

HD_FRAME_STORE_COMP_1 capture complete in path1

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xD094	HD_PIXEL_PER_LINE_0[7:0]							
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	HD_LINE_PER_FRAME_0[3:0]				HD_PIXEL_PER_LINE_0[11:8]			
	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
	HD_LINE_PER_FRAME_0[11:4]							
	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]
	RESERVE		HD_PART_PER_LINE_0					

HD_PIXEL_PER_LINE_0 pixel per line for HD in path0

HD_LINE_PER_FRAME_0 line per frame for HD in path0

HD_PART_PER_LINE_0 should be set to (HD_PIXEL_PER_LINE_0/128)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xD098	HD_LAST_PART_DNUM_0[7:0]							
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
				HD_IP_IND_0	HD_LAST_PART_DNUM_0[11:8]			
	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
	HD_MB_X_0							
	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]
	HD_MB_Y_0							

HD_LAST_PART_DNUM_0 set to (HD_PIXEL_PER_LINE_0%128)

HD_IP_IND_0 interlace or progressive indication
0: interlace
1: progressive

HD_MB_X_0 set to (HD_PIXEL_PER_LINE_0/16)

HD_MB_Y_0 set to (HD_LINE_PER_FRAME_0/16)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xD09C	HD_PIXEL_PER_LINE_1[7:0]							
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	HD_LINE_PER_FRAME_1[3:0]				HD_PIXEL_PER_LINE_1[11:8]			
	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
	HD_LINE_PER_FRAME_1[11:4]							
	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]
	RESERVE		HD_PART_PER_LINE_1					

HD_PIXEL_PER_LINE_1 pixel per line for HD in path1

HD_LINE_PER_FRAME_1 line per frame for HD in path1

HD_PART_PER_LINE_1 should be set to (HD_PIXEL_PER_LINE_1/128)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xD0A0	HD_LAST_PART_DNUM_1[7:0]							
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
				HD_IP_IND_1	HD_LAST_PART_DNUM_1[11:8]			
	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
	HD_MB_X_1							
	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]
	HD_MB_Y_1							

HD_LAST_PART_DNUM_1 — if (HD_PIXEL_PER_LINE_1%128 == 0) set 32
Else equal to (HD_PIXEL_PER_LINE_1%128)

HD_IP_IND_1 — interlace or progressive indication
0 interlace
1 progressive

HD_MB_X_1 — set to (HD_PIXEL_PER_LINE_1/16)

HD_MB_Y_1 — set to (HD_LINE_PER_FRAME_1/16)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xD07C	RESERVED							JPG_NTSC

JPG_NTSC — 1 NTSC
0 PAL (default)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xD0F8	RESERVE							PCI_MODE

PCI_MODE — 1 pci mode, the stream will be pushed up to system memory through pci master

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xD0FC	RESERVE							SOFT_RST
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	RESERVE							
	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
	RESERVE							
	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]
	ENC_COMP_RST_EN	CAP0_RST_EN	CAP1_RST_EN	TIMEOUT_ENABLE	ENCODE_TIMEOUT_ENB	RESERVE		

NOTE: IN SOME SPECIAL SITUATIONS, SUCH AS THE ORIGINAL SOURCE VIDEO IS NOT STABLE MAKING THE JPEG ENCODER ENTERS INTO THE INCORRECT STATUS, THE APPLICATION SOFTWARE CAN RESET JPEG MODULE ALONE WITHOUT AFFECTING OTHER PROCESS. SET IT TO 1 TO RESET, AND THEN SET IT BACK TO 0 TO RESUME. AFTER THIS, JPEG CORE CAN WORK AGAIN NORMALLY.

SOFT_RST — 1: start reset
0: reset complete

ENCODE_TIMEOUT_ENB — encode timeout enable

TIMEOUT_ENABLE — capture timeout enable

ENC_COMP_RST_EN — encode logic reset enable after compete one frame encode process, this bit should always be set to 1

CAP0_RST_EN — capture reset enable for path 0, which will enable watch dog logic, in noisy environment this bit should be set to 1. Anyway it is better to set this bit to 1

CAP1_RST_EN — capture reset enable for path 1, which will enable watch dog logic, in noisy environment this bit should be set to 1. Anyway it is better to set this bit to 1

0xD800 ~ 0xD93C: DDR mapping/EMUIF

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xD800 + 4* N	chN_encode_base_address[7:0]							
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	chN_encode_frame_number			chN_encode_base_address[12:8]				
	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
	RESERVED					chN_encode_type		
	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]
	RESERVED							

ChN_encode_base_address — The channel N encoding frame buffer base address.
N = 0 ~ 15

ChN_encode_frame_number

1	2 original frames and 2 reference frames
3	4 original frames and 4 reference frames
Others	Reserved

ChN_encode_type

0	CIF mode
1	D1 mode
2	H960
3	Half D1
4	720P
5	1080i
6	Reserved
7	Reserved

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xD840 + 4 * N	chN_decode_base_address[7:0]							
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	chN_decode_frame_number			chN_decode_base_address[12:8]				
	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
	RESERVED					chN_decode_type		
	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]
	RESERVED							

ChN_decode_base_address — The channel N decoding frame buffer base address N = 0 ~ 15

ChN_decode_frame_number

1	2 original frames and 2 reference frames
3	4 original frames and 4 reference frames
Others	Reserved

ChN_decode_type

0	CIF mode
1	D1 mode
2	H960
3	Half D1
4	720P
5	1080i
6	Reserved
7	Reserved

address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xD880	jpeg_base_address[7:0]							
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	RESERVED			jpeg_base_address[12:8]				
	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
	RESERVED							
	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]
	RESERVED							

jpeg_base_address jpeg base address based page, need 8M byte (16 pages) to buffer the jpeg data

address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xD888	mvt_base_address[7:0]							
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	RESERVED			mvt_base_address[12:8]				
	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
	RESERVED							
	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]
	RESERVED							

mvt_base_address motion vector temporary data base address based page, need 2 Mbyte (4pages) to buffer the motion vector temporary data

address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xD88C	mvr_base_address							
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	RESERVED							
	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
	RESERVED							
	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]
	RESERVED							

mvr_base_address motion vector result data base address based page, need 1 Mbyte (2pages) to buffer the motion vector result data

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xD890	audio_base_address[7:0]							
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	RESERVED			audio_base_address[12:8]				
	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
	RESERVED							
	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]
	RESERVED							

audio_base_address Audio base address based page, need 1M byte (2pages) to buffer the audio data

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xD894	revbuf_base_address[7:0]							
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	revbuf_frame_num [2:0]			revbuf_base_address[12:8]				
	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
	revbuf_frame_num[10:3]							
	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]
	RESERVED							revbuf_frame_num[11]

revbuf_base_address Reverse buffer base address

revbuf_frame_num Reverse buffer frame number parameter

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xD898	tembuf_base_address[7:0]							
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	tembuf_frame_num [2:0]			tembuf_base_address[12:8]				
	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
	tembuf_frame_num[10:3]							
	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]
	RESERVED							tembuf_frame_num[11]

tembuf_base_address temporary buffer base address based page

tembuf_frame_num temporary buffer frame number parameter

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xD89C							hd1_map_mode	cif_map_mode
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	RESERVED							
	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
	RESERVED							
	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]
	RESERVED							

hd1_map_mode	0	2 half D1 in 1 D1 frame space
	1	1 half D1 in 1 D1 frame space
cif_map_mode	0	4 CIFs in 1 D1 frame space
	1	1 CIF in 1 D1 frame space

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xD8A0	me_ref_frm_hptr[7:0]							
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	RESERVED				me_acc_type		me_ref_frm_hptr[9:8]	
	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
	RESERVED							
	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]
	RESERVED							

me_ref_frm_hptr	ME (motion estimation) access reference higher pointer	
me_acc_type	0	access normal frame
	1	access temporary frame
	2	access reverse frame
	3	reserved

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xD8A4	lpf_ref_frm_hptr[7:0]							
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	RESERVED				lpf_acc_type		lpf_ref_frm_hptr[9:8]	
	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
	RESERVED							
	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]
	RESERVED							

lpf_ref_frm_hptr	LPF reconstruction buffer pointer higher bits [11:2]. (Higher bits used for decoding purpose only) Note: pointer lower bits [1:0] specified at register 0x0210[13:12]	
lpf_acc_type	0	access normal frame
	1	access temporary frame
	2	access reverse frame
	3	reserved

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xD8A8	Ch3_plk_acc_type		Ch2_plk_acc_type		Ch1_plk_acc_type		Ch0_plk_acc_type	
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	Ch7_plk_acc_type		Ch6_plk_acc_type		Ch5_plk_acc_type		Ch4_plk_acc_type	
	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
	Ch11_plk_acc_type		Ch10_plk_acc_type		Ch9_plk_acc_type		Ch8_plk_acc_type	
	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]
	Ch15_plk_acc_type		Ch14_plk_acc_type		Ch13_plk_acc_type		Ch12_plk_acc_type	

Chn_plk_acc_type	0	access normal frames
	1	access temporary frames
	2	access reverse frames
	3	reserved

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xD8B0 + 4 * N	RESERVED	BAND_WEIGHT_REQ0_BUSN						
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	RESERVED	BAND_WEIGHT_REQ1_BUSN						
	[23]	[22]	[21]	[20]	[18]	[18]	[17]	[16]
	RESERVED	BAND_WEIGHT_REQ2_BUSN						
	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]
	RESERVED	BAND_WEIGHT_REQ3_BUSN						

N = 0 ~ 3

BAND_WEIGHT_REQ0_BUSN	Bandwidth allocated for request 0 of bus N.
BAND_WEIGHT_REQ1_BUSN	Bandwidth allocated for request 1 of bus N.
BAND_WEIGHT_REQ2_BUSN	Bandwidth allocated for request 2 of bus N.
BAND_WEIGHT_REQ3_BUSN	Bandwidth allocated for request 3 of bus N

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xD8C0	REQ_CNT_BUS0_DBG[7:0]							
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	REQ_CNT_BUS0_DBG[15:8]							
	[23]	[22]	[21]	[20]	[18]	[18]	[17]	[16]
	REQ_CNT_BUS1_DBG[7:0]							
	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]
	REQ_CNT_BUS1_DBG[15:8]							
Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xD8C4	REQ_CNT_BUS2_DBG[7:0]							
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	REQ_CNT_BUS2_DBG[15:8]							
	[23]	[22]	[21]	[20]	[18]	[18]	[17]	[16]
	RESERVED							
	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]
	RESERVED							

REQ_CNT_BUS0_DBG — Request count of bus0, debug only.

REQ_CNT_BUS1_DBG — Request count of bus1, debug only.

REQ_CNT_BUS2_DBG — Request count of bus2, debug only.

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xD8C8	rev_ fdip_baddr[7:0]							
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	rev_fdip_fnum[2:0]			rev_ fdip_baddr[12:8]				
	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
	rev_fdip_fnum[10:3]							
	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]
	RESERVED							

rev_ fdip_baddr — reverse buffer for display base address based page

rev_fdip_fnum — reverse buffer for display frame number parameter

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xD8CC	tmp_ fdip_baddr[7:0]							
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	tmp_ fdip_fnum[2:0]			tmp_ fdip_baddr[12:8]				
	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
	tmp_ fdip_fnum[10:3]							
	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]
	RESERVED							

tmp_ fdip_baddr — temporary buffer for display base address based page

tmp_ fdip_fnum — temporary buffer for display frame number parameter

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xD8D0	ext_rec_frm_ptr[7:0]							
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	ext_rec_hd1_map_mode	ext_rec_cif_map_mode	ext_rec_acc_type		ext_rec_frm_ptr[11:8]			
	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
	RESERVED							
	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]
	RESERVED							

ext_rec_frm_ptr	Second set of reconstruction frame pointer for display purpose.	
ext_rec_acc_type	0	normal buffers access
	1	temporary buffers access
	2	reverse buffers access
	3	reserved
ext_rec_cif_map_mode	0	4 channels cif use 1 D1 space
	1	1 channel cif use 1 D1 space
ext_rec_hd1_map_mode	0	2 channels half d1 use 1 D1 space
	1	1 channel half d1 use 1 D1 space

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xD900 + 4 * N	chN_rfd_base_address[7:0]							
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	chN_rfd_frame_number			chN_rfd_base_address[12:8]				
	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
	RESERVED			chN_ext_rec_enb	chN_ds_y		chN_ds_x	
	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]
	chN dis frm type(RO)			RESERVED				

Channel # N = 0 ~ 15

ChN_rfd_base_address ChN reconstruction buffer base address in DDR

ChN_rfd_frame_number 1 2 display frames per channel
3 4 display frames per channel
Others reserved

ChN_ds_x
0 X direction without down scale
1 X direction 1/2 down scale
2 X direction 1/4 down scale
3 Reserved

ChN_ds_y
0 Y direction without down scale
1 Y direction 1/2 down scale
2 Y direction 1/4 down scale
3 Reserved

ChN_ext_rec_enb
0 disable the 2nd (display) set of reconstruction frame buffer
2 enable the 2nd (display) set of reconstruction frame buffer

ChN_dis_frm_type(RO) after down scale frame type
0 CIF
1 D1
2 H960
3 Half D1
4 720p
5 1080i/p
6 Reserved
7 2nd set display buffer invalid

0xE000 ~ 0xFC00: Motion Vector

Address	[31:0]
0xE000 -0xE7FC	ME_MV_VEC

ME_MV_VEC — ME Motion Vector data (within a frame) for video analytic purpose (Four bytes for a quad-MB block)

E.g., ME quad-MB block ID 0, 1, ...

ME_MV_VEC[0]	address : 0xE000
ME_MV_VEC[1]	address : 0XE004
ME_MV_VEC[1FF]	address : 0xE7FC

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xFC00	MV_LEN[2:0]			DSP_WR_OF	MV_DSP_INTR	MV_EOF	MV_BK1_FULL	MV_BK0_FULL
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
				MV_LEN[7:3]				

MV_BK0_FULL	MV ping-pong buffer 0 full status, write "1" to clear
MV_BK1_FULL	MV ping-pong buffer 1 full status, write "1" to clear
MV_EOF	Slice end status, write "1" to clear
MV_DSP_INTR	MV encode interrupt status, write “1” to clear
DSP_WR_OF	MV write memory overflow, write "1" to clear
MV_LEN	MV stream length

0x18000 ~ 0x181FC: PCI Master

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x18000	JPEG_ INTR	TIMER_INTR	PREV_OVERFLOW_INTR	PREV_EOF_INTR			VLC_DONE_INTR	
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
						HD_PREV_INTR	GRAB_EOF_INTR	AUDIO_EOF_INTR
	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]
							AD_INTR_REG	IIC_DONE_INTR

This register is interrupt flag register. Write 1 to clear the corresponding bit.

VLC_DONE_INTR VLC coding done interrupt

PREV_EOF_INTR SD preview EOF interrupt

PREV_OVERFLOW_INTR Preview overflow interrupt

TIMER_INTR On-chip RTC interrupt

JPEG_ INTR JPEG interrupt

AUDIO_EOF_INTR Audio eof interrupt

GRAB_EOF_INTR Raw video grabbing EOF interrupt

HD_PREV_INTR HD prev EOF interrupt

IIC_DONE_INTR I2C done interrupt

AD_INTR_REG Front-end video exception interrupt (e.g.: video lost, video format changed)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x18004	JPEG_MAST_ENB	MCU_TIMER_INTR_ENB	PREV_OVFW_INTR_ENB	PREV_MAST_ENB	AD_MAST_ENB	MVD_VLC_MAST_ENB		PCI_MAST_ENB
	[15:8]							
								AU_MAST_ENB
	[23:16]							
	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]
	MV_MAST_ENB	PCI_TAR_BURST_ENB[4:0]					AD_INTR_ENB	IIC_INTR_ENB

PCI_MAST_ENB		**PCI master enable**
MVD_VLC_MAST_ENB		**MVD & VLC master enable**
AD_MAST_ENB		**Front-end Video vsync master enable**
PREV_MAST_ENB		**Preview master enable**
PREV_OVFW_INTR_ENB		**Preview overflow interrupt enable**
MCU_TIMER_INTR_ENB		**Timer interrupt enable**
JPEG_MAST_ENB		**JPEG master enable**
AU_MAST_ENB		**Audio Transfer enable**
IIC_INTR_ENB		**I2C interrupt enable**
AD_INTR_ENB		**Front-end Video interrupt enable**
PCI_TAR_BURST_ENB	[0]	**Target burst enable**
PCI_TAR_BURST_ENB	[1]	**VLC stream burst enable**
PCI_TAR_BURST_ENB	[2]	**DDR burst enable**
PCI_TAR_BURST_ENB	[4:3]	**Reserved**
MV_MAST_ENB		**MV master enable**

Address	[15:0]
0x18008	PREV_INTR_REG
	[31:16]
	AU_INTR_REG

The interrupt status register of each individual preview video and audio channel.
PREV_EOF_INTR is the "OR" of all bits of PREV_INTR_REG.
AUDIO_EOF_INTR is the "OR" of all bits of AU_ITNR_REG.

PREV_INTR_REG[n] Preview EOF interrupt flag of channel n, n = 0 ~ 15

AU_INTR_REG[n] Audio EOF interrupt flag of channel n, n = 0 ~ 15

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x1800C	PCI_JPEG_INTR_ENB		PCI_RREV_OF_INTR_ENB	PCI_PREV_INTR_ENB			PCI_VLC_INTR_ENB	
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
						PCI_HD _PREV _INTR_ENB	PCI_GRAB_INTR_ENB	PCI_AUD_INTR_ENB

PCI_VLC_INTR_ENB VLC interrupt enable

PCI_PREV_INTR_ENB Preview interrupt enable

PCI_PREV_OF_INTR_ENB Preview overflow interrupt enable

PCI_JPEG_INTR_ENB JPEG interrupt enable

PCI_AUD_INTR_ENB Preview interrupt enable

PCI_GRAB_INTR_ENB Raw video data grabbing interrupt enable

PCI_HD_PREV_INTR_ENB HD prev interrupt enable

Address	[15:0]
0x18010	PREV_BUF_FLAG
	[31:16]
	AUDIO_BUF_FLAG

Every channel of preview and audio have ping-pong buffers in system memory, this register is the buffer flag to notify software which buffer is been operated.

PREV_BUF_FLAG Preview buffer A/B flag

AUDIO_BUF_FALG Audio buffer A/B flag

Address	[7:0]							
0x18014	IIC_DATA							
	[15:8]							
	IIC_REG_ADDR							
	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
	IIC_DEV_ADDR							IIC_RW
	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]
								IIC_DONE

IIC_DATA	register data
IIC_REG_ADDR	register address
IIC_RW	rd/wr flag rd=1, wr=0
IIC_DEV_ADDR	device address
IIC_DONE	iic done, software kick off one time iic transaction through setting this bit to 1.Then poll this bit, value 1 indicate iic transaction have completed, if read, valid data have been stored in iic_data

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x18018								APP_SOFT_RST
	[31:16]							
	PCI_INF_VERSION							

APP_SOFT_RST	application software soft reset
PCI_INF_VERSION	PCI interface version, it is read only

Address	[31:0]
0x1801C	VLC_CRC_REG
0x18020	VLC_MAX_LENGTH

VLC_CRC_REG	vlc stream crc value, it is calculated in pci module
VLC_MAX_LENGTH	vlc max length, it is defined by software based on software assign memory space for vlc

Address	[31:0]	
	vlc_debug (0x1807C[2]) = 1	vlc_debug (0x1807C[2]) = 0
0x18024	VLC_LENGTH	HD_PREV_INTR_REG
0x18028	VLC_INTRA_CRC_I_REG	HD_PREV_BUF_FLAG
0x1802C	VLC_INTRA_CRC_O_REG	HD_PREV_CONF
0x18030	VLC_PAR_CRC_REG	HD_CH0_XY_SIZE
0x18034	VLC_PAR_LENGTH_REG	HD_CH1_XY_SIZE
0x18038	VLC_PAR_I_REG	VLC_EOF_CNT
0x1803C	VLC_PAR_O_REG	VLC_DONE_INTR_CNT

VLC_LENGTH	VLC length of one frame
VLC_INTRA_CRC_I_REG	VLC original CRC value
VLC_INTRA_CRC_O_REG	VLC original CRC value
VLC_PAR_CRC_REG	MV stream CRC value, it is calculated in PCI module
VLC_PAR _LENGTH_REG	MV length
VLC_PAR_I_REG	MV original crc value
VLC_PAR_O_REG	MV original crc value
HD_PREV_INTR_REG	HD preview interrupt register
HD_PREV_BUF_FLAG	HD preview buffer flag register
HD_PREV_CONF	HD preview config register
HD_CH0_XY_SIZE	HD preview path0 resolution
HD_CH1_XY_SIZE	HD preview path1 resolution
VLC_EOF_CNT	VLC EOF number (for debug)
VLC_DONE_INTR_CNT	VLC interrupt number (for debug)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x18040							PREV_PCI_ENB_CHN	
	[31:16]							
	PREV_NONREALTIME_CNT[15:0]							
Address	[7:0]							
0x18044	PREV_FRAME_FORMAT_IN[7:0]							
	[15:8]							
	PREV_FRAME_FORMAT_IN[15:8]							
	[31:16]							
	PREV_NONREALTIME_CNT[31:16]							

Preview bus4 enable register, only channel2 and channel3 of bus0 can be used to bus4.Because format setting is faced on bus, if the channel2 or channel3 is defined to bus4, it can use other format for bus0

PREV_PCI_ENB_CHN [0] Channel 2 is used as bus 4

PREV_PCI_ENB_CHN [1] Channel 3 is used as bus 4

PREV_NONREALTIME_CNT Non-real-time hold counter

PREV_FRAME_FORMAT_IN [1:0] bus0 frame format

00	CIF
01	QCIF
10	4CIF
11	D1

PREV_FRAME_FORMAT_IN [3:2] bus1 frame format

00	CIF
01	QCIF
10	4CIF
11	D1

PREV_FRAME_FORMAT_IN [5:4] bus2 frame format

00	CIF
01	QCIF
10	4CIF
11	D1

PREV_FRAME_FORMAT_IN [7:6] bus3 frame format

00	CIF
01	QCIF
10	4CIF
11	D1

PREV_FRAME_FORMAT_IN [8] Bus0 progressive/interlace flag

0	interlace
1	progressive

PREV_FRAME_FORMAT_IN [9] Bus1 progressive/interlace flag

0 interlace

1 progressive

PREV_FRAME_FORMAT_IN [10] Bus2 progressive/interlace flag

0 interlace

1 progressive

PREV_FRAME_FORMAT_IN [11] Bus3 progressive/interlace flag

0 interlace

1 progressive

PREV_FRAME_FORMAT_IN [12] PAL/NTSC format select,

0 PAL

1 NTSC

PREV_FRAME_FORMAT_IN [14:13] Bus4 frame format

00 CIF

01 QCIF

10 4CIF

11 D1

PREV_FRAME_FORMAT_IN [15] Bus4 progressive/interlace flag

0 PAL

1 NTSC

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x18048								IIC_EN

IIC_EN IIC enable

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x1804C							MCU_TIMER_INTR_COUNT	

MCU_TIMER_INTR_COUNT Timer interrupt interval

00 1ms

01 2ms

10 4ms

11 8ms

Address	[31:0]
0x18050	JPEG_MAX_LENGTH

JPEG_MAX_LENGTH Define the jpeg operation max length, during reset, it will be initialized to default value 100KB

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x18054							PREV_MV_BUF_BUM	VLC_MV_BUF_NUM

This register defines the maximum number buffer in system memory, which indicates it can store the number of mv data for one channel. It can be 2 or 4.

VLC_MV_BUF_NUM	1	4 buffers
	0	2 buffers
PREV_MV_BUF_NUM	1	4 buffers
	0	2 buffers

Address	[31:0]
0x18058	PREV_MV_BUF_FLAG
0x1805C	VLC_MV_BUF_FLAG

Every channel use 2 bit to indicate which buffer is being operated. For 2 buffers mode, only the low bit of two bits is valid.

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x18060	JPEG_INTR_REG							

Because JPEG have 8 buffers separately, so using this registers to indicate interrupt status for every buffers. This is secondary interrupt status register. Treat the "OR" operation of the JPEG_INTR_REG [7:0] as a single bit JPEG end of file interrupt.

JPEG_INTR_REG	JPEG interrupt register

Address	[31:0]
0x18064	INTR_OUTPUT_ENABLE_REG

This register is used to control which interrupt can be valid in the interrupt line.

INTR_OUTPUT_ENABLE_REG	Interrupt output enable register

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x1807c						VLC_DEBUG		

VLC_DEBUG	Select which registers are read out (0x18024~0x1803c)

Address	[31:0]
0x18080	VLC stream base address
0x18084	MV stream base address

VLC_STREAM_BASE_ADDR — The base address of VLC stream in the DDR memory

MV_STREAM_BASE_ADDR — The base address of MV stream in the DDR memory

0x180A0 – 0x180BC: Audio Burst Base Address

Address	[31:0]
0x180a0	Audio Channel 0 – channel 3 bank A base address
0x180a4	Audio Channel 0 – channel 3 bank B base address
0x180a8	Audio Channel 4 – channel 7 bank A base address
0x180ac	Audio Channel 4 – channel 7 bank B base address
0x180b0	Audio Channel 8 – channel 11 bank A base address
0x180b4	Audio Channel 8 – channel 11 bank B base address
0x180b8	Audio Channel 12 – channel 15 bank A base address
0x180bc	Audio Channel 12 – channel 15 bank B base address

0x180C0 – 0x180DC: JPEG Burst Base Address

Address	[31:0]
0x180c0	jpeg buffer0 base address
0x180c4	jpeg buffer1 base address
0x180c8	jpeg buffer2 base address
0x180cc	jpeg buffer3 base address
0x180d0	jpeg buffer4 base address
0x180d4	jpeg buffer5 base address
0x180d8	jpeg buffer6 base address
0x180dc	jpeg buffer7 base address

0x180E0: Grab Buffer Base Address

Address	[31:0]
0x180e0	grab buffer base address

0x180F0 – 0x180FC: HD Preview Base Address

Address	[31:0]
0x180f0	hd preview buffer0 base address
0x180f4	hd preview buffer1 base address
0x180f8	hd preview buffer2 base address
0x180fc	hd preview buffer3 base address

0x18100 – 0x1817C: Preview Base Address

Address	[31:0]
0x18100	Preview Channel 0 bank A base address
0x18104	Preview Channel 0 bank B base address
0x18108	Preview Channel 1 bank A base address
0x1810c	Preview Channel 1 bank B base address
0x18110	Preview Channel 2 bank A base address
0x18114	Preview Channel 2 bank B base address
0x18118	Preview Channel 3 bank A base address
0x1811c	Preview Channel 3 bank B base address
0x18120	Preview Channel 4 bank A base address
0x18124	Preview Channel 4 bank B base address
0x18128	Preview Channel 5 bank A base address
0x1812c	Preview Channel 5 bank B base address
0x18130	Preview Channel 6 bank A base address
0x18134	Preview Channel 6 bank B base address
0x18138	Preview Channel 7 bank A base address
0x1813c	Preview Channel 7 bank B base address
0x18140	Preview Channel 8 bank A base address
0x18144	Preview Channel 8 bank B base address
0x18148	Preview Channel 9 bank A base address
0x1814c	Preview Channel 9 bank B base address
0x18150	Preview Channel 10 bank A base address
0x18154	Preview Channel 10 bank B base address
0x18158	Preview Channel 11 bank A base address
0x1815c	Preview Channel 11 bank B base address
0x18160	Preview Channel 12 bank A base address
0x18164	Preview Channel 12 bank B base address
0x18168	Preview Channel 13 bank A base address
0x1816c	Preview Channel 13 bank B base address
0x18170	Preview Channel 14 bank A base address
0x18174	Preview Channel 14 bank B base address
0x18178	Preview Channel 15 bank A base address
0x1817c	Preview Channel 15 bank B base address

0x18180 – 0x181BC: VLC MV Flag Base Address

Address	[31:0]
0x18180	VLC MV Flag Channel 0 base address
0x18184	VLC MV Flag Channel 1 base address
0x18188	VLC MV Flag Channel 2 base address
0x1818c	VLC MV Flag Channel 3 base address
0x18190	VLC MV Flag Channel 4 base address
0x18194	VLC MV Flag Channel 5 base address
0x18198	VLC MV Flag Channel 6 base address
0x1819c	VLC MV Flag Channel 7 base address
0x181a0	VLC MV Flag Channel 8 base address
0x181a4	VLC MV Flag Channel 9 base address
0x181a8	VLC MV Flag Channel 10 base address
0x181ac	VLC MV Flag Channel 11 base address
0x181b0	VLC MV Flag Channel 12 base address
0x181b4	VLC MV Flag Channel 13 base address
0x181b8	VLC MV Flag Channel 14 base address
0x181bc	VLC MV Flag Channel 15 base address

0x181C0 – 0x181FC: PREV MV Flag Base Address

Address	[31:0]
0x181c0	PREV MV flag Channel 0 base address
0x181c4	PREV MV flag Channel 1 base address
0x181c8	PREV MV flag Channel 2 base address
0x181cc	PREV MV flag Channel 3 base address
0x181d0	PREV MV flag Channel 4 base address
0x181d4	PREV MV flag Channel 5 base address
0x181d8	PREV MV flag Channel 6 base address
0x181dc	PREV MV flag Channel 7 base address
0x181e0	PREV MV flag Channel 8 base address
0x181e4	PREV MV flag Channel 9 base address
0x181e8	PREV MV flag Channel 10 base address
0x181ec	PREV MV flag Channel 11 base address
0x181f0	PREV MV flag Channel 12 base address
0x181f4	PREV MV flag Channel 13 base address
0x181f8	PREV MV flag Channel 14 base address
0x181fc	PREV MV flag Channel 15 base address

The above registers are pci base address registers. Application software will initialize them to tell chip where the corresponding stream will be dumped to. Application software will select appropriate base address interval based on the stream length.

0x1C000 ~ 0x1CFFF: Analog Front-end

Note: The front-end registers below are represented with offset address. The actual address is derived with 0x1C000 + 4 * offset

Note:
Register offset 0x000 ~ 0x1FF is for the first set of quad video/audio decoder
Register offset 0x200 ~ 0x3FF is for the second set of quad video/audio decoder

#	Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	0x000	VDLOSS*	HLOCK*	SLOCK*	FLD*	VLOCK*	NOVIDEO*	MONO*	DET50*
1	0x010								
2	0x020								
3	0x030								
4	0x200								
5	0x210								
6	0x220								
7	0x230								

*** Read only bits**

VDLOSS	1	Video not present. (sync is not detected in number of consecutive line periods specified by MISSCNT register)
	0	Video detected.
HLOCK	1	Horizontal sync PLL is locked to the incoming video source.
	0	Horizontal sync PLL is not locked.
SLOCK	1	Sub-carrier PLL is locked to the incoming video source.
	0	Sub-carrier PLL is not locked.
FLD	1	Even field is being decoded.
	0	Odd field is being decoded.
VLOCK	1	Vertical logic is locked to the incoming video source.
	0	Vertical logic is not locked.
NOVIDEO	Reserved for TEST.	
MONO	1	No color burst signal detected.
	0	Color burst signal detected.
DET50	0	60Hz source detected
	1	50Hz source detected
	The actual vertical scanning frequency depends on the current standard invoked.	

	Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	0x001	VCR*	WKAIR*	WKAIR1*	VSTD*	NINTL*	VSHP		
1	0x011								
2	0x021								
3	0x031								
4	0x201								
5	0x211								
6	0x221								
7	0x231								

* Read only bits

VCR	VCR signal indicator	
WKAIR	Weak signal indicator 2.	
WKAIR1	Weak signal indicator controlled by WKTH	
VSTD	1 =	Standard signal
	0 =	Non-standard signal
NINTL	1 =	Non-interlaced signal
	0 =	interlaced signal
VSHP	Vertical Sharpness Control	
	0 =	None (default)
	7 =	Highest
	**Note: VSHP must be set to '0' if COMB = 0	

#	Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	0x006	0	0	VACTIVE_XY[8]	VDELAY_XY[8]	HACITIVE_XY[9:8]		HDELAY_XY[9:8]	
1	0x016								
2	0x026								
3	0x036								
4	0x206								
5	0x216								
6	0x226								
7	0x236								
0	0x002	HDELAY_XY[7:0]							
1	0x012								
2	0x022								
3	0x032								
4	0x202								
5	0x212								
6	0x222								
7	0x232								

HDELAY_XY This 10 bit register defines the starting location of horizontal active pixel for display / record path. A unit is 1 pixel. The default value is 0x00F for NTSC and 0x00A for PAL.

#	Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	0x006	0	0	VACTIVE_XY[8]	VDELAY_XY[8]	HACITIVE_XY[9:8]		HDELAY_XY[9:8]	
1	0x016								
2	0x026								
3	0x036								
4	0x206								
5	0x216								
6	0x226								
7	0x236								
0	0x003	HACTIVE_XY[7:0]							
1	0x013								
2	0x023								
3	0x033								
4	0x203								
5	0x213								
6	0x223								
7	0x233								

HACTIVE_XY This 10bit register defines the number of horizontal active pixel for display / record path. A unit is 1 pixel. The default value is decimal 720.

#	Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	0x006	0	0	VACTIVE_XY[8]	VDELAY_XY[8]	HACITIVE_XY[9:8]		HDELAY_XY[9:8]	
1	0x016								
2	0x026								
3	0x036								
4	0x206								
5	0x216								
6	0x226								
7	0x236								
0	0x004	VDELAY_XY[7:0]							
1	0x014								
2	0x024								
3	0x034								
4	0x204								
5	0x214								
6	0x224								
7	0x234								

VDELAY_XY — This 9 bit register defines the starting location of vertical active for display / record path. A unit is 1 line. The default value is decimal 6.

#	Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	0x006	0	0	VACTIVE_XY[8]	VDELAY_XY[8]	HACITIVE_XY[9:8]		HDELAY_XY[9:8]	
1	0x016								
2	0x026								
3	0x036								
4	0x206								
5	0x216								
6	0x226								
7	0x236								
0	0x005	VACTIVE_XY[7:0]							
1	0x015								
2	0x025								
3	0x035								
4	0x205								
5	0x215								
6	0x225								
7	0x235								

VACTIVE_XY — This 9bit register defines the number of vertical active lines for display / record path. A unit is 1 line. The default value is decimal 240.

#	Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	0x007	HUE							
1	0x017								
2	0x027								
3	0x037								
4	0x207								
5	0x217								
6	0x227								
7	0x237								

HUE — These bits control the color hue as 2's complement number. They have value from +36° (7Fh) to -36° (80h) with an increment of 2.8°. The 2 LSB has no effect. The positive value gives greenish tone and negative value gives purplish tone. The default value is 0° (00h). This is effective only on NTSC system. The default is 00h.

#	Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	0x008	SCURVE	VSF	CTI		SHARPNESS			
1	0x018								
2	0x028								
3	0x038								
4	0x208								
5	0x218								
6	0x228								
7	0x238								

SCURVE — This bit controls the center frequency of the peaking filter. The corresponding gain adjustment is HFLT.

0 Low

1 center

VSF — This bit is for internal used. The default is 0.

CTI — CTI level selection. The default is 1.

0 None

3 Highest

SHARPNESS — These bits control the amount of sharpness enhancement on the luminance signals. There are 16 levels of control with '0' having no effect on the output image. 1 through 15 provides sharpness enhancement with 'F' being the strongest. The default is 1.

#	Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	0x009	CONTRAST							
1	0x019								
2	0x029								
3	0x039								
4	0x209								
5	0x219								
6	0x229								
7	0x239								

CONTRAST These bits control the luminance contrast gain. A value of 100 (64h) has a gain of 1. The range adjustment is from 0% to 255% at 1% per step. The default is 64h.

VIN	Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	0x00A	BRIGHTNESS							
1	0x01A								
2	0x02A								
3	0x03A								
4	0x20A								
5	0x21A								
6	0x22A								
7	0x23A								

BRIGHTNESS These bits control the brightness. They have value of –128 to 127 in 2's complement form. Positive value increases brightness. A value 0 has no effect on the data. The default is 00h.

#	Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	0x00B	SAT_U							
1	0x01B								
2	0x02B								
3	0x03B								
4	0x20B								
5	0x21B								
6	0x22B								
7	0x23B								

SAT_U These bits control the digital gain adjustment to the U (or Cb) component of the digital video signal. The color saturation can be adjusted by adjusting the U and V color gain components by the same amount in the normal situation. The U and V can also be adjusted independently to provide greater flexibility. The range of adjustment is 0 to 200%. A value of 128 (80h) has gain of 100%. The default is 80h.

#	Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	0x00C	SAT_V							
1	0x01C								
2	0x02C								
3	0x03C								
4	0x20C								
5	0x21C								
6	0x22C								
7	0x23C								

SAT_V These bits control the digital gain adjustment to the V (or Cr) component of the digital video signal. The color saturation can be adjusted by adjusting the U and V color gain components by the same amount in the normal situation. The U and V can also be adjusted independently to provide greater flexibility. The range of adjustment is 0 to 200%. A value of 128 (80h) has gain of 100%. The default is 80h.

#	Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	0x00D	SF*	PF*	FF*	KF*	CSBAD*	MCVSN*	CSTRIPE*	CTYPE2*
1	0x01D								
2	0x02D								
3	0x03D								
4	0x20D								
5	0x21D								
6	0x22D								
7	0x23D								

* Read only bits

SF This bit is for internal use

PF This bit is for internal use

FF This bit is for internal use

KF This bit is for internal use

CSBAD 1 Macrovision color stripe detection may be un-reliable

MCVSN 1 Macrovision AGC pulse detected.
0 Not detected.

CSTRIPE 1 Macrovision color stripe protection burst detected.
0 Not detected.

CTYPE2 This bit is valid only when color stripe protection is detected, i.e. if CSTRIPE=1,
1 Type 2 color stripe protection
0 Type 3 color stripe protection

#	Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	0x00E	DETSTUS*	STDNOW*			ATREG	STANDARD		
1	0x01E								
2	0x02E								
3	0x03E								
4	0x20E								
5	0x21E								
6	0x22E								
7	0x23E								

* Read only bits

DETSTUS	0	Idle
	1	Detection in progress
STDNOW	Current standard invoked	
	0	NTSC (M)
	1	PAL (B, D, G, H, I)
	2	SECAM
	3	NTSC4.43
	4	PAL (M)
	5	PAL (CN)
	6	PAL 60
	7	Not valid
ATREG	1	Disable the shadow registers
	0	Enable VACTIVE and HDELAY shadow registers value depending on STANDARD. (Default)
STANDARD	Standard selection	
	0	NTSC (M)
	1	PAL (B, D, G, H, I)
	2	SECAM
	3	NTSC4.43
	4	PAL (M)
	5	PAL (CN)
	6	PAL 60
	7	Auto detection (Default)

#	Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	0x00F	ATSTART	PAL60EN	PALCNEN	PALMEN	NTSC44EN	SECAMEN	PALBEN	NTSCEN
1	0x01F								
2	0x02F								
3	0x03F								
4	0x20F								
5	0x21F								
6	0x22F								
7	0x23F								

ATSTART	1	Writing 1 to this bit will manually initiate the auto format detection process. This bit is a self-clearing bit
	0	Manual initiation of auto format detection is done. (Default)
PAL60EN	1	Enable recognition of PAL60 (Default)
	0	Disable recognition
PALCNEN	1	Enable recognition of PAL (CN). (Default)
	0	Disable recognition
PALMEN	1	Enable recognition of PAL (M). (Default)
	0	Disable recognition
NTSC44EN	1	Enable recognition of NTSC 4.43. (Default)
	0	Disable recognition
SECAMEN	1	Enable recognition of SECAM. (Default)
	0	Disable recognition
PALBEN	1	Enable recognition of PAL (B, D, G, H, I). (Default)
	0	Disable recognition
NTSCEN	1	Enable recognition of NTSC (M). (Default)
	0	Disable recognition

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x045 0x245	0	0	VSMODE	FLDPOL	HSPOL	VSPOL	0	0

VSMODE — Control the VS and field flag timing

- 0 — VS and field flag is aligned with vertical sync of incoming video (Default)
- 1 — VS and field flag is aligned with HS

FLDPOL — Select the FLD polarity

- 0 — Odd field is high
- 1 — Even field is high (Default)

HSPOL — Select the HS polarity

- 0 — Low for sync duration (Default)
- 1 — High for sync duration

VSPOL — Select the VS polarity

- 0 — Low for sync duration (Default)
- 1 — High for sync duration

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x046	AGCEN4	AGCEN3	AGCEN2	AGCEN1	AGCGAIN4[8]	AGCGAIN3[8]	AGCGAIN2[8]	AGCGAIN1[8]
0x246	AGCEN8	AGCEN7	AGCEN6	AGCEN5	AGCGAIN8[8]	AGCGAIN7[8]	AGCGAIN6[8]	AGCGAIN5[8]
0x047	AGCGAIN1[7:0]							
0x048	AGCGAIN2[7:0]							
0x049	AGCGAIN3[7:0]							
0x04A	AGCGAIN4[7:0]							
0x247	AGCGAIN5[7:0]							
0x248	AGCGAIN6[7:0]							
0x249	AGCGAIN7[7:0]							
0x24A	AGCGAIN8[7:0]							

AGCENn — Select Video AGC loop function on VIN of channel n

- 0 — AGC loop function enabled (recommended for most application cases) (default).
- 1 — AGC loop function disabled. Gain is set by AGCGAINn

AGCGAINn — These registers control the AGC gain of channel n when AGC loop is disabled. Default value is 0F0h.

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x04B 0x24B	PD_BIAS	V_ADC_SAVE			0	0	0	YFLEN

PD_BIAS
1 Power down the alias of all 4 VADC
0 Do not power down the bias

V_ADC_SAVE
Power Saving Mode Selection.
0 Most Power Consuming
7 Most Power Saving

YFLEN
Analog Video CH1/CH2/CH3/CH4 anti-alias filter control
1 Enable(default)
0 Disable

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x04D 0x04E 0x24D 0x24E	0	0	0	0	0	0	0	0

Reserved

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x04F 0x24F	FRM		YNR		CLMD		PSP	

FRM
Free run mode control
0 Auto(default)
2 Default to 60Hz
3 Default to 50Hz

YNR
Y HF noise reduction
0 None(default)
1 Smallest
2 Small
3 Medium

CLMD
Clamping mode control
0 Sync top
1 Auto(default)
2 Pedestal
3 N/A

PSP
Slice level control
0 Low
1 Medium(default)
2 High

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x050	HFLT2				HFLT1			
0x051	HFLT4				HFLT3			
0x250	HFLT6				HFLT5			
0x251	HFLT8				HFLT7			

HFLTn HFLTn controls the peaking function of channel n. Reserved for test purpose.

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x052 0x252	CTEST	YCLEN	0	AFLTEN	GTEST	VLPF	CKLY	CKLC

CTEST Clamping control for debugging use. (Test purpose only)
(Default 0)

YCLEN
1 Y channel clamp disabled (Test purpose only)
0 Enabled (default)

AFLTEN
1 Analog Audio input Anti-Aliasing Filter enabled (default)
0 Disabled

GTEST
1 Test (Test purpose only)
0 Normal operation (default)

VLPF Clamping filter control (default 0)

CKLY Clamping current control 1 (default 0)

CKLC Clamping current control 2 (default 0)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x053	NT502	NT501						
0x054	NT504	NT503	DIV_RST	DOUT_RST	ACALEN	AADC_SAVE		
0x253	NT506	NT505						
0x254	NT508	NT507	DIV_RST	DOUT_RST	ACALEN	AADC_SAVE		

NT50n — 1: Force the Video Decoder n to a special NTSC 50 Hz format
0: Do not force to NTSC 50 Hz format

DIV_RST — Audio ADC divider reset. This bit must be set to 0 again after reset.

DOUT_RST — Audio ADC digital output reset for all channel. This bit must be setup up to 0 again after reset.

ACALEN — Audio ADC Calibration control. This be must be set up to 0 again after enabled.

AADC_SAVE — Audio ADC Power Saving Mode. 7 is most power saving.

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x055 0x255	FLD*				VAV*			

FLD — Status of the field flag for corresponding channel (*Read only)*
FLD [3:0] are FIELD ID for VIN3 to VIN0.
0: Odd field when FLDPOL (0x045) = 1
1: Even field when FLDPOL (0x045) = 1

VAV — Status of the vertical active video signal for corresponding channel (*Read only).* VAV [3:0] is Vertical Active Video Signals for VIN3 to VIN0.
0: Vertical blanking time
1: Vertical active time

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x057 0x257	SHCOR				0	0	0	0

SHCOR — These bits provide coring function for the sharpness control (default 3h)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x058 0x258	PBW	DEM	PALSW	SET7	COMB	HCOMP	YCOMB	PDLY

PBW	1	Wide Chroma BPF BW (Default)
	0	Normal Chroma BPF BW
DEM	Reserved (Default 1)	
PALSW	1	PAL switch sensitivity low.
	0	PAL switch sensitivity normal (Default)
SET7	1	The black level is 7.5 IRE above the blank level.
	0	The black level is the same as the blank level (Default)
COMB	1	Adaptive comb filter for NTSC and PAL (Recommended). This setting is not for SECAM (Default)
	0	Notch filter. For SECAM, always set to 0.
HCOMP	1	Operation mode 1 (Recommended) (Default)
	0	Mode 0
YCOMB	1	Bypass Comb filter when no burst presence
	0	No bypass (Default)
PDLY	0	Enable PAL delay line (default)
	1	Disable PAL delay line

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x059 0x259	GMEN	CKHY		HSDLY				

GMEN	Reserved (Default 0)	
CKHY	Color killer hysteresis.	
	0	Fastest (Default)
	1	Fast
	2	Medium
	3	Slow
HSDLY	Reserved for test	

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x05A 0x25A	CTCOR		CCOR		VCOR		CIF	

CTCOR These bits control the coring for CTI (Default 1h)

CCOR These bits control the low level coring function for the Cb/Cr output (Default 0h)

VCOR These bits control the coring function of vertical peaking
(Default 1h)

CIF These bits control the IF compensation level.

0 None (default)
1 1.5dB
2 3dB
3 6dB

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x05B 0x25B	CLPEND				CLPST			

CLPEND These 4 bits set the end time of the clamping pulse. Its value should be larger than the value of CLPST (Default 5h)

CLPST These 4 bits set the start time of the clamping. It is referenced to PCLAMP position. (Default 0h)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x05C 0x25C	NMGAIN				WPGAIN			FC27

NMGAIN These bits control the normal AGC loop maximum correction value (Default 4h)

WPGAIN Peak AGC loop gain control (Default 1h)

FC27

1 Normal ITU-R656 operation (Default)
0 Squared Pixel mode for test purpose only

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x05D 0x25D	PEAKWT							

PEAKWT These bits control the white peak detection threshold. Setting ‘FF’ can disable this function (Default D8h)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x05E 0x25E	CLMPLD	CLMPL						

CLMPLD
0 Clamping level is set by CLMPL
1 Clamping level preset at 60d (Default)

CLMPL These bits determine the clamping level of the Y channel (Default 3Ch)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x05F 0x25F	SYNCTD	SYNCT						

SYNCTD
0 Reference sync amplitude is set by SYNCT
1 Reference sync amplitude is preset to 38h (Default)

SYNCT These bits determine the standard sync pulse amplitude for AGC reference (Default 38h)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x062 0x262	M_RLSWAP	RM_SYNC	RM_PBSEL		R_ADATM		R_MULTCH	

M_RLSWAP

Define the sequence of mixing and playback audio data on the ADATM pin

If RM_SYNC=0: I2S format

0 Mixing audio on position 0 and playback audio on position 8 (Default)

1 Playback audio on position 0 and mixing audio on position 8

If RM_SYNC=1: DSP format

0 Mixing audio on position 0 and playback audio on position 1 (Default)

1 Playback audio on position 0 and mixing audio on position 1

RM_SYNC

Define the digital serial audio data format for record and mixing audio on the ACLKR, ASYNR, ADATR and ADATM pin

0 I2S format (Default)

1 DSP format

RM_PBSEL

Select the output PlayBackIn data for the ADATM pin

0 First Stage PalyBackIn audio (Default)

1 Second Stage PalyBackIn audio

2 Third Stage PalyBackIn audio

3 Last Stage PalyBackIn audio

R_ADATM

Select the output mode for the ADATM pin

0 Digital serial data of mixing audio (Default)

1 Digital serial data of ADATR format record audio

2 Digital serial data of ADATM format record audio

R_MULTCH

Define the number of audio for record on the ADATR pin

0 2 audios (Default)

1 4 audios

2 8 audios

3 16 audios

Number of output data is limited as shown on Sequence of Multi-channel Audio Record table. Also, each output position data are selected by R_SEQ_0/R_SEQ_1/.../R_SEQ_F registers.

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x063 0x263	AAUTO_MUTE	PBREFEN	VRSTSEL		FIRSTCNUM			

AAUTO_MUTE	1	When input Analog data is less than ADET_THn level, output PCM data will be set to 0. Audio DAC data input is 0x200.
	0	No effect

PBREFEN

Audio ACKG Reference (refin) input select

0	ACKG has video VRST refin input selected by VRSTSEL register (Default)
1	ACKG has audio ASYNP refin input

VRSTSEL

Select VRST (V reset) signal of VIN1 ~ VIN4 as ACKG (Audio Clock Generator) refin input.

0	VIN1 Video Decoder Path VRST (default)
1	VIN2 Video Decoder Path VRST
2	VIN3 Video Decoder Path VRST
3	VIN4 Video Decoder Path VRST

FIRSTCNUM

Set up First Stage number on audio cascade mode connection.

Set up the value of (Cascade chip number-1). In 4 chips cascade case, this value is 3h for ALINK mode. In single chip application case, this doesn't need to be set up.

0	(default)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x064 0x264	R_SEQ_1				R_SEQ_0			
0x065 0x265	R_SEQ_3				R_SEQ_2			
0x066 0x266	R_SEQ_5				R_SEQ_4			
0x067 0x267	R_SEQ_7				R_SEQ_6			
0x068 0x268	R_SEQ_9				R_SEQ_8			
0x069 0x269	R_SEQ_B				R_SEQ_A			
0x06A 0x26A	R_SEQ_D				R_SEQ_C			
0x06B 0x26B	R_SEQ_F				R_SEQ_E			

R_SEQ — Define the sequence of record audio on the ADATR pin.
Refer to Table 11 for the detail of the R_SEQ_0 ~ R_SEQ_F.
The default value of R_SEQ_0 is "0", R_SEQ_1 is "1", ... and R_SEQ_F is "F".

0	AIN1
1	AIN2
:	:
:	:
14	AIN15
15	AIN16

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x06C 0x26C	ADACEN	AADCEN	PB_ MASTER	PB_LRSEL	PB_SYNC	RM_8BIT	ASYNROEN	ACLKRMASTER

ADACEN — Audio DAC Function mode

- 0 Audio DAC function disable (test purpose only)
- 1 Audio DAC function enable (Default)

AADCEN — Audio ADC Function mode

- 0 Audio ADC function disable (test purpose only)
- 1 Audio ADC function enable (Default)

PB_MASTER — Define the operation mode of the ACLKP and ASYNP pin for playback.

- 0 All type I2S/DSP Slave mode (ACLKP and ASYNP is input) (Default)
- 1 TW5866 type I2S/DSP Master mode (ACLKP and ASYNP is output)

PB_LRSEL — Select the channel for playback.

- 0 Left channel audio is used for playback input (Default)
- 1 Right channel audio is used for playback input

PB_SYNC — Define the digital serial audio data format for playback audio on the ACLKP, ASYNP and ADATP pin.

- 0 I2S format (Default)
- 1 DSP format

RM_8BIT — Define output data format per one word unit on ADATR pin.

- 0 16bit one word unit output (Default)
- 1 8bit one word unit packed output

ASYNROEN — Define input/output mode on the ASYNR pin.

- 1 ASYNR pin is input
- 0 ASYNR pin is output (Default)

ACLKRMASTER — Define input/output mode on the ACLKR pin and set up audio 256xfs system processing

- 0 ACLKR pin is input. External 256xfs clock should be connected to ACLKR pin. This function is single chip Audio slave mode only.
- 1 ACLKR pin is output. Internal ACKG generates 256xfs clock (Default)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x06D	LAWMD		MIX_ DERATIO	MIX_MUTE0[4:0]				
0x26D	LAWMD		MIX_ DERATIO	MIX_MUTE1[4:0]				

LAWMD Select u-Law/A-Law/PCM/SB data output format on ADATR and ADATM pin.

0 PCM output (default)

1 SB (Signed MSB bit in PCM data is inverted) output

2 u-Law output

3 A-Law output

MIX_DERATIO Disable the mixing ratio value for all audio.

0 Apply individual mixing ratio value for each audio (Default)

1 Apply nominal value for all audio commonly

MIX_MUTE0 [n] Enable the mute function for audio channel AINn when n is 1 to 4. It effects only for mixing. When n = 4, it enable the mute function of the playback audio input. It effects only for single chip or the last stage chip

0 Normal

1 Muted (default)

MIX_MUTE1 [n] Enable the mute function for audio channel AIN5 ~ AIN8 when n is 0 to 3. It effects only for mixing. When n = 4, it enable the mute function of the playback audio input. It effects only for single chip or the last stage chip

0 Normal

1 Muted (default)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x06E	MIX_RATIO2				MIX_RATIO1			
0x06F	MIX_RATIO4				MIX_RATIO3			
0x26E	MIX_RATIO6				MIX_RATIO5			
0x26F	MIX_RATIO8				MIX_RATIO7			
0x070 0x270	0				MIX_RATIOP			

MIX_RATIOn Define the ratio values for audio mixing of channel AINn

MIX_RATIOP Define the ratio values for audio mixing of playback audio input

If MRATIO1MD / MRATIO2MD = 0 (default)

0	0.25
1	0.31
2	0.38
3	0.44
4	0.50
5	0.63
6	0.75
7	0.88
8	1.00 (default)
9	1.25
10	1.50
11	1.75
12	2.00
13	2.25
14	2.50
15	2.75

If MRATIO1MD / MRATIO2MD = 1, Mixing ratio is MIX_RATIOn / 64

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x071 0x271	V_ADC_CKPOL	A_ADC_CKPOL	A_DAC_CKPOL	MIX_OUTSEL				

V_ADC_CKPOL	Test purpose only (Default 0)
A_ADC_CKPOL	Test purpose only (Default 0)
A_DAC_CKPOL	Test purpose only (Default 0)
MIX_OUTSEL	In TW5866, there are two audio stages cascaded on-chip. The MIX_OUTSEL of 0x071 and 0x271 selects the audio output of each stage. The final audio fed to the audio DAC is further selected by the bypass register at 0xEC8 BYP_A2_AUD. If the BYP_A2_AUD is '1', the DAC will be driven by the first stage audio output. Otherwise it is driven by the second stage audio output.

0	Select record audio of channel 1
1	Select record audio of channel 2
2	Select record audio of channel 3
3	Select record audio of channel 4
4	Select record audio of channel 5
5	Select record audio of channel 6
6	Select record audio of channel 7
7	Select record audio of channel 8
8	Select record audio of channel 9
9	Select record audio of channel 10
10	Select record audio of channel 11
11	Select record audio of channel 12
12	Select record audio of channel 13
13	Select record audio of channel 14
14	Select record audio of channel 15
15	Select record audio of channel 16
16	Select playback audio of the first stage chip
17	Select playback audio of the second stage chip
18	Select playback audio of the third stage chip
19	Select playback audio of the last stage chip
20	Select mixed audio (default)
21	Select record audio of channel AIN51
22	Select record audio of channel AIN52
23	Select record audio of channel AIN53
24	Select record audio of channel AIN54

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x072	AAMPMD	ADET_FILT			ADET_TH4[4]	ADET_TH3[4]	ADET_TH2[4]	ADET_TH1[4]
0x272	AAMPMD	ADET_FILT			ADET_TH8[4]	ADET_TH7[4]	ADET_TH6[4]	ADET_TH5[4]
0x073	ADET_TH2[3:0]				ADET_TH1[3:0]			
0x074	ADET_TH4[3:0]				ADET_TH3[3:0]			
0x273	ADET_TH6[3:0]				ADET_TH5[3:0]			
0x274	ADET_TH8[3:0]				ADET_TH7[3:0]			

AAMPMD — Define the audio detection method.

0 Detect audio if absolute amplitude is greater than threshold

1 Detect audio if differential amplitude is greater than Threshold (default)

ADET_FILT — Select the filter for audio detection (default 4h)

0 Wide LPF

: :

7 Narrow LPF

ADET_THn — Define the threshold value for audio detection of AINn (Default Ah)

0 Low value

: :

31 High value

If fs = 8kHz Audio Clock setting mode, Registers

0x072 = 0xC0

0x073 = 0xAA

0x074 = 0xAA

are typical setting.

If fs=16kHz/32kHz/44.1kHz/48kHz Audio Clock setting mode, Registers

0x072 = 0xE0

0x073 = 0xBB

0x074 = 0xBB

are typical setting.

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x075 0x275	ACKI[7:0]							
0x076 0x276	ACKI[15:8]							
0x077 0x277	0	0	ACKI[21:16]					

ACKI — These bits control ACKI Clock Increment in ACKG block.

09B583h for fs = 8 kHz is default

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x078 0x278	ACKN[7:0]							
0x079 0x279	ACKN[15:8]							
0x07A 0x27A	0	0	0	0	0	0	ACKN[17:16]	

ACKN These bits control ACKN Clock Number in ACKG block.
000100h for Playback Slave-in lock is default.

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x07B 0x27B	0	0	SDIV					

SDIV These bits control SDIV Serial Clock Divider in ACKG block (Default 01h)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x07C 0x27C	0	0	LRDIV					

LRDIV These bits control LRDIV Left/Right Clock Divider in ACKG block (Default 20h)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x07D 0x27D	APZ	APG			0	ACPL	SRPH	LRPH

APZ These bits control Loop in ACKG block (Default 1)

APG These bits control Loop in ACKG block (Default 4h)

ACPL These bits control Loop closed/open in ACKG block
0 Loop closed
1 Loop open (recommended on typical application case) (Default)

SRPH Reserved. These bits are not used in TW5866 chip.

LRPH Reserved. These bits are not used in TW5866 chip.

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x0C0 0x2C0	BGNDEN				BGNDCOL	AUTO_BGND	LIM_656	0

BGNDEN[n] Enable the background color for channel n for byte-interleave video decoder output.

0 Background color is disabled (Default)

1 Background color is enabled

BGNDCOL Select the background color when BGNDEN = "1" or when AUTO_BGND = "1" and Video Loss is detected

0 Blue color (Default)

1 Black color

AUTO_BGND Select the decoder background mode.

0 Manual background mode (Default)

1 Automatic background mode when No-video is detected

LIM_656 Clamp the Y and C value in the video stream

0 Maximum of Y is 254, Minimum of Y is 1

Maximum of C is 254, Minimum of Y is 1

1 Maximum of Y is 235, Minimum of Y is 16

Maximum of Y is 240, Minimum of Y is 16

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x0C1 0x2C1	0	OUT_CHID	SAV_CHID	TST_EHAV_BLK	0	0	0	0

TST_EHAV_BLK Testing purpose only

1 Force the Y value to be 0 when HAV is high.

0 Normal Operation

OUT_CHID Enable the channel ID format in the horizontal blanking period

0 Disable the channel ID format (default)

1 Enable the channel ID format

The lowest 4 bits of Y and C pixel value during horizontal blanking is

Bit 3 Video Loss

Bit 2 Analog Mux A/B

Bit 1-0 Port ID

SAV_CHID Enable the channel ID format in the SAV / EAV header

0 Disable the channel ID format (default)

1 Enable the channel ID format

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x0D0	AADC4OFS[9:8]		AADC3OFS[9:8]		AADC2OFS[9:8]		AADC1OFS[9:8]	
0x0D5	0		0		0		AADC51OFS[9:8]	
0x2D0	AADC8OFS[9:8]		AADC7OFS[9:8]		AADC6OFS[9:8]		AADC5OFS[9:8]	
0x2D5	0		0		0		AADC52OFS[9:8]	
0x0D1	AADC1OFS[7:0]							
0x0D2	AADC2OFS[7:0]							
0x0D3	AADC3OFS[7:0]							
0X0D4	AADC4OFS[7:0]							
0x0D6	AADC51OFS[7:0]							
0x2D1	AADC5OFS[7:0]							
0x2D2	AADC6OFS[7:0]							
0x2D3	AADC7OFS[7:0]							
0X2D4	AADC8OFS[7:0]							
0x2D6	AADC52OFS[7:0]							

Digital ADC input data offset control for AIN1 ~ AIN10. Digital ADC input data is adjusted by

ADJAADCn = AUDADCn + AADCnOFS

Where AUDADCn is 2's formatted Analog Audio ADC output, and AADCnOFS is adjusted offset value by 2's format. All default 10bit data value is 3EFh.

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x0D7	0	ADCISEL0			AUDADC0_n[9:8]*		ADJAADC0_n[9:8]*	
0x0D8	AUDADC0_n[7:0]*							
0x0D9	ADJAADC0_n[7:0]*							
0x2D7	0	ADCISEL1			AUDADC1_n[9:8]*		ADJAADC1_n[9:8]*	
0x2D8	AUDADC1_n[7:0]*							
0x2D9	ADJAADC1_n[7:0]*							

AUDADC0_n
`

Current Analog Audio AIN1 ~ AIN4 ADC Digital Output Value by 2's format

These value show the first input data value in front of Digital Audio Decimation Filtering process.

ADJAADC0_n

Current adjusted Audio AIN1 ~ AIN4 ADC Digital input data value by 2's format. These value show the first input data value in front of Digital Audio Decimation Filtering process.

ADCISEL0

Select AUDADC0_n, ADJAADC0_n Audio input number. AUDADC0_n and ADJAADC0_n read value shows following selected Audio input data.

0 AIN1
1 AIN2
2 AIN3
3 AIN4

AUDADC1_n
`

Current Analog Audio AIN5 ~ AIN8 ADC Digital Output Value by 2's format

These value show the first input data value in front of Digital Audio Decimation Filtering process.

ADJAADC1_n

Current adjusted Audio AIN5 ~ AIN8 ADC Digital input data value by 2's format. These value show the first input data value in front of Digital Audio Decimation Filtering process.

ADCISEL1

Select AUDADC1_n, ADJAADC1_n Audio input number. AUDADC1_n and ADJAADC1_n read value shows following selected Audio input data.

0 AIN5
1 AIN6
2 AIN7
3 AIN8

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x0DA 0x2DA	0	0	0	I2SO_RSEL				
0x0DB 0x2DB	0	0	0	I2SO_LSEL				
0x0DC 0x2DC	I2SRECSEL54		I2SRECSEL53		I2SRECSEL52		I2SRECSEL51	
0x0DD	A51OUT_OFF	ADATM_ I2SOEN	MIX_MUTE _A51	ADET_TH51				
0x2DD	A52OUT_OFF	ADATM_ I2SOEN	MIX_MUTE _A52	ADET_TH52				

A51OUT_OFF — AIN51 data output control on ADATR record signal.

- 0 — Output AIN51/AIN52/AIN53/AIN54 record data on ADATR
- 1 — Not output AIN51/AIN52/AIN53/AIN54 record data on ADATR

A52OUT_OFF — AIN52 data output control on ADATR record signal.

- 0 — Output AIN51/AIN52/AIN53/AIN54 record data on ADATR
- 1 — Not output AIN51/AIN52/AIN53/AIN54 record data on ADATR

ADATM_I2SOEN — Define ADATM pin output 2 word data to make standard I2S output.

- 0 — Output Mixing or Playback data only on ADATM pin as specified by M_RLSWAP register (Default)
- 1 — L/R data on ADATM pin is selected by I2SO_RSEL/I2SO_LSEL registers

MIX_MUTE_A51 — Audio input AIN51 mute function control

- 0 — Normal
- 1 — Muted

MIX_MUTE_A52 — Audio input AIN52 mute function control

- 0 — Normal
- 1 — Muted

ADET_TH51 — AIN51 threshold value for audio detection

ADET_TH52 — AIN52 threshold value for audio detection

I2SO_RSEL/ I2SO_LSEL — Select L/R output data on ADATM pin when ADATM_I2SOEN=1.
Both I2SO_RSEL and I2SO_LSEL select output data by following order.

- 0 — Select record audio of channel 1(AIN0)
- 1 — Select record audio of channel 2(AIN1)
- 2 — Select record audio of channel 3(AIN2)
- 3 — Select record audio of channel 4(AIN3)

	4	Select record audio of channel 5(AIN4)
	5	Select record audio of channel 6(AIN5)
	6	Select record audio of channel 7(AIN6)
	7	Select record audio of channel 8(AIN7)
	8	Select record audio of channel 9(AIN8)
	9	Select record audio of channel 10(AIN9)
	10(Ah)	Select record audio of channel 11(AIN10)
	11(Bh)	Select record audio of channel 12(AIN11)
	12(Ch)	Select record audio of channel 13(AIN12)
	13(Dh)	Select record audio of channel 14(AIN13)
	14(Eh)	Select record audio of channel 15(AIN14)
	15(Fh)	Select record audio of channel 16(AIN15)
	16(10h)	Select playback audio of the first stage chip (PB1)
	17(11h)	Select playback audio of the second stage chip (PB2)
	18(12h)	Select playback audio of the third stage chip (PB3)
	19(13h)	Select playback audio of the last stage chip (PB4)
	20(14h)	Select mixed audio
	21(15h)	Select record audio of channel 51(AIN51) (default)
	22(16h)	Select record audio of channel 52(AIN52)
	23(17h)	Select record audio of channel 53(AIN53)
	24(18h)	Select record audio of channel 54(AIN54)
	Others	No audio output
I2SRECSEL5n	Select output data of port n in the position below	
	0	AIN51
	1	AIN52
	2	AIN53
	3	AIN54

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x0DE					MIX_RATIO51			
0x2DE					MIX_RATIO52			

MIX_RATIO51

Define the ratio values for audio mixing of channel AIN51 using MIX_RATIO51 to the ratio values for audio mixing of playback audio input

If MRATIO1MD = 0 (default)

0	0.25
1	0.31
2	0.38
3	0.44
4	0.50
5	0.63
6	0.75
7	0.88
8	1.00 (default)
9	1.25
10	1.50
11	1.75
12	2.00
13	2.25
14	2.50
15	2.75

If MRATIO1MD = 1, Mixing ratio is MIX_RATIO51 / 64

MIX_RATIO52

Define the ratio values for audio mixing of channel AIN52 using MIX_RATIO52 to the ratio values for audio mixing of playback audio input

If MRATIO2MD = 0 (default)

0	0.25
1	0.31
2	0.38
3	0.44
4	0.50
5	0.63
6	0.75
7	0.88
8	1.00 (default)
9	1.25
10	1.50
11	1.75
12	2.00
13	2.25
14	2.50
15	2.75

If MRATIO2MD = 1, Mixing ratio is MIX_RATIO52 / 64

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x0DF	0	0	ACLKR128	ACLKR64	AFS384	AIN51MD	0	0
0x2DF	0	0	ACLKR128	ACLKR64	AFS384	AIN52MD	0	0

ACLKR128

ACLKR clock output mode for special 16x8bit (total 128bit) data interface.

0 ACLKR output is normal (Default).

1 the number of ACLKR clock per fs is 128.This function is effective with RM_8BIT=1 8bit mode (special purpose).

ACLKR64

ACLKR clock output mode for special 4 word output interface. ACLKRMASTER=1 mode only.

0 ACLKR output is normal (Default)

1 the number of ACLKR clock per fs is 64.

AFS384

Special Audio fs sampling mode.

0 Audio fs Sampling mode is normal 256xfs if AIN5 = 0. (Default)

1 Audio fs Sampling mode is 384xfs mode. In this mode, AIMANU=1, A1NUM=0, A2NUM=1, A3NUM=2, A4NUM = 3, A5NUM=4 setting are needed.

AIN51MD

Audio Input process mode

0 AIN1/AIN2/AIN3/AIN4 4 audio input mode. This mode is 256xfs if AFS384 = 0. In this mode, AIN51 is not used.

1 AIN1/AIN2/AIN3/AIN4/AIN51 5 audio input mode. This mode is 320xfs mode if AFS384 = 0.

AIN52MD

Audio Input process mode

0 AIN5/AIN6/AIN7/AIN8 4 audio input mode. This mode is 256xfs if AFS384 = 0. In this mode, AIN52 is not used.

1 AIN5/AIN6/AIN7/AIN8/AIN52 5 audio input mode. This mode is 320xfs mode if AFS384 = 0.

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x0E0	MRATIO1MD	0	0	0	0	0	0	0
0x2E0	MRATIO2MD	0	0	0	0	0	0	0

MRATIO1MD

1 Use a more exponential way to interpret the MRATIO1. Perform the following transformation before using the ratio

0 ~ 3 => 4 ~ 7

4 ~ 7 => 8 ~ 14

8 ~ 11 => 16 ~ 28

12 ~ 15 => 32 ~ 44

0 Use the MRATIO1 as the ratio

MRATIO2MD

1 Use a more exponential way to interpret the MRATIO2. Perform the following transformation before using the ratio

0 ~ 3 => 4 ~ 7

4 ~ 7 => 8 ~ 14

8 ~ 11 => 16 ~ 28

12 ~ 15 => 32 ~ 44

0 Use the MRATIO2 as the ratio

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x0E3 0x2E3	0	0	ACLKRPOL	ACLKPPOL	AFAUTO	AFMD		

ACLKRPOL

ACLKR input signal polarity inverse.

0 Not inversed (Default)

1 Inversed

ACLKPPOL

ACLKP input signal polarity inverse.

0 Not inversed (Default)

1 Inversed

AFAUTO

ACKI [21:0] control automatic set up with AFMD registers

This mode is only effective when ACLKRMASTER=1

0 ACKI [21:0] registers set up ACKI control

1 ACKI control is automatically set up by AFMD register values

AFMD

AFAUTO control mode

0 8 kHz setting (Default)

1 16 kHz setting

2 32 kHz setting

3 44.1 kHz setting

4 48 kHz setting

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x0E4 0x2E4	I2S8MODE	MASCKMD	PBINSWAP	ASYNRDLY	ASYNPDLY	ADATPDLY	INLAWMD	

I2S8MODE — 8bit I2S Record output mode.

0 L/R half length separated output (Default).

1 One continuous packed output equal to DSP output format.

MASCKMD — Audio Clock Master ACLKR output wave format.

0 High period is one 27MHz clock period (default).

1 Almost duty 50-50% clock output on ACLKR pin. If this mode is selected, two times bigger number value need to be set up on the ACKI register. If AFAUTO=1, ACKI control is automatically set up even if MASCKMD=1.

PBINSWAP — Playback ACLKP/ASYNP/ADATP input data MSB-LSB swapping.

0 Not swapping

1 Swapping.

ASYNRDLY — ASYNR input signal delay.

0 No delay

1 Add one 27MHz period delay in ASYNR signal input

ASYNPDLY — ASYNP input signal delay.

0 no delay

1 add one 27MHz period delay in ASYNP signal input

ADATPDLY — ADATP input data delay by one ACLKP clock.

0 No delay (Default).This is for I2S type 1T delay input interface.

1 Add 1 ACLKP clock delay in ADATP input data. This is for left-justified type 0T delay input interface.

INLAWMD — Select u-Law/A-Law/PCM/SB data input format on ADATP pin.

0 PCM input (Default)

1 SB (Signed MSB bit in PCM data is inverted) input

2 u-Law input

3 A-Law input

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x0E5	0	0	0	0	0	0	0	A51DETENA
0x2E5	0	0	0	0	0	0	0	A52DETENA

A51DETENA — Enable state register updating and interrupt request of audio AIN51 detection for each input

0 Disable state register updating and interrupt request

1 Enable state register updating and interrupt request

A52DETENA — Enable state register updating and interrupt request of audio AIN52 detection for each input

0 Disable state register updating and interrupt request

1 Enable state register updating and interrupt request

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x0E9 0x2E9	CKLM	YDLY			0	0	0	0

CKLM — Color Killer mode.

0 Normal (Default)

1 Fast (For special application)

YDLY — Luma delay fine adjustment. This 2's complement number provides –4 to +3 unit delay control (Default 3h)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x0EA	0	0	ADECRST	0	VDEC4RST	VDEC3RST	VDEC2RST	VDEC1RST
0x2EA	0	0	ADECRST	0	VDEC8RST	VDEC7RST	VDEC6RST	VDEC5RST

ADECRST — A 1 written to this bit resets the audio portion to its default state but all register content remains unchanged. This bit is self-cleared.

VDECnRST — A 1 written to this bit resets the VINn path Video Decoder portion to its default state but all register content remain unchanged. This bit is self cleared.

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x0EB 0x2EB	MISSCNT				HSWIN			

MISSCNT — These bits set the threshold for horizontal sync miss count threshold (Default 4h)

HSWIN — These bits determine the VCR mode detection threshold (Default 4h)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x0EC 0x2EC	PCLAMP							

PCLAMP — These bits set the clamping position from the PLL sync edge (Default 2Ah)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x0ED 0x2ED	VLCKI		VLCKO		VMODE	DETV	AFLD	VINT

VLCKI — Vertical lock in time
- 0 Fastest (Default)
- :
- 3 Slowest.

VLCKO — Vertical lock out time
- 0 Fastest (Default)
- :
- 3 Slowest

VMODE — This bit controls the vertical detection window
- 1 Search mode
- 0 Vertical countdown mode (Default)

DETV
- 1 Recommended for special application only
- 0 Normal Vsync logic (Default)

AFLD — Auto field generation control
- 0 Off (Default)
- 1 On

VINT — Vertical integration time control
- 1 Short
- 0 Normal (Default)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x0EE 0x2EE	BSHT			VSHT				

BSHT — Burst PLL center frequency control (Default 0h)

VSHT — Vsync output delay control in the increment of half line length (Default 0h)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x0EF 0x2EF	CKILLMAX		CKILLMIN					

CKILLMAX These bits control the amount of color killer hysteresis. The hysteresis amount is proportional to the value (Default 1h)

CKILLMIN These bits control the color killer threshold. Larger value gives lower killer level (Default 28h)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x0F0 0x2F0	COMBMD	HTL			VTL			

COMBMD
- 0 Adaptive mode (Default)
- 1 Fixed comb

HTL Adaptive Comb filter threshold control 1 (Default 4h)

VTL Adaptive Comb filter threshold control 2 (Default Ch)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x0F1 0x2F1	HPLC	EVCNT	PALC	SDET	0	BYPASS	0	0

HPLC Reserved for internal use (Default 0)

EVCNT
- 1 Even field counter in special mode
- 0 Normal operation (Default)

PALC Reserved for future use (Default 0)

SDET ID detection sensitivity. A '1' is recommended (Default 1)

BYPASS It controls the standard detection and should be set to ‘1’ in normal use (Default 1)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x0F2 0x2F2	HPM		ACCT		SPM		CBW	

HPM Horizontal PLL acquisition time.

3	Fast
2	Auto1 (Default)
1	Auto2
0	Normal

ACCT ACC time constant

0	No ACC
1	Slow
2	Medium (Default)
3	Fast

SPM Burst PLL control

0	Slowest
1	Slow (Default)
2	Fast
3	Fastest

CBW Chroma low pass filter bandwidth control. Refer to filter curves (Default 1)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x0F3 0x2F3	NKILL	PKILL	SKILL	CBAL	FCS	LCS	CCS	BST

NKILL	1	Enable noisy signal color killer function in NTSC mode (Default)
	0	Disabled
PKILL	1	Enable automatic noisy color killer function in PAL mode (Default)
	0	Disabled
SKILL	1	Enable automatic noisy color killer function in SECAM Mode (Default)
	0	Disabled
CBAL	0	Normal output (Default)
	1	Special output mode.
FCS	1	Force decoder output value determined by CCS
	0	Disabled (Default)
LCS	1	Enable pre-determined output value indicated by CCS when video loss is detected
	0	Disabled (Default)
CCS	When FCS is set high or video loss condition is detected when LCS is set high, one of two colors display can be selected.	
	1	Blue color
	0	Black (Default)
BST	1	Enable blue stretch
	0	Disabled (Default)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x0F4	0	0	MONITOR1					
0x0F5	HREF1*							
0x2F4	0	0	MONITOR2					
0x2F5	HREF2*							

These registers are for test purpose only. The MONITOR is used to select the HREF status of a certain video decoder port into Reg0x0F5 and 0x2F5 register.

MONITOR1 Value	Select video decoder HREF to show in HREF1 in 0x0F5	
	00h	HREF1 shows VIN1 Video Decoder Path HREF [9:2]
	10h	HREF1 shows VIN2 Video Decoder Path HREF [9:2]
	20h	HREF1 shows VIN3 Video Decoder Path HREF [9:2]
	30h	HREF1 shows VIN4 Video Decoder Path HREF [9:2]
MONITOR2 Value	Select video decoder port for HREF2 in 0x2F5	
	00h	HREF2 shows VIN5 Video Decoder Path HREF [9:2]
	10h	HREF2 shows VIN6 Video Decoder Path HREF [9:2]
	20h	HREF2 shows VIN7 Video Decoder Path HREF [9:2]
	30h	HREF2 shows VIN8 Video Decoder Path HREF [9:2]

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x0F6	0	CVSTD1*			CVFMT1			
0x0F7	0	CVSTD2*			CVFMT2			
0x0F8	0	CVSTD3*			CVFMT3			
0x0F9	0	CVSTD4*			CVFMT4			
0x2F6	0	CVSTD5*			CVFMT5			
0x2F7	0	CVSTD6*			CVFMT6			
0x2F8	0	CVSTD7*			CVFMT7			
0x2F9	0	CVSTD8*			CVFMT8			

CVSTDn

CVFMTn

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x0FA	IDX1		NSEN1/SSEN1/PSEN1/WKTH1					
0x0FB	IDX2		NSEN2/SSEN2/PSEN2/WKTH2					
0x0FC	IDX3		NSEN3/SSEN3/PSEN3/WKTH3					
0x0FD	IDX4		NSEN4/SSEN4/PSEN4/WKTH4					
0x2FA	IDX5		NSEN5/SSEN5/PSEN5/WKTH5					
0x2FB	IDX6		NSEN6/SSEN6/PSEN6/WKTH6					
0x2FC	IDX7		NSEN7/SSEN7/PSEN7/WKTH7					
0x2FD	IDX8		NSEN8/SSEN8/PSEN8/WKTH8					

NSENn/SSENn/PSENn/WKTHn shared the same 6 bits in the register. IDXn is used to select which of the four parameters is being controlled. The write sequence is a two steps process unless the same register is written. A write of {ID, 000000} selects one of the four registers to be written. A subsequent write will actually write into the register. (Default 0h)

IDXn
- 0 Controls the NTSC color carrier detection sensitivity (NSENn) (Default 1Ah)
- 1 Controls the SECAM ID detection sensitivity (SSENn) (Default 20h)
- 2 Controls the PAL ID detection sensitivity (PSENn) (Default 1Ch)
- 3 Controls the weak signal detection sensitivity (WKTHn) (Default 2Ah)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x110	PALNT1				FLD_POL1	0	0	EN_NR1
0x111	PALNT2				FLD_POL2	0	0	EN_NR2
0x112	PALNT3				FLD_POL3	0	0	EN_NR3
0x113	PALNT4				FLD_POL4	0	0	EN_NR4
0x310	PALNT5				FLD_POL5	0	0	EN_NR5
0x311	PALNT6				FLD_POL6	0	0	EN_NR6
0x312	PALNT7				FLD_POL7	0	0	EN_NR7
0x313	PALNT8				FLD_POL8	0	0	EN_NR8

EN_NRn Enable Noise Reduction of Channel n

1 Enable Noise Reduction

0 Disable Noise Reduction

PALNTn Set PAL/NTSC for Channel n.

1 Set to PAL

0 Set to NTSC

FLD_POLn Set field polarity

1 Reverse field polarity

0 Do not reverse field polarity

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x114 0x115 0x116 0x117 0x118 0x119 0x11E 0x314 0x315 0x316 0x317 0x318 0x319 0x31E	0	0	0	0	0	0	0	0

Reserved registers. Set to 0 all the time.

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x120 0x320	0xAA							
0x121 0x321	0x3C							
0x122 0x322	0x32							
0x123 0x323	0x14							
0x124 0x324	0x28							
0x125 0x325	0xA5							
0x126 0x326	0x14							
0x127 0x327	0x14							
0x128 0x328	0x0F							
0x129 0x329	0xAA							
0x12A 0x32A	0xA5							
0x12B 0x32B	0x28							
0x12C 0x32C	0xAA							
0x12D 0x32D	0x14							
0x12E 0x32E	0x0F							
0x130 0x330	0x05							
0x131 0x331	0x0A							
0x132 0x332	0x08							
0x133 0x333	0x0F							
0x134 0x334	0x19							
0x135 0x335	0x25							
0x136 0x336	0x19							
0x137 0x337	0xF0							

Reserved registers. Do not overwrite these registers.

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x178 0x378			SAV_DETVID	2BIT_CHID	BLUE_BGND	LIM_656	BLANK_CHID	SAV_CHID

SAV_CHID Enable CHID in the SAV/EAV for byte-interleaving preview output

BLANK_CHID Enable CHID in the horizontal blanking area for byte-interleaving preview output

LIM_656 Limit pixel data to between 16 and 235 at the preview output port.

BLUE_BGND
- 1 Show blue background color when no video is detected and the auto background color control AUTO_BGND is enabled or when the BGND_ENn is enabled.
- 0 Show black background color when no video is detected and the auto background color control AUTO_BGND is enabled or when the BGND_ENn is enabled.

2BIT_CHID
- 1 Use only 2 bit for channel ID in the SAV/EAV
- 0 Use 4 bit for channel ID in the SAV/EAV, with upper two bit set to 0.

SAV_DETVID
- 1 Show the detect video flag at bit 7 of SAV/EAV
- 0 Do not show the detect video flag at bit 7 of SAV/EAV

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x179					BGND_EN4	BGND_EN3	BGND_EN2	BGND_EN1
0x379					BGND_EN8	BGND_EN7	BGND_EN6	BGND_EN5

BGND_ENn
- 1 Force to show blue or black background color on channel n
- 0 Do not force to show background color on channel n

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x17A				AUTO_BGND				
0x37A				AUTO_BGND				

AUTO_BGND
- 1 Show a channel as background color when no video signal is detected on the channel input
- 0 Do not show background color even when no video signal is detected

0x1D400 ~ 0x1D7FF: SD Scalers/Interrupts

Note: The front-end registers below are represented with offset address. The actual address is derived with 0x1C000 + 4 * offset

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x500	IN_PIC_WIDTH							
0x501		IN_PIC_HEIGHT						
0x502	OUT_PIC_WIDTH							
0x503		OUT_PIC_HEIGHT						

IN_PIC_WIDTH — Input picture width setting for scalers in 4 pixels unit. (Default 720 / 4)

IN_PIC_HEIGHT — Input picture height setting for scalers in 4 lines unit. (Default 240 / 4)

OUT_PIC_WIDTH — Output picture width setting for scalers in 4 pixels unit. This value is used to decide the width of CIF. The QCIF width will be derived from this setting. (Default 360 / 4)

OUT_PIC_HEIGHT — Output picture height setting for scalers in 4 lines unit. This value is used to decide the height of CIF. The QCIF height will be derived from this setting. (Default 120 / 4)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x560							SMALL_FR	PAL

PAL — NTSC/PAL control for mode detection

- 0 NTSC
- 1 PAL

SMALL_FR — Small frame size setting for simulation

- 0 Normal frame size
- 1 Small frame size

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x5D0	INTERRUPT[7:0]							
0x5D1	INTERRUPT[15:8]							
0x5D2	INTERRUPT[23:16]							
0x5D3	INTERRUPT[31:24]							
0x5D4	INTERRUPT[39:32]							
0x5D5	INTERRUPT[47:40]							
0x5D6	INTERRUPT[55:48]							
0x5D7	INTERRUPT[63:56]							

INTERRUPT — Interrupt status register from the front-end. Write "1" to each bit to clear the interrupt

15:0 Motion detection interrupt for channel 0 ~ 15
31:16 Night detection interrupt for channel 0 ~ 15
47:32 Blind detection interrupt for channel 0 ~ 15
63:48 No video interrupt for channel 0 ~ 15

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x5D8	INTERRUPT_MASK[7:0]							
0x5D9	INTERRUPT[_MASK 15:8]							
0x5DA	INTERRUPT_MASK [23:16]							
0x5DB	INTERRUPT_MASK [31:24]							
0x5DC	INTERRUPT_MASK [39:32]							
0x5DD	INTERRUPT_MASK [47:40]							
0x5DE	INTERRUPT_MASK [55:48]							
0x5DF	INTERRUPT_MASK [63:56]							

INTERRUPT_MASK — Interrupt mask register for interrupts in 0x5D0 ~ 0x5D7

15:0 Motion detection interrupt for channel 0 ~ 15
31:16 Night detection interrupt for channel 0 ~ 15
47:32 Blind detection interrupt for channel 0 ~ 15
63:48 No video interrupt for channel 0 ~ 15

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x5F0	INTERRUPT_SUMMARY[7:0]							

INTERRUPT_SUMMARY — Interrupt summary register for interrupts & interrupt mask from in 0x5D0 ~ 0x5D7 and 0x5D8 ~ 0x5DF

bit 0 : interrupt occurs in 0x5D0 & 0x5D8
bit 1 : interrupt occurs in 0x5D1 & 0x5D9
bit 2 : interrupt occurs in 0x5D2 & 0x5DA
bit 3 : interrupt occurs in 0x5D3 & 0x5DB
bit 4 : interrupt occurs in 0x5D4 & 0x5DC
bit 5 : interrupt occurs in 0x5D5 & 0x5DD
bit 6 : interrupt occurs in 0x5D6 & 0x5DE
bit 7 : interrupt occurs in 0x5D7 & 0x5DF

0x1D800 ~ 0x1DBFF: SD MD/BD/ND

Note: The front-end registers below are represented with offset address. The actual address is derived with 0x1C000 + 4 * offset

<table>
<tr><th>#</th><th>Address</th><th>[7]</th><th>[6]</th><th>[5]</th><th>[4]</th><th>[3]</th><th>[2]</th><th>[1]</th><th>[0]</th></tr>
<tr><td>0</td><td>0x600</td><td rowspan="16"></td><td rowspan="16"></td><td rowspan="16">MD_DIS</td><td rowspan="16"></td><td rowspan="16">MD_STRB</td><td rowspan="16">MD_STRB_E N</td><td rowspan="16" colspan="2">BD_CELLSENS</td></tr>
<tr><td>1</td><td>0x608</td></tr>
<tr><td>2</td><td>0x610</td></tr>
<tr><td>3</td><td>0x618</td></tr>
<tr><td>4</td><td>0x620</td></tr>
<tr><td>5</td><td>0x628</td></tr>
<tr><td>6</td><td>0x630</td></tr>
<tr><td>7</td><td>0x638</td></tr>
<tr><td>8</td><td>0x640</td></tr>
<tr><td>9</td><td>0x648</td></tr>
<tr><td>10</td><td>0x650</td></tr>
<tr><td>11</td><td>0x658</td></tr>
<tr><td>12</td><td>0x660</td></tr>
<tr><td>13</td><td>0x668</td></tr>
<tr><td>14</td><td>0x670</td></tr>
<tr><td>15</td><td>0x678</td></tr>
</table>

MD_DIS — Disable the motion and blind detection.
- 0 Enable motion and blind detection (default)
- 1 Disable motion and blind detection

MD_STRB — Request to start motion detection on manual trigger mode
- 0 None Operation (default)
- 1 Request to start motion detection

MD_STRB_EN — Select the trigger mode of motion detection
- 0 Automatic trigger mode of motion detection (default)
- 1 Manual trigger mode for motion detection

BD_CELSENS — Define the threshold of cell for blind detection.
- 0 Low threshold (More sensitive) (default)
- : :
- 3 High threshold (Less sensitive)

#	Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	0x601	MD_TMPSENS				MD_PIXEL_OS			
1	0x609								
2	0x611								
3	0x619								
4	0x621								
5	0x629								
6	0x631								
7	0x639								
8	0x641								
9	0x649								
10	0x651								
11	0x659								
12	0x661								
13	0x669								
14	0x671								
15	0x679								

MD_TMPSENS Control the temporal sensitivity of motion detector.

0 More Sensitive (default)

: :

15 Less Sensitive

MD_PIXEL_OS Adjust the horizontal starting position for motion detection

0 0 pixel (default)

: :

15 15 pixels

#	Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	0x602	MD_REFFLD	MD_FIELD		MD_LVSENS				
1	0x60A								
2	0x612								
3	0x61A								
4	0x622								
5	0x62A								
6	0x632								
7	0x63A								
8	0x642								
9	0x64A								
10	0x652								
11	0x65A								
12	0x662								
13	0x66A								
14	0x672								
15	0x67A								

MD_REFFLD — Control the updating time of reference field for motion detection.

0 Update reference field every field (default)

1 Update reference field according to MD_SPEED

MD_FIELD — Select the field for motion detection.

0 Detecting motion for only odd field (default)

1 Detecting motion for only even field

2 Detecting motion for any field

3 Detecting motion for both odd and even field

MD_LVSENS — Control the level sensitivity of motion detector.

0 More sensitive (default)

: :

15 Less sensitive

#	Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	0x603	MD_CELSENS		MD_SPEED					
1	0x60B								
2	0x613								
3	0x61B								
4	0x623								
5	0x62B								
6	0x633								
7	0x63B								
8	0x643								
9	0x64B								
10	0x653								
11	0x65B								
12	0x663								
13	0x66B								
14	0x673								
15	0x67B								

MD_CELSENS — Define the threshold of sub-cell number for motion detection.

0	Motion is detected if 1 sub-cell has motion (More sensitive) (default)
1	Motion is detected if 2 sub-cells have motion
2	Motion is detected if 3 sub-cells have motion
3	Motion is detected if 4 sub-cells have motion (Less sensitive)

MD_SPEED — Control the velocity of motion detector.
Large value is suitable for slow motion detection.

0	1 field intervals (default)
1	2 field intervals
:	:
61	62 field intervals
62	63 field intervals
63	Not supported

#	Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	0x604	MD_SPSENS				BD_LVSENS			
1	0x60C								
2	0x614								
3	0x61C								
4	0x624								
5	0x62C								
6	0x634								
7	0x63C								
8	0x644								
9	0x64C								
10	0x654								
11	0x65C								
12	0x664								
13	0x66C								
14	0x674								
15	0x67C								

MD_SPSENS — Control the spatial sensitivity of motion detector.

0 More Sensitive (default)

: :

15 Less Sensitive

BD_LVSENS — Define the threshold of level for blind detection.

0 Low threshold (More sensitive) (default)

: :

15 High threshold (Less sensitive)

#	Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	0x605	ND_TMPSENS				ND_LVSENS			
1	0x60D								
2	0x615								
3	0x61D								
4	0x625								
5	0x62D								
6	0x635								
7	0x63D								
8	0x645								
9	0x64D								
10	0x655								
11	0x65D								
12	0x665								
13	0x66D								
14	0x675								
15	0x67D								

ND_TMPSENS — Define the threshold of temporal sensitivity for night detection.

0	Low threshold (More sensitive) (default)
:	:
15	High threshold (Less sensitive)

ND_LVSENS — Define the threshold of level for night detection.

0	Low threshold (More sensitive) (default)
:	:
3	High threshold (Less sensitive)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x680	MD_BASE_ADDR[7:0]							
0x681					MD_BASE_ADDR[11:8]			

MD_BASE_ADDR — The base address of the motion detection buffer. This address is in unit of 64K bytes. The generated DDR address will be {MD_BASE_ADDR, 16'h0000}. The default value should be 12'h000

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x682					MOTION_CH_SEL			

MOTION_CH_SEL — This controls the channel ID of the motion detection result shown in register 0x6A0 ~ 0x6B7. Before reading back motion result, always set this first.

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x686	MD_STRB [7:0]*							
0x687	MD_STRB [15:8]*							
0x688	NOVID_DET[7:0]*							
0x689	NOVID_DET[15:8]*							
0x68A	MD_DET[7:0]*							
0x68B	MD_DET[15:8]*							
0x68C	BD_DET[7:0]*							
0x68D	BD_DET[15:8]*							
0x68E	ND_DET[7:0]*							
0x68F	ND_DET[15:8]*							

* Read Only

MD_STRB[n]	MD strobe has been performed at channel n (read only)
NOVID_DET[n]	NO_VIDEO Detected from channel n (read only)
MD_DET[n]	Motion Detected from channel n (read only)
BD_DET[n]	Blind Detected from channel n (read only)
ND_DET[n]	Night Detected from channel n (read only)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x6A0	MOTION_FLAG[7:0]							
0x6A1	MOTION_FLAG[15:8]							
0x6A2	MOTION_FLAG[23:16]							
0x6A3	MOTION_FLAG[31:24]							
0x6A4	MOTION_FLAG[39:32]							
0x6A5	MOTION_FLAG[47:40]							
0x6A6	MOTION_FLAG[55:48]							
0x6A7	MOTION_FLAG[63:56]							
0x6A8	MOTION_FLAG[71:64]							
0x6A9	MOTION_FLAG[79:72]							
0x6AA	MOTION_FLAG[87:80]							
0x6AB	MOTION_FLAG[95:88]							
0x6AC	MOTION_FLAG[103:96]							
0x6AD	MOTION_FLAG[111:104]							
0x6AE	MOTION_FLAG[119:112]							
0x6AF	MOTION_FLAG[127:120]							
0x6B0	MOTION_FLAG[135:128]							
0x6B1	MOTION_FLAG[143:136]							
0x6B2	MOTION_FLAG[151:144]							
0x6B3	MOTION_FLAG[159:152]							
0x6B4	MOTION_FLAG[167:160]							
0x6B5	MOTION_FLAG[175:168]							
0x6B6	MOTION_FLAG[183:176]							
0x6B7	MOTION_FLAG[191:184]							

MOTION_FLAG 192 bit motion flag of the channel specified by MOTION_CH_SEL in 0x682

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x6B8	MD_DI_CNT[7:0]*							
0x6B9							MD_DI_CNT[9:8]*	

* Read only

MD_DI_CNT The motion cell count of a specific channel selected by 0x682. This is for DI purpose.

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x6BA	MD_DI_CELLSENS							
0x6BB	MD_DI_LVSENS							

MD_DI_CELLSENS The motion detection cell sensitivity for DI purpose

MD_DI_LVSENS The motion detection threshold level for DI purpose

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x6E0	MOTION_MASK[7:0]							
0x6E1	MOTION_ MASK [15:8]							
0x6E2	MOTION_ MASK [23:16]							
0x6E3	MOTION_ MASK [31:24]							
0x6E4	MOTION_ MASK [39:32]							
0x6E5	MOTION_ MASK [47:40]							
0x6E6	MOTION_ MASK [55:48]							
0x6E7	MOTION_ MASK [63:56]							
0x6E8	MOTION_ MASK [71:64]							
0x6E9	MOTION_ MASK [79:72]							
0x6EA	MOTION_ MASK [87:80]							
0x6EB	MOTION_ MASK [95:88]							
0x6EC	MOTION_ MASK [103:96]							
0x6ED	MOTION_ MASK [111:104]							
0x6EE	MOTION_ MASK [119:112]							
0x6EF	MOTION_ MASK [127:120]							
0x6F0	MOTION_ MASK [135:128]							
0x6F1	MOTION_ MASK [143:136]							
0x6F2	MOTION_ MASK [151:144]							
0x6F3	MOTION_ MASK [159:152]							
0x6F4	MOTION_ MASK [167:160]							
0x6F5	MOTION_ MASK [175:168]							
0x6F6	MOTION_ MASK [183:176]							
0x6F7	MOTION_ MASK [191:184]							

MOTION_MASK 192 bit motion mask of the channel specified by MASK_CH_SEL in 0x6FE

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x6FE				MASK_CH_SEL				

MASK_CH_SEL The channel selection to access masks in 0x6E0 ~ 0x6F7

0x1DC00 ~ 0x1DFFF: HD MD/BD/ND

Note: The front-end registers below are represented with offset address. The actual address is derived with 0x1C000 + 4 * offset

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x700 0x708			MD_DIS		MD_STRB	MD_STRB_E N	BD_CELLSENS	

MD_DIS — Disable the motion and blind detection.
- 0 Enable motion and blind detection (default)
- 1 Disable motion and blind detection

MD_STRB — Request to start motion detection on manual trigger mode
- 0 None Operation (default)
- 1 Request to start motion detection

MD_STRB_EN — Select the trigger mode of motion detection
- 0 Automatic trigger mode of motion detection (default)
- 1 Manual trigger mode for motion detection

BD_CELSENS — Define the threshold of cell for blind detection.
- 0 Low threshold (More sensitive) (default)
- : :
- 2 High threshold (Less sensitive)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x701 0x709	MD_TMPSENS				MD_PIXEL_OS			

MD_TMPSENS — Control the temporal sensitivity of motion detector.
- 0 More Sensitive (default)
- : :
- 15 Less Sensitive

MD_PIXEL_OS — Adjust the horizontal starting position for motion detection
- 0 0 pixel (default)
- : :
- 15 15 pixels

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x702 0x70A	MD_REFFLD	MD_FIELD		MD_LVSENS				

MD_REFFLD Control the updating time of reference field for motion detection.

0 Update reference field every field (default)

1 Update reference field according to MD_SPEED

MD_FIELD Select the field for motion detection.

0 Detecting motion for only odd field (default)

1 Detecting motion for only even field

2 Detecting motion for any field

3 Detecting motion for both odd and even field

MD_LVSENS Control the level sensitivity of motion detector.

0 More sensitive (default)

: :

15 Less sensitive

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x703 0x70B	MD_CELSENS		MD_SPEED					

MD_CELSENS Define the threshold of sub-cell number for motion detection.

0 Motion is detected if 1 sub-cell has motion (More sensitive) (default)

1 Motion is detected if 2 sub-cells have motion

2 Motion is detected if 3 sub-cells have motion

3 Motion is detected if 4 sub-cells have motion (Less sensitive)

MD_SPEED Control the velocity of motion detector.

Large value is suitable for slow motion detection.

In MD_DUAL_EN = 1, MD_SPEED should be limited to 0 ~ 31.

0 1 field intervals (default)

1 2 field intervals

: :

61 62 field intervals

62 63 field intervals

63 Not supported

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x704 0x70C	MD_SPSENS				BD_LVSENS			

MD_SPSENS Control the spatial sensitivity of motion detector.

0 More Sensitive (default)

: :

15 Less Sensitive

BD_LVSENS Define the threshold of level for blind detection.

0 Low threshold (More sensitive) (default)

: :

15 High threshold (Less sensitive)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x705 0x70D	ND_TMPSENS				ND_LVSENS			

ND_TMPSENS Define the threshold of temporal sensitivity for night detection.

0 Low threshold (More sensitive) (default)

: :

15 High threshold (Less sensitive)

ND_LVSENS Define the threshold of level for night detection.

0 Low threshold (More sensitive) (default)

: :

3 High threshold (Less sensitive)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x710	HD_BYTELANE_656		HD_MODE		HD_FLD_POL		HD_BYPASS_EC	
0x711			HD_INTER_PROG		HD_NOVID_POL		HD_DIS_NOVID	

Bit 0 of each parameter: HD1
Bit 1 of each parameter: HD2

HD_BYPASS_EC[n]	1'b0: don't bypass bt_xxx sync code. (Default) 1'b1: bypass bt_xxx sync code.
HD_FLD_POL[n]	1'b0: Normal mode (default) 1'b1: Invert field.
HD_MODE[n]	1'b0: Input stream is BT.656 format. 1'b1: Input stream is BT.1120 format.
HD_BYTELANE_656 [n]	1'b0: when in BT.656 mode, choose bit [7:0] as data. 1'b1: when in BT.656 mode, choose bit [15:8] as data.
HD_DIS_NOVID[n]	1'b0: Extract non-video bit in bt_xxx sync code. (Default) 1'b1: Don't extract non-video bit in bt_xxx sync code.
HD_NOVID_POL[n]	1'b0: Normal mode. (Default) 1'b1: Invert non-video.
HD_INTER_PROG[n]	1'b0: Input is interleaving video. (Default) 1'b1: Input is progressive video.

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x712	HD2_PREV_SEL		HD1_PREV_SEL		HD2_ENC_SEL		HD1_ENC_SEL	
0x713					HD2_JPEG_SEL		HD1_JPEG_SEL	

HDn_ENC_SEL	2'b00: Choose x/y-direction non downscale scale version. (Default) 2'b01: Choose x-direction 1/4 downscale, y-direction 1/2 downscale version. 2'b10: Choose both x/y-direction 1/2 down scale version. 2'b11: Choose x-direction 1/2 downscale, y-direction non downscale version
HDn_PREV_SEL	2'b00: Choose x/y-direction non downscale scale version. (Default) 2'b01: Choose x-direction 1/4 downscale, y-direction 1/2 downscale version. 2'b10: Choose both x/y-direction 1/2 down scale version. 2'b11: Choose x-direction 1/2 downscale, y-direction non downscale version
HDn_JPEG_SEL	2'b00: Choose x/y-direction non downscale scale version. (Default) 2'b01: Choose x-direction 1/4 downscale, y-direction 1/2 downscale version. 2'b10: Choose both x/y-direction 1/2 down scale version. 2'b11: Choose x-direction 1/2 downscale, y-direction non downscale version

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x720	HD1_cell_left_width				HD1_cell_right_width			
0x721	HD1_cell_up_height				HD1_cell_low_height			
0x730	HD2_cell_left_width				HD2_cell_right_width			
0x731	HD2_cell_up_height				HD2_cell_low_height			

HDn_cell_left_width	The HD Motion Cell width at the left hand quadrants	
	8:	1080i
	5:	720p
	6:	4D1 NTSC/PAL
	4:	WD1 NTSC/PAL
HDn_cell_right_width	The HD Motion Cell width at the right hand quadrants	
	7:	1080i
	5:	720p
	5:	4D1 NTSC/PAL
	3:	WD1 NTSC/PAL
HDn_cell_up_height	The HD Motion Cell width at the upper 2 quadrants	
	B:	1080i
	F:	720p
	C:	4D1/WD1 NTSC/PAL
HDn_cell_lower_height	The HD Motion Cell width at the lower 2 quadrants	
	B:	1080i
	F:	720p
	C:	4D1 NTSC/PAL
	X:	WD1

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x780	HD1_MD_BASE_ADDR[7:0]							
0x781					HD1_MD_BASE_ADDR[11:8]			

HD1_MD_BASE_ADDR

The base address of the motion detection buffer for HD channel 1. This address is in unit of 64K bytes. The generated DDR address will be {HD1_MD_BASE_ADDR, 16'h0000}. The default value should be 12'h000

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x782					HD_RGR_MOTION_SEL			

HD_RGR_MOTION_SEL This controls the channel of the HD motion detection result shown in register 0x7A0 ~ 0x7B7. Before reading back motion result, always set this first. Since each HD channel has 4 * 192 bit of motion flag, therefore

0 Upper left quadrant of HD channel 1
1 Upper right quadrant of HD channel 1
2 Lower left quadrant of HD channel 1
3 Lower right quadrant of HD channel 1
4 Upper left quadrant of HD channel 2
5 Upper right quadrant of HD channel 2
6 Lower left quadrant of HD channel 2
7 Lower left quadrant of HD channel 2

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x786							HD_MD_STRB [1:0]*	
0x788							HD_NOVID_DET[1:0]*	
0x78A							HD_MD_DET[1:0]*	
0x78C							HD_BD_DET[1:0]*	
0x78E							HD_ND_DET[1:0]*	

* Read Only

Bit 0 of each parameter: HD1
Bit 1 of each parameter: HD2

HD_MD_STRB[n] MD strobe has been performed at HD channel n (read only)

HD_NOVID_DET[n] NO_VIDEO Detected from HD channel n (read only)

HD_MD_DET[n] Motion Detected from HD channel n (read only)

HD_BD_DET[n] Blind Detected from HD channel n (read only)

HD_ND_DET[n] Night Detected from HD channel n (read only)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x790	HD2_MD_BASE_ADDR[7:0]							
0x791					HD2_MD_BASE_ADDR[11:8]			

HD2_MD_BASE_ADDR The base address of the motion detection buffer for HD channel 2. This address is in unit of 64K bytes. The generated DDR address will be {HD2_MD_BASE_ADDR, 16'h0000}. The default value should be 12'h000

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x7A0	HD_MOTION_FLAG[7:0]							
0x7A1	HD_MOTION_FLAG[15:8]							
0x7A2	HD_MOTION_FLAG[23:16]							
0x7A3	HD_MOTION_FLAG[31:24]							
0x7A4	HD_MOTION_FLAG[39:32]							
0x7A5	HD_MOTION_FLAG[47:40]							
0x7A6	HD_MOTION_FLAG[55:48]							
0x7A7	HD_MOTION_FLAG[63:56]							
0x7A8	HD_MOTION_FLAG[71:64]							
0x7A9	HD_MOTION_FLAG[79:72]							
0x7AA	HD_MOTION_FLAG[87:80]							
0x7AB	HD_MOTION_FLAG[95:88]							
0x7AC	HD_MOTION_FLAG[103:96]							
0x7AD	HD_MOTION_FLAG[111:104]							
0x7AE	HD_MOTION_FLAG[119:112]							
0x7AF	HD_MOTION_FLAG[127:120]							
0x7B0	HD_MOTION_FLAG[135:128]							
0x7B1	HD_MOTION_FLAG[143:136]							
0x7B2	HD_MOTION_FLAG[151:144]							
0x7B3	HD_MOTION_FLAG[159:152]							
0x7B4	HD_MOTION_FLAG[167:160]							
0x7B5	HD_MOTION_FLAG[175:168]							
0x7B6	HD_MOTION_FLAG[183:176]							
0x7B7	HD_MOTION_FLAG[191:184]							

HD_MOTION_FLAG 192 bit motion flag of a quadrant of a HD channel specified by HD_RGR_MOTION_SEL in 0x782

HD_RGR_MOTION_SEL = 0 ~ 3 HD Channel 1
HD_RGR_MOTION_SEL = 4 ~ 7 HD Channel 2

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x7B8	HD_MD_DI_CNT[7:0]*							
0x7B9					HD_MD_DI_CNT[11:8]*			

* Read only

HD_MD_DI_CNT The motion cell count of a specific channel selected by HD_RGR_MOTION_SEL in 0x782. This is for DI (de-interlacing) purpose.

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x7BA	HD_MD_DI_CELLSENS							
0x7BB	HD_MD_DI_LVSENS							

HD_MD_DI_CELLSENS The motion detection cell sensitivity for DI purpose

HD_MD_DI_LVSENS The motion detection threshold level for DI purpose

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x7D0	HD_INTERRUPT[7:0]							

HD_INTERRUPT Interrupt status register from the front-end. Write “1” to each bit to clear the interrupt

1:0 Motion detection interrupt for HD channel 1 ~ 2
3:2 Night detection interrupt for HD channel 1 ~ 2
5:4 Blind detection interrupt for HD channel 1 ~ 2
7:6 No video interrupt for HD channel 1 ~ 2

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x7D1	HD_INTERRUPT_MASK[7:0]							

HD_INTERRUPT_MASK Interrupt mask register for interrupts in 0x7D0.

1:0 Motion detection interrupt mask for HD channel 1 ~ 2
3:2 Night detection interrupt mask for HD channel 1 ~ 2
5:4 Blind detection interrupt mask for HD channel 1 ~ 2
7:6 No video interrupt for mask HD channel 1 ~ 2

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x7DF	HD_MASKED_INTERRUPT							

HD_MASKED_INTERRUPT Interrupt status masked with0x7D1register

HD_MASKED_INTERRUPT = HD_INTERRUPT & HD_INTERRUPT_MASK

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x7E0	HD_MD_MASK[7:0]							
0x7E1	HD_MD_ MASK [15:8]							
0x7E2	HD_MD_ MASK [23:16]							
0x7E3	HD_MD_ MASK [31:24]							
0x7E4	HD_MD_ MASK [39:32]							
0x7E5	HD_MD_ MASK [47:40]							
0x7E6	HD_MD_ MASK [55:48]							
0x7E7	HD_MD_ MASK [63:56]							
0x7E8	HD_MD_ MASK [71:64]							
0x7E9	HD_MD_ MASK [79:72]							
0x7EA	HD_MD_ MASK [87:80]							
0x7EB	HD_MD_ MASK [95:88]							
0x7EC	HD_MD_ MASK [103:96]							
0x7ED	HD_MD_ MASK [111:104]							
0x7EE	HD_MD_ MASK [119:112]							
0x7EF	HD_MD_ MASK [127:120]							
0x7F0	HD_MD_ MASK [135:128]							
0x7F1	HD_MD_ MASK [143:136]							
0x7F2	HD_MD_ MASK [151:144]							
0x7F3	HD_MD_ MASK [159:152]							
0x7F4	HD_MD_ MASK [167:160]							
0x7F5	HD_MD_ MASK [175:168]							
0x7F6	HD_MD_ MASK [183:176]							
0x7F7	HD_MD_ MASK [191:184]							

HD_MD_MASK 192 bit motion mask of the channel specified by MASK_CH_SEL in 0x7FE

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x7FE				HD_MASK_CH_SEL				

HD_MASK_CH_SEL The channel selection to access masks in 0x7E0 ~ 0x7F7

0x1F400 ~ 0x1F7FF: DDR2 PHY Control

Note: The front-end registers below are represented with offset address. The actual address is derived with 0x1C000 + 4 * offset

For detailed description of the DDR2 PHY setup, please refer to the separate Application Note: "TW5866 DDR2 PHY setup"

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xD00								DFI_INIT_C

DFI_INIT_C: DDR2 PHY Initialization complete (Read Only)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xD10	0	0	0	0	0	1	0	0

Reserved. Do not overwrite.

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xD11	PHY_BOARD_LPBK_TX		PHY_CLK_STALL_LVL	PHY_AT_SPD_ATPG	0	PHY_LOOPBK	0	0

PHY_LOOPBK — Loopback testing.
1 enable,
0 disable;

PHY_AT_SPD_ATPG — This is for delay line
1 Test with full clock speed but lower coverage.
0 Test with lower clock speed but higher coverage.

PHY_CLK_STALL_LVL — This port determines whether delay line clock stalls at low level. The expected input is a very slow clock to asymmetric aging in delay lines.

PHY_BOARD_LPBK_TX — External Board Loopback testing.
1 This Slice behaves as Transmitter for board loopback.
0 Default

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xD12							PHY_BOARD_LPBK_RX	

PHY_BOARD_LPBK_RX — External Board Loopback testing.
1 This Slice behaves as receiver for board loopback.
0 Disable

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xD13	PHY_DQ_OFFSET[7:0]							
0xD14			PHY_DQ_OFFSET[13:8]					

PHY_DQ_OFFSET — Offset value from DQS to DQ. Default value: 0x40 (for 90 degree shift).

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xD15	PHY_GATELVL_INIT_RATIO[7:0]							
0xD16	PHY_GATELVL_INIT_RATIO[15:8]							
0xD17		PHY_GATELVL_INIT_MD	PHY_GATELVL_INIT_RATIO[21:16]					

PHY_GATELVL_INIT_RATIO [10:0] Default value 0; when inverted clock: 'h48;

PHY_GATELVL_INIT_RATIO [21:11] Default value 0; when inverted clock: 'h48;

PHY_GATELVL_INIT_MD The user programmable init ratio selection mode
1 Selects a starting ratio value based on PHY_GATELVL_INIT_RATIO port.
0 Selects a starting ratio value based on Write Leveling of the same data slice. (Default)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xD18					PHY_GATELVL_NUM_OF_DQ0			

PHY_GATELVL_NUM_OF_DQ0 This register value determines the number of samples for DDR data DQ0 input for each ratio increment by the Gate Training FSM. (Default 4'h9)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xD19	PHY_CTRL_SLAVE_RATIO[7:0]							
0xD1A							PHY_CTRL_SLAVE_RATIO[9:8]	

PHY_CTRL_SLAVE_RATIO Ratio value for address/command launch timing in phy_ctrl macro. This is the fraction of a clock cycle represented by the shift to be applied to the read DQS in units of 256ths. In other words, the full-cycle tap value from the master DLL will be scaled by this number over 256 to get the delay value for the slave delay line. (Default 10'h80)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xD1B	PHY_CTRL_SLAVE_DELAY[7:0]							
0xD1C							PHY_CTRL_SLAVE_FORCE	PHY_CTRL_SLAVE_DELAY[8]

PHY_CTRL_SLAVE_DELAY If PHY_RD_DQS_SLAVE_FORCE is 1, replace delay/tap value for address/command timing slave DLL with this value (Default 0)

PHY_CTRL_SLAVE_FORCE 1 Overwrite the delay/tap value for address/command timing slave DLL with the value of the PHY_RD_DQS_SLAVE_DELAY.

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xD1D	PHY_RD_DQS_SLAVE_RATIO[7:0]							
0xD1E	PHY_RD_DQS_SLAVE_RATIO[15:8]							
0xD1F			PHY_RD_DQS_SLAVE_FORCE		PHY_RD_DQS_SLAVE_RATIO[19:16]			

PHY_RD_DQS_SLAVE_RATIO Ratio value for read DQS slave DLL. This is the fraction of a clock cycle represented by the shift to be applied to the read DQS in units of 256ths. In other words, the full-cycle tap value from the master DLL will be scaled by this number over 256 to get the delay value for the slave delay line (Default 20'h10040)

PHY_RD_DQS_SLAVE_FORCE Overwrite the delay/tap value for read DQS slave DLL with the value of the PHY_RD_DQS_SLAVE_DELAY (Default 0)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xD20	PHY_RD_DQS_SLAVE_DELAY[7:0]							
0xD21	PHY_RD_DQS_SLAVE_DELAY[15:8]							
0xD22							PHY_RD_DQS_SLAVE_DELAY[17:16]	

PHY_RD_DQS_SLAVE_DELAY — If PHY_RD_DQS_SLAVE_FORCE is 1, replace delay/tap value for read DQS slave DLL with this value (Default 0)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xD23	PHY_FIFO_WE_SLAVE_RATIO[7:0]							
0xD24	PHY_FIFO_WE_SLAVE_RATIO[15:8]							
0xD25			PHY_FIFO_WE_SLAVE_RATIO[21:16]					

PHY_FIFO_WE_SLAVE_RATIO — Default 22'h020040.

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xD26	PHY_FIFO_WE_IN_DELAY[7:0]							
0xD27	PHY_FIFO_WE_IN_DELAY [15:8]							
0xD28					PHY_FIFO_WE_IN_FORCE		PHY_FIFO_WE_IN_DELAY [17:16]	

PHY_FIFO_WE_IN_DELAY — Delay value to be used when PHY_FIFO_WE_IN_FORCE is set to 1. (Default 0)

PHY_FIFO_WE_IN_FORCE — Overwrite the delay/tap value for fifo_we slave DLL with the value of the PHY_FIFO_WE_IN_DELAY. (Default 0)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xD29	PHY_WR_DATA_SLAVE_RATIO[7:0]							
0xD2A	PHY_WR_DATA_SLAVE_RATIO[15:8]							
0xD2B					PHY_WR_DATA_SLAVE_RATIO[19:16]			

PHY_WR_DATA_SLAVE_RATIO — Defaut value: 'h10040.
Ratio value for write data slave DLL. This is the fraction of a clock cycle represented by the shift to be applied to the write DQ muxes in units of 256ths. In other words, the full-cycle tap value from the master DLL will be scaled by this number over 256 to get the delay value for the slave delay line.

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xD2C	PHY_WR_DATA_SLAVE_DELAY[7:0]							
0xD2D	PHY_WR_DATA_SLAVE_DELAY[15:8]							
0xD2E					PHY_WR_DATA_SLAVE_FORCE		PHY_WR_DATA_SLAVE_DELAY[17:16]	

PHY_WR_DATA_SLAVE_DELAY — Default value 0.
If PHY_WR_DATA_SLAVE_FORCE is 1, replace delay/tap value for write data slave DLL with this value.

PHY_WR_DATA_SLAVE_FORCE — Default value 0.
1 — Overwrite the delay/tap value for write data slave DLL with the value of the PHY_WR_DATA_SLAVE_DELAY.

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xD2F				PHY_WR_RL_DELAY				
0xD30				PHY_RD_RL_DELAY				
0xD31				1	PHY_DLL_LOCK_DIFF			

PHY_WR_RL_DELAY Default value 'h01.
This delay determines when to select the active bank ratio logic delay for Write Data and Write DQS slave delay lines after PHY receives a write command at Control Interface.

PHY_RD_RL_DELAY Default value 'h01
This delay determines when to select the active rank's ratio logic delay for FIFO_WE and Read DQS slave delay lines after PHY receives a read command at Control Interface.

PHY_DLL_LOCK_DIFF Default value 1
The maximum number of delay line taps variation allowed while maintaining the master DLL lock.

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xD32	PHY_WR_LOCAL_ODT		PHY_DATA_SLICE_IN_USE		PHY_RDC_WE_TO_RE_DELAY			
0xD33	PHY_RDC_FIFO_RST_ERR_CNT_CLR	PHY_DIS_CALIB_RST	PHY_USE_FIX_RE	PHY_USE_RD_DQS_GATELVL	PHY_IDLE_LOCAL_ODT		PHY_RD_LOCAL_ODT	
0xD34				PHY_INVERT_CKOUT	0	0	0	0

PHY_RDC_WE_TO_RE_DELAY Default value 'h4.
Read Capture FIFO read is enabled after (first_rd + rdc_we_to_re_delay +1) clock cycles. Valid if „use_fixed_re" is high.

PHY_DATA_SLICE_IN_USE Default value 'h3.
Data bus width selection for Read FIFO RE generation. One bit for each data slice. 1: data slice is valid. 0: read data responses are ignored.

PHY_WR_LOCAL_ODT Set the write-side ODT (on-die termination) impedance value

PHY_RD_LOCAL_ODT Set the read-side ODT impedance value

PHY_IDLE_LOCAL_ODT Set the idle ODT value

PHY_USE_FIX_RE Default value 1
PHY generates FIFO read enable after fixed number of clock cycles as defined by PHY_RDC_WE_TO_RE_DELAY [3:0].

PHY uses nonempty flag to do the read enable generation.

PHY_DIS_CALIB_RST Default value 0. Disable the resetting of the Read Capture FIFO pointers with dll_calib (internally generated signal). The pointers are reset to ensure that the PHY can recover if the appropriate number of DQS edges is not observed after a read command (which can happen when the DQS squelch timing is manually overridden via the debug registers).
0: enable, 1: disable.

PHY_RDC_FIFO_RST_ERR_CNT_CL — Default 0. Clear/reset for counter

PHY_INVERT_CKOUT — Default 0. Inverts the polarity of DRAM clock.
0 core clock is passed on to DRAM.
1 inverted core clock is passed on to DRAM.

NOTE: **THE REGISTERS BELOW (0XD36 ~ 0XD50) ARE READ ONLY**

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xD37	PHY_RDLVL_FIFOWEIN_RATIO[7:0]							
0xD38	PHY_RDLVL_FIFOWEIN_RATIO [15:8]							
0xD39			PHY_RDLVL_FIFOWEIN_RATIO [21:16]					

PHY_RDLVL_FIFOWEIN_RATIO — Ratio value generated by Read Gate training FSM.

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xD3A	PHY_DLL_SLAVE_VALUE[7:0]							
0xD3B								PHY_DLL_SLAVE_VALUE[8]

PHY_DLL_SLAVE_VALUE — Shows the current Coarse and Fine delay values going to all the Slave DLLs. Bit [1:0] is the fine value, and bit [8:2] is the coarse value.

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xD3C	PHY_IN_DELAY_VALUE[7:0]							
0xD3D								PHY_IN_DELAY_VALUE[8]

PHY_IN_DELAY_VALUE — The Coarse and Fine values going into the Output Filter in Master DLL. Bit [1:0] is the fine value, and bit [8:2] is the coarse value.

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xD3E	PHY_OUT_DELAY_VALUE[7:0]							
0xD3F					PHY_DLL_LOCK	PHY_IN_LOCK_STATE		PHY_OUT_DELAY_VALUE[8]

PHY_OUT_DELAY_VALUE — The Coarse and Fine values coming out of the Output Filter in Master DLL. Bit [1:0] is the fine value, and bit [8:2] is the coarse value.

PHY_IN_LOCK_STATE — Lock status from the Output Filter module inside the Master DLL.
Bit [0] – Fine lock
Bit [1] – Coarse lock

PHY_DLL_LOCK — Status signal
0 Master DLL is not locked
1 Master DLL is locked

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xD40	PHY_CTRL_DLL_SLAVE_VALUE[7:0]							
0xD41								PHY_CTRL_DLL_SLAVE_VALUE[8]

PHY_CTRL_DLL_SLAVE_VALUE — Shows the current Coarse and Fine delay value going to the PHY_CTRL Slave DLL. Bit [1:0] is the fine value, and bit [8:2] is the coarse value.

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xD42	PHY_CTRL_IN_DELAY_VALUE[7:0]							
0xD43								PHY_CTRL_IN_DELAY_VALUE[8]

PHY_CTRL_IN_DELAY_VALUE — The Coarse and Fine values going into the Output Filter in PHY_CTRL Master DLL. Bit [1:0] is the fine value, and bit [8:2] is the coarse value.

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xD44	PHY_CTRL_OUT_DELAY_VALUE[7:0]							
0xD45					PHY_CTRL_DLL_LOCK	PHY_CTRL_IN_LOCK_STATE		PHY_CTRL_OUT_DELAY_VALUE[8

PHY_CTRL_OUT_DELAY_VALUE — The Coarse and Fine values coming out of the Output Filter in PHY_CTRL Master DLL. Bit [1:0] is the fine value, and bit [8:2] is the coarse value.

PHY_CTRL_IN_LOCK_STAT — Lock status from the Output Filter module inside the PHY_CTRL Master DLL

Bit [0] – Fine delay line lock status.

1: locked, 0: unlocked.

Bit [1] – Coarse delay line lock status.

1: locked, 0: unlocked.

PHY_CTRL_DLL_LOCK — PHY_CTRL Master DLL Status signal:

1 – Master DLL is locked

0 – Master DLL is not locked

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xD46	PHY_RD_DQS_SLAVE_DLL_VALUE [7:0]							
0xD47	PHY_RD_DQS_SLAVE_DLL_VALUE [15:8]							
0xD48							PHY_RD_DQS_SLAVE_DLL_VALUE[17:16]	

PHY_RD_DQS_SLAVE_DLL_VALUE — Delay value applied to read DQS slave DLL.

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xD49	PHY_WR_DATA_SLAVE_DLL_VALUE [7:0]							
0xD4A	PHY_ WR_DATA _SLAVE_DLL_VALUE [15:8]							
0xD4B							PHY_WR_DATA_SLAVE_DLL_VALUE[17:16]	

PHY_WR_DATA_SLAVE_DLL_VALUE — Delay value applied to write data slave DLL.

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xD4C	PHY_FIFO_WE_SLAVE_DLL_VALUE [7:0]							
0xD4D	PHY_ FIFO_WE _SLAVE_DLL_VALUE [15:8]							
0xD4E							PHY_FIFO_WE_SLAVE_DLL_VALUE[17:16]	

PHY_FIFO_WE_SLAVE_DLL_VALUE Delay value applied to FIFO WE slave DLL.

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xD4F	PHY_CTRL_SLAVE_DLL_VALUE[7:0]							
0xD50				PHY_RDC_FIFO_RST_ERR_CNT				PHY_CTRL_SLAVE_DLL_VALUE[8

PHY_CTRL_SLAVE_DLL_VALUE Shows the current Coarse and Fine delay value going to the PHY_CTRL Slave DLL. Bit [1:0] is the fine value, and bit [8:2] is the coarse value.

PHY_RDC_FIFO_RST_ERR_CNT Counter for counting how many times the pointers of read data capture FIFO are reset when the FIFO is not empty (an error). It saturates after reaching 4'hF. Cleared by PHY_RDC_FIFO_RST_ERR_CNT_CLR (0xD33).

0x1F800 ~ 0x1FBFF: MISC & PLL / Analog IP

Note: The front-end registers below are represented with offset address. The actual address is derived with 0x1C000 + 4 * offset

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xEA0	CODEC_RSTN[7:0]							
0xEA1	CODEC_RSTN[15:8]							
0xEA2	CODEC_RSTN[23:16]							
0xEA3	CODEC_RSTN[31:24]							
0xEA4	CODEC_RSTN[39:32]							

CODEC_RSTN [0]	H264 Core RSTN
CODEC_RSTN [1]	DSP Interface RSTN
CODEC_RSTN [4]	Arbiter 12 RSTN
CODEC_RSTN [5]	Audio Encoder RSTN
CODEC_RSTN [6]	DDR Controller RSTN
CODEC_RSTN [7]	EMUIF RSTN
CODEC_RSTN [8]	EMUIF OPB RSTN
CODEC_RSTN [9]	IIC RSTN
CODEC_RSTN [10]	IRQ RSTN
CODEC_RSTN [11]	JPEG RSTN
CODEC_RSTN [12]	MV Detection RSTN
CODEC_RSTN [13]	MVF PCI RSTN
CODEC_RSTN [14]	MVF DDR RSTN
CODEC_RSTN [15]	MVF R/W RSTN
CODEC_RSTN [16]	PCI APP MAS RSTN
CODEC_RSTN [17]	PCI PREV RSTN
CODEC_RSTN [18]	PCI VLC RSTN
CODEC_RSTN [19]	PCI AUDIO RSTN
CODEC_RSTN [21]	PLBK RSTN
CODEC_RSTN [22]	VD INF RSTN
CODEC_RSTN [23]	VD INF V RSTN
CODEC_RSTN [24]	VP INF RSTN
CODEC_RSTN [25]	VP INF V RSTN
CODEC_RSTN [26]	VJ INF RSTN
CODEC_RSTN [27]	VJ INF V RSTN
CODEC_RSTN [28]	FRM HD V RSTN
CODEC_RSTN [29]	FRM HD RSTN
CODEC_RSTN [30]	SENIF HD RSTN
CODEC_RSTN [31]	PLBK 0 RSTN
CODEC_RSTN [32]	PLBK 1 RSTN

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xEB0		CLK108_PD		CLK108_IREF	CLK108_CPX4		CLK108_LPX4	

CLK108_LPX4 — 108 MHz clock PLL loop filter select

0 — 80K Ohms
1 — 40K Ohms (default)
2 — 30K Ohms
3 — 20K Ohms

CLK108_CPX4 — 108 MHz clock PLL charge pump select

0 — 1 uA
1 — 5 uA (default)
2 — 10 uA
3 — 15 uA

CLK108_IREF — 108 MHz clock PLL current control

0 — Low current (default)
1 — Higher current (30% more)

CLK108_PD

0 — Do not power down 108 MHz PLL (default)
1 — Power down 108 MHz PLL

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xEB1	HDPLL_M[7:0]							
0xEB2				HDPLL_N[4:0]				
0xEB3	HDPLL_PD			HDPLL_M[8]			HDPLL_P[1:0]	
0xEB4	HDPLL_LP_X8		HDPLL_VCO		HDPLL_CP_SEL			HDPLL_IREF
0xEB5				HDPLL_RST				

The HD playback clock (74.25 MHz) is generated with an on-chip system clock PLL (HD_PLL) using input crystal clock of 27 MHz. The HD PLL frequency is controlled with the following equation.

$$CLK\_OUT = CLK\_IN * (M+1) / ((N+1) * P)$$

HDPLL_M — M parameter

HDPLL_N — N parameter

HDPLL_P — P parameter

HDPLL_IREF — SYSPLL bias current control

0 — Lower current (default)
1 — 30% higher current

HDPLL_CP_SEL — SYSPLL charge pump current selection

0 — 1.5 μA
1 — 4 μA
2 — 9 μA
3 — 19 μA

4	39 µA
5	79 µA
6	159 µA
7	319 µA

HDPLL_VCO Select the VCO range

0	100 ~ 300 MHz
1	150 ~ 400 MHz (default)
2	200 ~ 500 MHz
3	250 ~ 600 MHz

HDPLL_LP_X8 Loop resistor for PLLX8

00	140K
01	46.5K (default)
10	23.3K
11	16.4K

HDPLL_RST PLL Reset

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xEB6		MPLL_F						
0xEB7	MPLL_OD			MPLL_R				
0xEB8	MPLL_LD				MPLL_PD	MPLL_BP	MPLL_BS	

The MPLL playback clock (333 MHz) is generated with an on-chip system clock PLL (MPLL) using input crystal clock of 27 MHz. The MPLL frequency is controlled with the following equation.

$$MCLK = CLK\_IN * (F+1) / ((R+1) * NO)$$

MPLL_F Feedback divider value F

MPLL_R Input divider value R

MPLL_OD Select Output Divider value NO

00	1
01	2
10	4
11	8

MPLL_PD Power Down mode

1	No MCLK output
0	Normal MCLK output

MPLL_BP Bypass

0	Normal Output
1	MCLK = CLK_IN

MPLL_BS Band Selection

00	Low-band
01	Middle-band
10	High-band
11	Forbiddance

MPLL_LD Read only

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xEBB		SYSPLL_F						
0xEBC	SYSPLL_OD			SYSPLL_R				
0xEBD	SYSPLL_LD				SYSPLL_PD	SYSPLL_BP	SYSPLL_BS	

The SYSPLL playback clock (280 MHz) is generated with an on-chip system clock PLL (SYSPLL) using input crystal clock of 27 MHz. The SYSPLL frequency is controlled with the following equation.

SYS_CLK = CLK_IN * (F+1) / ((R+1) * OD)

SYSPLL_F Feedback divider value F

SYSPLL_R Input divider value R

SYSPLL_OD Select Output Divider value NO

00	1
01	2
10	4
11	8

SYSPLL_PD Power Down mode

0	Normal
1	No SYSCLK output

SYSPLL_BP Bypass

0	Normal
1	SYSCLK = CLK_IN

SYSPLL_BS Band Selection

00	Low-band
01	Middle-band
10	High-band
11	Forbiddance

SYSPLL_LD Read only

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xEC8	BYP_A2_AUD	BYP_A1_LINK			0	0	0	0
0xEC9	VADC8_PD	VADC7_PD	VADC6_PD	VADC5_PD	VADC4_PD	VADC3_PD	VADC2_PD	VADC1_PD
0xECA	AADC2_PD	AADC1_PD	ADAC_PD	ADAC_CK_P	AADC2_CK_P	AADC1_CK_P	VADC2_CK_P	VADC1_CK_P
0xECB		ADAC_TEST			ADAC_AOGAIN			
0xECC	ADAC_CK_INV	ADAC_LPF_SEL					ADAC_BIAS	ADAC_VCM

BYP_A2_AUD	0	Connect audio module 1 and 2 together
	1	Bypass audio module 2, and connect the module 1 signals to output ports
BYP_A1_LINK	0	Connect audio input pin ALINI to module 1 ALINKI
	1	Bypass audio module 1, and connect the audio input ALINKI to audio input pin of module 2 ALINKI
VADCn_PD	0	Normal Function
	1	Power down VADCn
VADC1_CK_P	0	Does not reverse the clock polarity of VADC1 ~ VADC4
	1	Reverse the clock polarity of VADC1 ~ VADC4
VADC2_CK_P	0	Does not reverse the clock polarity of VADC5 ~ VADC8
	1	Reverse the clock polarity of VADC5 ~ VADC8
AADC1_CK_P	0	Does not reverse the clock polarity of AADC1 ~ AADC5
	1	Reverse the clock polarity of AADC1 ~ AADC5
AADC2_CK_P	0	Does not reverse the clock polarity of AADC6 ~ AADC10
	1	Reverse the clock polarity of AADC6 ~ AADC10
ADAC_CK_P	0	Does not reverse the clock polarity of ADAC
	1	Reverse the clock polarity of ADAC
ADAC_PD	0	Normal Function
	1	Power down audio DAC
AADC1_PD	0	Normal Function
	1	Power down audio ADC1 ~ ADC5
AADC2_PD	0	Normal Function
	1	Power down audio ADC6 ~ ADC10
ADAC_AOGAIN	Audio DAC gain control	
ADAC_TEST	Audio DAC test control	
ADAC_VCM	Audio DAC VCM	

ADAC_BIAS Audio DAC Bias

ADAC_LPF_SEL Audio DAC LPF_SEL

ADAC_CK_INV Audio DAC clock polarity inversion

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xECD	AADC_GAIN2				AADC_GAIN1			
0xECE	AADC_GAIN4				AADC_GAIN3			
0xECF					AADC_GAIN51			
0xED0	AADC_GAIN6				AADC_GAIN5			
0xED1	AADC_GAIN8				AADC_GAIN7			
0xED2					AADC_GAIN52			

AADC_GAINn Audio ADCn gain control

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xEF0	FR_SW1_RST	FR_SW2_RST	FR_VD_RST					
0xEF8	PV1_CK_P		PV1_CK_SEL		PV1_CK_DLY			
0xEF9	PV2_CK_P		PV2_CK_SEL		PV2_CK_DLY			
0xEFA	PV2_SEL				PV1_SEL			

FR_SW1_RST Front-end Quad AV decoder module 1 software reset

0 Normal

1 Assert reset

FR_SW2_RST Front-end Quad AV decoder module 2 software reset

0 Normal

1 Assert reset

FR_VD_RST Software Reset Control for the front-end mux / capture modules

0 Normal

1 Reset

PVn_CK_P Preview Port n Clock output polarity control

0 Do not reverse the clock polarity

1 Reverse the clock polarity

PVn_CK_SEL Preview Port n Clock selection

0 27 MHz

1 54 MHz

2 54 MHz

3 108 MHz

PVn_CK_DLY Preview Port n Clock output delay line selection

	0	Smallest delay
	F	Largest delay
PV1_SEL	Selection preview port 1 sources	
	0	Port 1 ~ 4 (4 channel) 108 MHz byte interleaving
	1	Port 1 output in 27 MHz
	2	Port 2 output in 27 MHz
	3	Port 3 output in 27 MHz
	4	Port 4 output in 27 MHz
	5	Port 5 output in 27 MHz
	6	Port 6 output in 27 MHz
	7	Port 7 output in 27 MHz
	8	Port 8 output in 27 MHz
	9	Port 1 ~ 2 (2 channel) 54 MHz byte interleaving
	10	Port 3 ~ 4 (2 channel) 54 MHz byte interleaving
	11	Port 5 ~ 6 (2 channel) 54 MHz byte interleaving
	12	Port 7 ~ 8 (2 channel) 54 MHz byte interleaving
	13	Reserved
PV2_SEL	Selection preview port 2 sources	
	0	Port 5 ~ 8 (4 channel) 108 MHz byte interleaving
	1	Port 5 output in 27 MHz
	2	Port 6 output in 27 MHz
	3	Port 7 output in 27 MHz
	4	Port 8 output in 27 MHz
	5	Port 1 output in 27 MHz
	6	Port 2 output in 27 MHz
	7	Port 3 output in 27 MHz
	8	Port 4 output in 27 MHz
	9	Port 5 ~ 6 (2 channel) 54 MHz byte interleaving
	10	Port 7 ~ 8 (2 channel) 54 MHz byte interleaving
	11	Port 1 ~ 2 (2 channel) 54 MHz byte interleaving
	12	Port 3 ~ 4 (2 channel) 54 MHz byte interleaving
	13	Reserved

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xEFB	PB1_OUT_DLY				PB1_CLK_P	PB1_SEL1	PB1_SEL0	
0xEFC	PB2_OUT_DLY				PB2_CLK_P	PB2_SEL1	PB2_SEL0	
0xEFD				PB_CASD_P			HD_PB2	CASD_EN

PBn_OUT_DLY — Select PB port output clock delay

0 Smallest delay

F Largest delay

PBn_CLK_P — Select PB port output clock polarity

0 Do not reverse the clock polarity

1 Reverse the clock polarity

PBn_SEL0 — Select PB port n clock source

When PBn_SEL1 is 0

0 27 MHz

1 54 MHz

2 Reserved

3 108 MHz

When PBn_SEL1 is 1

0 HD1 Clock

1 HD2 clock

2 HDPLL clock

3 HD3 (cascade input) clock

PBn_SEL1 — Select PB port n clock source for either SD or HD purpose

0 SD clock sources, such as 27, 54, 108 MHz clock.

1 HD clock sources, such as HD1, HD2, HD3, or HDPLL clock source.

CASD_EN — Select PB_HD2 port as either playback or cascade input port

0 Cascade input port

1 PB_HD2 output port

HD_PB2 — Select PB2 port as HD

0 PB2 port is SD 656

1 PB2 port is bit 15:8 of PB_HD1

PB_CASD_P — Reverse the VD3 clock input polarity as a playback clock

0 Do not reverse clock polarity

1 Reverse the clock polarity

Parametric Information

Absolute Maximum Ratings (TA = +25°C)

Supply Voltage
- VDDI .... +1.2V
- VDDO .... +3.96V
- VDDSSTL .... +1.2V
- VDDPSSTL .... +2.0V
- VREFSSTL .... +1.2V
- VDDSYSPLL, VDDMPLL .... +1.2V
- VDDSPLL, VDDHDPLL .... +3.96V
- VDDVADC, VDDAADC, VDDADAC .... +3.96V

Voltage on any Digital Signal Pin
- (See the note below)........................ -0.3V to VDDO+0.3V

Analog Video Input Voltage .... -0.3V to VDDVADC+0.3V
Analog Audio Input Voltage .... -0.3V to VDDAADC+0.3V

Thermal Information

- Storage Temperature Range .... -55°C to +125°C
- Junction Temperature Range .... -40°C to +125°C
- Pb-free Reflow Profile .... see link below
  http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTE: This device employs high-impedance CMOS devices on all signal pins. It must be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the ranges list in Absolute Maximum Ratings can induce destructive latch-up.

AC/DC Electrical Parameters

PARAMETER	SYMBOL	MIN (NOTE 1)	TYPICAL	MAX (NOTE 1)	UNITS
POWER SUPPLY					
Power Supply — Digital Core	V_{VDDI}	0.9	1.0	1.1	V
	I_{VDDI}		652		mA
Power Supply — Digital I/O	V_{VDDO}	2.97	3.3	3.63	V
	I_{VDDO}		78		mA
Power Supply — SSTL Core	$V_{VDDSSTL}$	0.9	1.0	1.1	V
	$I_{VDDSSTL}$		633		mA
Power Supply — SSTL I/O	$V_{VDDPSSTL}$	1.7	1.8	1.9	V
	$I_{VDDPSSTL}$		267		mA
SSTL VREF	$V_{VREFSSTL}$	0.49 * $V_{VDDPSSTL}$	0.9	0.51 * $V_{VDDPSSTL}$	V
	$I_{VREFSSTL}$		10		mA
Power Supply — SYSPLL / MPLL	$V_{VDDSYSPLL}$ $V_{VDDMPLL}$	0.9	1.0	1.1	V
	$I_{VDDSYSPLL}$, $I_{VDDMPLL}$		3.6		mA
Power Supply — SPLL / HDPLL	$V_{VDDSPLL}$ $V_{VDDHDPLL}$	2.97	3.3	3.63	V
	$I_{VDDSPLL}$, $I_{VDDHDPLL}$		3.8		mA
Power Supply — Video A/D, Audio A/D, D/A	$V_{VDDVADC}$, $V_{VDDAADC}$, $V_{VDDADAC}$	2.97	3.3	3.63	V

PARAMETER	SYMBOL	MIN (NOTE 1)	TYPICAL	MAX (NOTE 1)	UNITS
	$I_{VDDVADC}$, $I_{VDDAADC}$, $I_{VDDADAC}$		368		mA
Ambient Operating Temperature	T_A	0		+70	°C
DIGITAL INPUTS					
Input High Voltage (TTL)	V_{IH}	2.0		3.6	V
Input Low Voltage (TTL)	V_{IL}	-0.3		0.8	V
Input High Current (V_{IN} = V_{DD})	I_{IH}			10	µA
Input Low Current (V_{IN} =V_{SS})	I_{IL}			–10	µA
Input Capacitance (f = 1MHz, V_{IN} = 2.4V)	C_{IN}		6		pF
DIGITAL OUTPUTS					
Output High Voltage (IOH = –4mA)	V_{OH}	2.4		VDD0	V
Output Low Voltage (IOL = 4mA)	V_{OL}			0.4	V
3-State Current	I_{OZ}			10	µA
Output Capacitance	C_O		6		pF

NOTE:

1. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

Video Decoder AC/DC Specifications

PARAMETER	SYMBOL	MIN (NOTE 1)	TYPICAL	MAX (NOTE 1)	UNITS
ANALOG INPUTS					
Analog Pin Input Voltage at VIN1, VIN2, VIN3, VIN4, VIN5, VIN6, VIN7, VIN8, AIN1, AIN2, AIN3, AIN4, AIN5, AIN6, AIN7, AIN8, AIN51, AIN52 Input Range (AC Coupling Required)	Vi	0	1.0	2.0	Vpp
Analog Pin Input Capacitance	C_A		6		pF
ADCS					
	ADCR		10		bits
	AINL		±1		LSB
	ADNL		±1		LSB
	f_{ADC}		27		MHz
HORIZONTAL PLL					
Line Frequency (50Hz)	f_{LN}		15.625		kHz
Line Frequency (60Hz)	f_{LN}		15.734		kHz
Static Deviation	Δf_H			6.2	%
SUBCARRIER PLL					
Subcarrier Frequency (NTSC-M)	f_{SC}		3579545		Hz
Subcarrier Frequency (PAL-BDGHI)	f_{SC}		4433619		Hz
Subcarrier Frequency (PAL-M)	f_{SC}		3575612		Hz
Subcarrier Frequency (PAL-N)	f_{SC}		3582056		Hz
Lock In Range	Δf_H	±450			Hz
SUBCARRIER PLL					
Nominal Frequency (Fundamental)			27		MHz
Deviation				±50	ppm
Temperature Range	T_A	0		70	°C
Load Capacitance	CL		20		pF
Series Resistor	RS		80		Ω

NOTE:

1. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

DDR2 Interface Electrical Characteristics

SYMBOL	PARAMETER	MIN (NOTE 1)	MAX (NOTE 1)	UNITS
V_{IH}(DC)	DC Input High (logic 1) Voltage	V_{REF} + 125	$V_{VDDPSSTL}$	mV
V_{IL}(DC)	DC Input Low (logic 0) Voltage	-300	V_{REF} - 125	mV
V_{IH}(AC)	Maximum AC Input Logic High	V_{REF} + 0.2V	$V_{VDDPSSTL}$	mV
V_{IL}(AC)	Minimum AC Input Logic Low	-0.3V	V_{REF} – 0.2V	
VOX	AC Differential Cross-Point Voltage	0. 5 x $V_{VDDPSSTL}$ - 125	0. 5 x $V_{VDDPSSTL}$ + 125	V/ns
V_{SWING}	AC Differential Voltage Swing	1		V

NOTE:

1. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

DDR2 Interface AC Timing

SYMBOL	PARAMETER	MIN (NOTE 1)	MAX (NOTE 1)	UNITS
CLOCK				
t_{CK}	Clock Cycle Time	3	8	Ns
t_{CH}	Clock High Level Width	0.48	0.52	tCK
t_{CL}	Clock Low Level Width	0.48	0.52	tCK
t_{AC}	DQ Input Access Time from CK/CK#	-450	450	Ps
t_{HP}	Half Clock Period	min(tCH,tCL)		
t_{JITper}	Period Jitter	-125	125	Ps
t_{JITcc}	Cycle to Cycle Jitter		250	Ps
DATA STROBE-IN				
t_{DQSCK}	Access Window of DQS Input from CK/CK#	-400	400	Ps
t_{RPRE}	DQS Read Preamble	0.9	1.1	tCK
t_{RPST}	DQS Read Postamble	0.4	0.6	tCK
DATA STROBE-OUT				
t_{DQSS}	DQS Rising Edge to Clock Rising Edge	-0.25	0.25	tCK
t_{DQSH}	DQS High Pulse Width	0.35		tCK
t_{DQSL}	DQS Low Pulse Width	0.35		tCK
t_{DSS}	DQS Falling to CK Rising: Setup Time	0.2		tCK
t_{DSH}	DQS Falling from CK Rising Hold Time	0.2		tCK
t_{WPRE}	DQS Write Preamble	0.35		tCK
t_{WPST}	DQS Write Postamble	0.4	0.6	tCK
DATA IN				
t_{AC}	DQ Input Access Time from CK/CK#	-450	450	ps
t_{DQSQ}	DQS-DQ Skew, DQS to last DQ Valid, Per Group		240	ps
t_{QHS}	DQ Hold From Next DQS Strobe		340	ps
DVW	Data Valid Input Window	tHP – tQHS - tDQSQ		
DATA OUT				
t_{DS}	DQ and DM Output Setup Time Relative to DQS	300		ps
t_{DH}	DQ and DM Output Hold Time Relative to DQS	300		ps
ADDRESS AND COMMAND				

SYMBOL	PARAMETER	MIN (NOTE 1)	MAX (NOTE 1)	UNITS
t_{IS}	Address and Control Output Setup Time	400		ps
t_{IH}	Address and Control Output Hold Time	400		ps

NOTE:

1. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
2. The Vref on the evaluation is 0.9v. VDDQ is 1.8v.
3. For all the timing, please refer to the figures below.

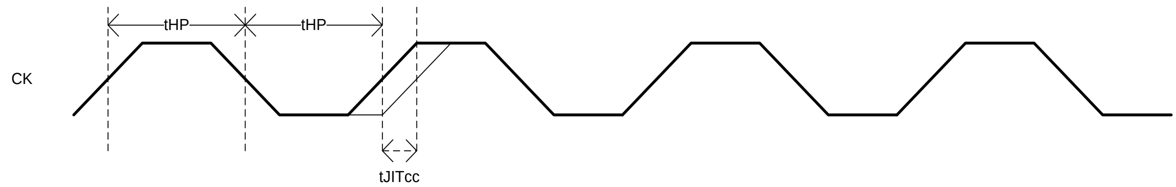


FIGURE 38. DDR2 INTERFACE CLOCK TIMING

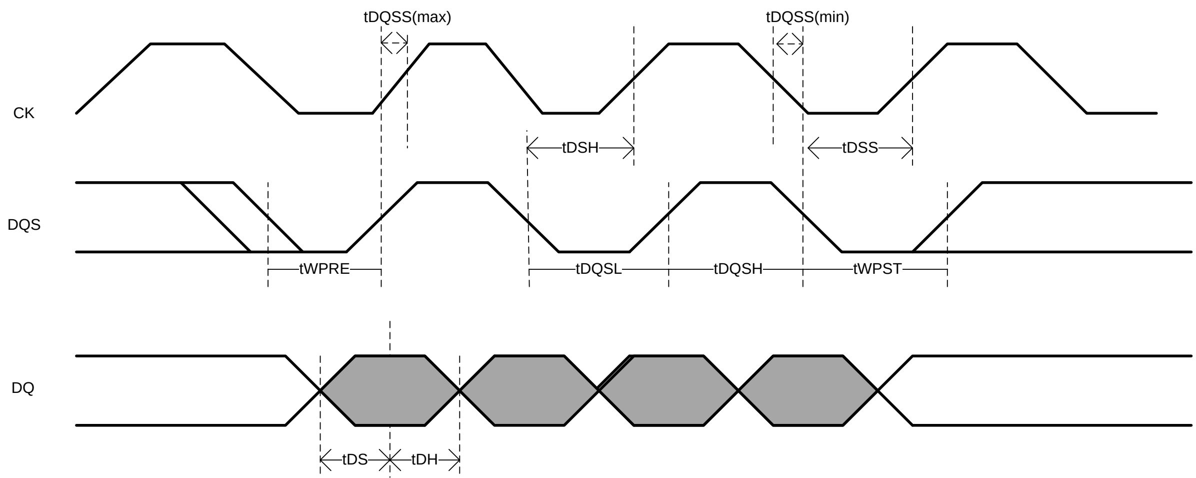


FIGURE 39. DDR2 INTERFACE OUTPUT TIMING

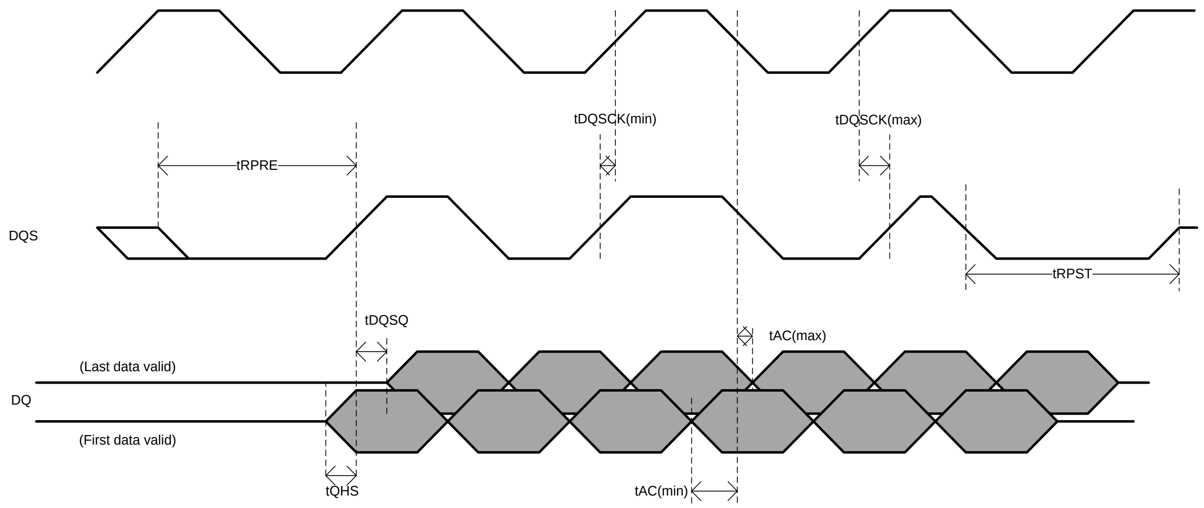


FIGURE 40. DDR2 INTERFACE INPUT TIMING

PCI Interface AC Timing

SYMBOL	PARAMETER	66 MHZ MIN (NOTE 1)	66 MHZ MAX (NOTE 1)	33 MHZ MIN (NOTE 1)	33 MHZ MAX (NOTE 1)	UNITS
t_{SU}	Input Setup Time to PCI_CLK – Bused Signals	3		7		ns
$t_{SU(PTP)}$	Input Setup Time to PCI_CLK – Point-to-Point	5		10, 12(4)		ns
t_H	Input Hold Time from PCI_CLK	0		0		ns
t_{VAL}	PCI_CLK to Signal Valid Delay – Bused Signals	2	8.5	2	11	ns
$t_{VAL(PTP)}$	PCI_CLK to Signal Valid Delay – Point-to-Point	2	7.5	2	12	ns
t_{ON}	Float to Active Delay	2		2		ns
t_{OFF}	Active to Float Delay		14		28	ns
t_{CYCLE}	PCI_CLK Cycle Time	15	30	30		ns
t_{HIGH}	PCI_CLK High Time	6		11		ns
t_{LOW}	PCI_CLK Low Time	6		11		ns
t_{RST}	Reset Active Time After Power Stable	1		1		ms
$t_{RST-CLK}$	Reset Active Time After PCI_CLK Stable	100		100		µs
$t_{RST-OFF}$	Reset Active to Output Float		40		40	ns

NOTE:

1. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
2. See PCI Signal Timing Measurement Conditions.
3. All interface signals are synchronized to PCI_CLK.
4. Point-to-point signals are PCI_REQ_N, PCI_GNT_N. Bused signals are PCI_AD, PCI_CBE_N, PCI_PAR, PCI_PERR_N, PCI_SERR_N, PCI_STOP_N, PCI_FRAME_N, PCI_IRDY_N, PCI_TRDY_N, PCI_DEVSEL_N, and PCI_IDSEL.
5. REQ_N signals have a setup of 10 and GNT_N signals have a setup of 12.

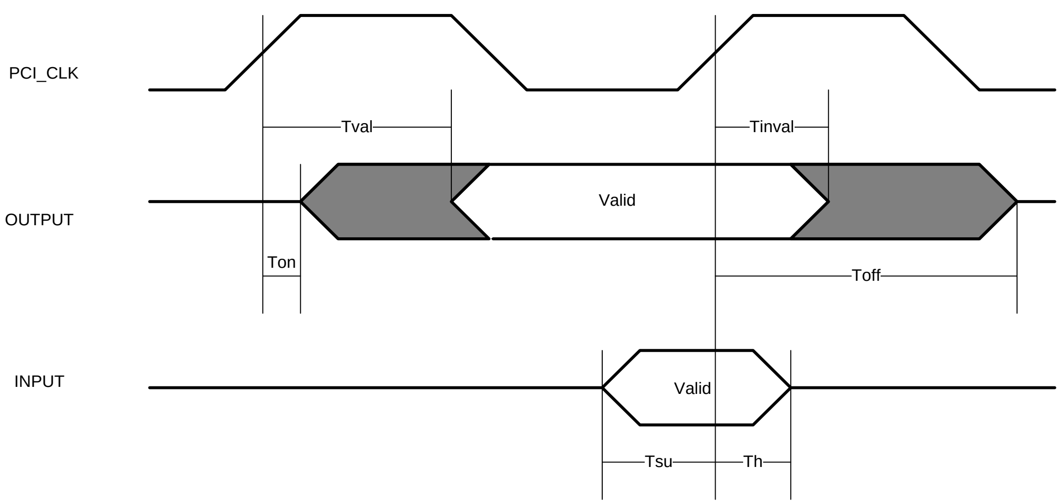


FIGURE 41. PCI INTERFACE TIMING CONDITION

Video Inputs AC Timing

SYMBOL	PARAMETER	MIN (NOTE 3)	MAX (NOTE 3)	UNITS
BT.656/8 BITS MODE/VDIX PORTS				
f_{ICK}	Video Input Clock Frequency	27	108	MHz
t_{ICK}	Video Input Clock Period	$1/f_{ICK}$(max)	$1/f_{ICK}$(min)	ns
t_{ISU}	Setup Time to Input Clock Rising Edge	2.5		ns
t_{IHD}	Hold Time to Input Clock Rising Edge	1		ns
BT.1120/16 BITS MODE/HDIX PORTS				
f_{ICK}	Video Input Clock Frequency	74.25	148.5	MHz
t_{ICK}	Video Input Clock Period	$1/f_{ICK}$(max)	$1/f_{ICK}$(min)	ns
t_{ISU}	Setup Time to Input Clock Rising Edge	2.7		ns
t_{IHD}	Hold Time to Input Clock Rising Edge	1		ns

NOTE:
1. Clocks – VD1_CLK/HD1_CLK, VD2_CLK, HD2_CLK, HD3_CLK
2. Data – VD1_DATA[7:0], VD2_DATA[7:0], HD2_DATA[15:0], HD3_DATA[15:0]
3. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

Video Outputs AC Timing

SYMBOL	PARAMETER	MIN (NOTE 3)	MAX (NOTE 3)	UNITS
BT.656/8 BITS MODE/PVX/PBX PORTS				
f_{OCK}	Video Output Clock Frequency	27	108	MHz
t_{OCK}	Video Output Clock Period	$1/f_{OCK}$(max)	$1/f_{OCK}$(min)	ns
t_{OSU}	Setup Time to Output Clock Rising Edge	1.5		ns
t_{OHD}	Hold Time to Output Clock Rising Edge	1.5		ns
BT.1120/16 BITS MODE/PBX PORTS				
f_{OCK}	Video Output Clock Frequency	74.25	74.25	MHz
t_{OCK}	Video Output Clock Period	$1/f_{OCK}$(max)	$1/f_{OCK}$(min)	ns
t_{OSU}	Setup Time to Output Clock Rising Edge	1.5		ns
t_{OHD}	Hold Time to Output Clock Rising Edge	1.5		ns

NOTE:
1. Clocks – PV1_CLK, PV2_CLK, PB1_CLK, PB2_CLK
2. Data – PV1_DATA[7:0], PV2_DATA[7:0], PB1_DATA[7:0], PB2_DATA[7:0]
3. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

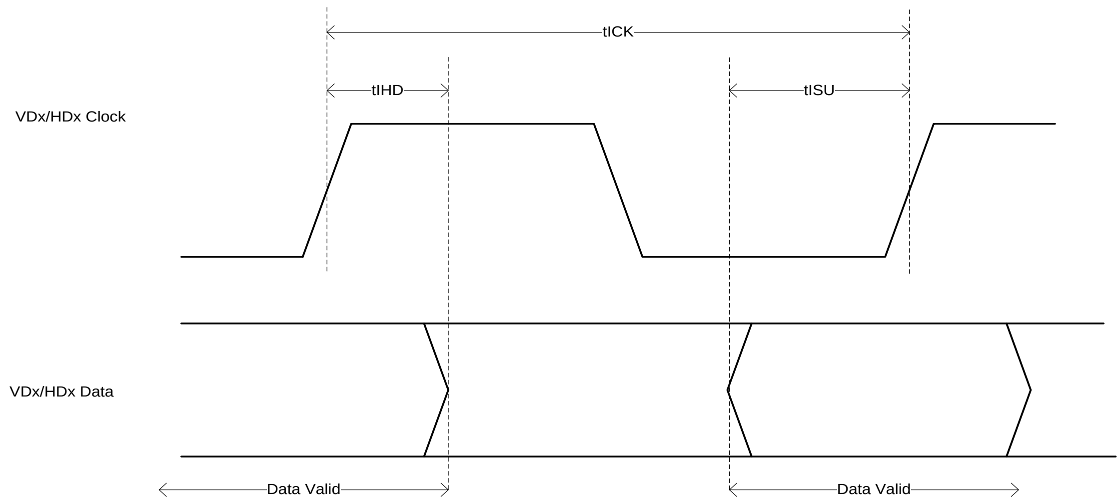


FIGURE 42. VIDEO INTERFACE INPUT TIMING

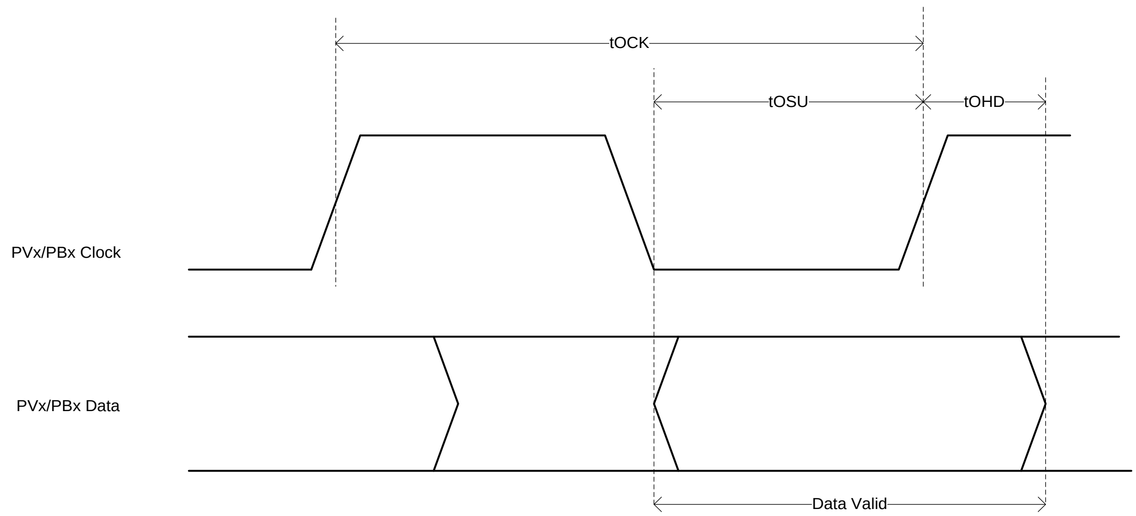


FIGURE 43. VIDEO INTERFACE OUTPUT TIMING

I²C Interface AC Timing

SYMBOL	PARAMETER	MIN (NOTE 1)	MAX (NOTE 1)	UNITS
t_{BF}	Bus Free Time Between STOP and START	1.3		µs
t_{S_SDAT}	SDAT Setup Time	100		
t_{H_SDAT}	SDAT Hold Time		0.9	
t_{S_STA}	Setup Time for START Condition	0.6		
t_{H_STA}	Hold Time for START Condition	0.6		
t_{S_STO}	Setup Time for STOP Condition	0.6		
t_R	Rising Time for SDAT and SCLK		300	
t_F	Falling Time for SDAT and SCLK		300	
C_{BUS}	Capacity Load for Each Bus Line		400	pF
F_{SCLK}	SCLK Clock Frequency		400	kHz

NOTE:

1. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

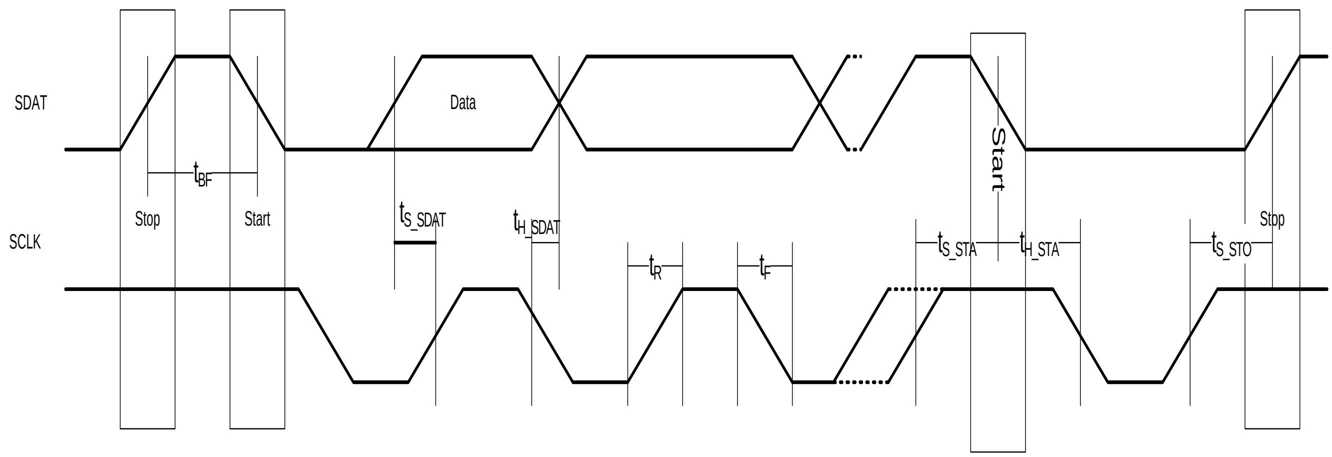


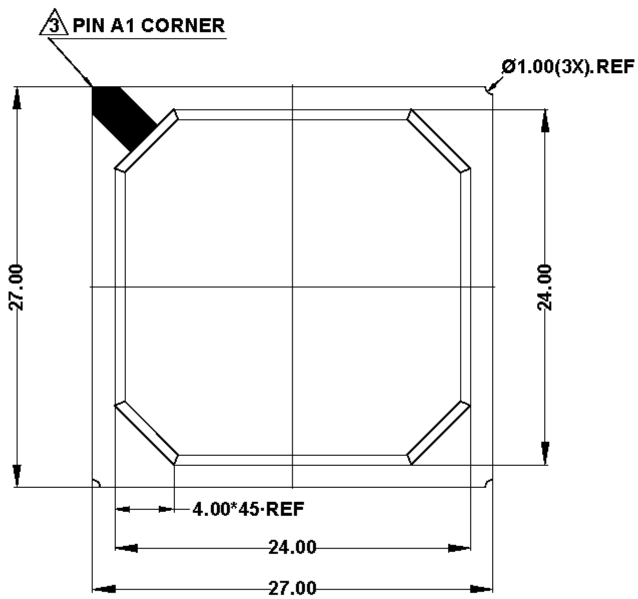
FIGURE 44. I2C INTERFACE TIMING CONDITION

Package Outline Drawing

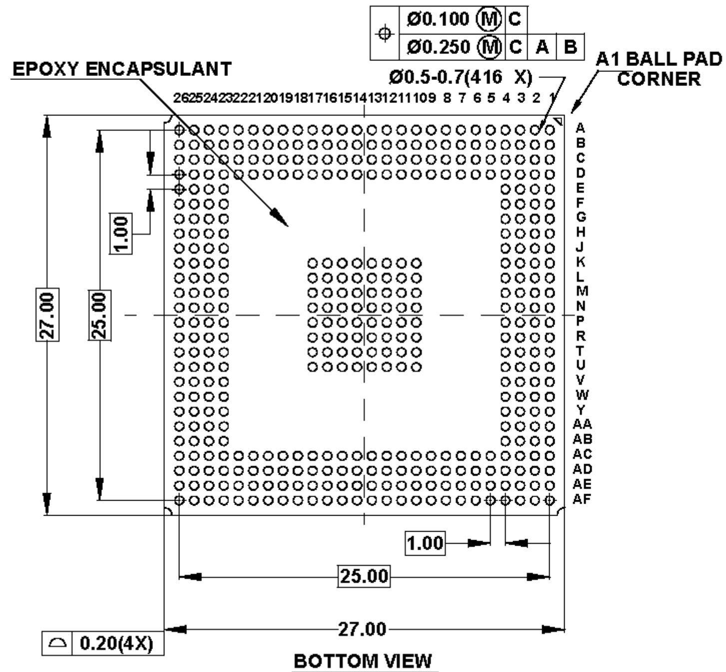
V416.27x27

416 PLASTIC BALL GRID ARRAY PACKAGE (CAVITY DOWN)

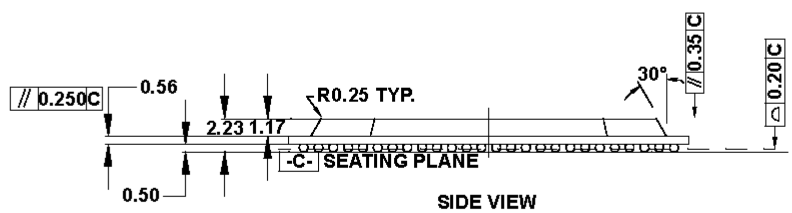
Rev 0, 9/11



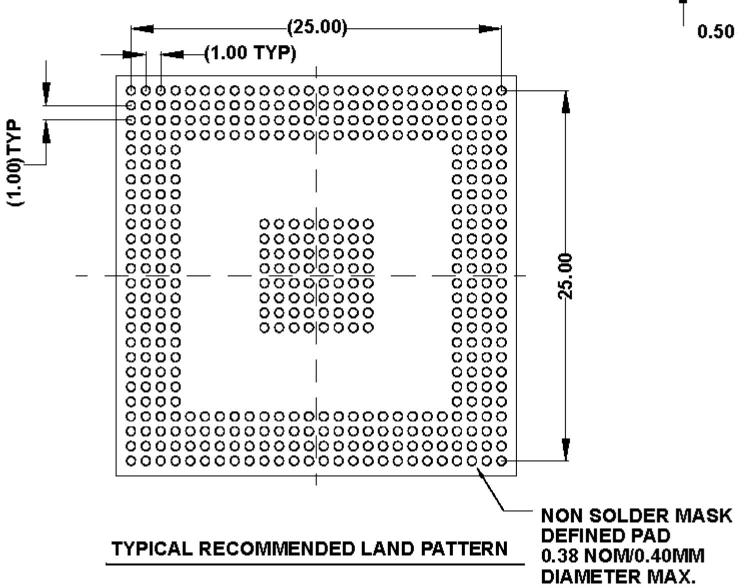
TOP VIEW



BOTTOM VIEW



SIDE VIEW



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. All dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Terminal positions designation per JESD 95-1, SPP-010.
3. Pin #1 identifier can be chamfer, ink mark or metallized mark but located within the zone indicated.
4. Reflow ball diameter.
5. Compliant to JEDEC registered outline MS-034, variation AAF-1.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

REVISION	DATE	CHANGES NOTE
FN8319.0	February 27, 2013	Initial Release.

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