











LMK04832

SNAS752 - AUGUST 2017

LMK04832 Ultra Low-Noise JESD204B Compliant Clock Jitter Cleaner With Dual Loop PLLs

1 Features

- Maximum Clock Output Frequency: 3250 MHz
- Multi-Mode: Dual PLL, Single PLL, and Clock Distribution
- Ultra-Low Noise, at 3200 MHz:
 - 47 fs RMS Jitter (12 kHz to 20 MHz)
 - 50 fs RMS Jitter (100 Hz to 100 MHz)
 - 158 dBc/Hz Noise Floor
- PLL2
 - PLL FOM of –230 dBc/Hz
 - PLL 1/f of –126 dBc/Hz
 - Phase Detector Rate up to 320 MHz
 - Two Integrated VCOs: 2495 to 2705 MHz and 2945 to 3205 MHz
- Up to 14 Differential Device Clocks
 - CML, LVPECL, LCPECL, HSDS, LVDS, and 2xLVCMOS Programmable Outputs
- Up to 1 Buffered VCXO/XO Output
 - LVPECL, LVDS, 2xLVCMOS Programmable
- Capable of 3.13-MHz Device Clock from 3.2 GHz
- Capable of 391-kHz SYSREF from 3.2 GHz
- 25-ps Step Analog Delay for SYSREF Clocks
- Digital Delay and Dynamic Digital Delay for Device Clock and SYSREF
- Holdover Mode with PLL1
- 0-Delay with PLL1 or PLL2
- +125°C Junction Temperature
- Supports 105°C PCB Temperature (Measured at Thermal Pad)

2 Applications

- Test and Measurement
- RADAR
- Microwave Backhaul
- Data Converter Clocking

3 Description

The LMK04832 is the industry's highest performance clock conditioner with JEDEC JESD204B support and is also pin compatible with the LMK0482x family of devices.

The 14 clock outputs from PLL2 can be configured to drive seven JESD204B converters or other logic devices using device and SYSREF clocks. SYSREF can be provided using both DC and AC coupling. Not limited to JESD204B applications, each of the 14 outputs can be individually configured as high performance outputs for traditional clocking systems.

The LMK04832 can be configured for operation in dual PLL, single PLL, or clock distribution modes with or without SYSREF generation or reclocking. PLL2 may operate with either internal or external VCO.

The high performance combined with features like the ability to trade off between power and performance, dual VCOs, dynamic digital delay, and holdover make the LMK04832 ideal for providing flexible high performance clocking trees.

Device Information(1)

PART NUMBER	DESCRIPTION	BODY SIZE (NOM)		
LMK04832NKDT LMK04832NKDR	WQFN (64)	9 mm x 9 mm		

- For all available packages, see the orderable addendum at the end of the data sheet.
- (2) T = Tape; R = Reel

Simplified Schematic

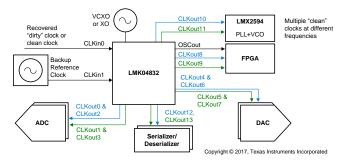






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4 Revision History

DATE	REVISION	NOTES
August 2017	*	Initial release.

ADVANCE INFORMATION



www.ti.com

5 Device and Documentation Support

5.1 Device Support

5.1.1 Development Support

5.1.1.1 Clock Architect

Part selection, loop filter design, simulation.

To run the online Clock Architect tool, go to www.ti.com/clockarchitect.

5.1.1.2 PLLatinum Sim

Supports loop filter design and simulation. All simulation is for a single loop, to perform dual loop simulations, the result of the first PLL sim must be loaded as a reference to the second PLL sim.

To download PLLatinum Sim tool, go to www.ti.com/tool/PLLATINUMSIM-SW

5.1.1.3 TICS Pro

EVM programming software. Can also be used to generate register map for programming and calculate current consumption estimate.

For TICS Pro, go to www.ti.com/tool/TICSPRO-SW

5.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community TI's Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

5.3 Trademarks

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

5.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

5.5 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

6 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This data is subject to change without notice and revision of this document.

Product Folder Links: LMK04832



PACKAGE OPTION ADDENDUM

19-Sep-2017

PACKAGING INFORMATION

Orderable Device	Status	Package Type	Package	Pins	Package	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking	Samples
	(1)		Drawing		Qty	(2)	(6)	(3)		(4/5)	
PLMK04832NKDT	ACTIVE	WQFN	NKD	64	250	TBD	Call TI	Call TI	-40 to 85		Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (CI) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

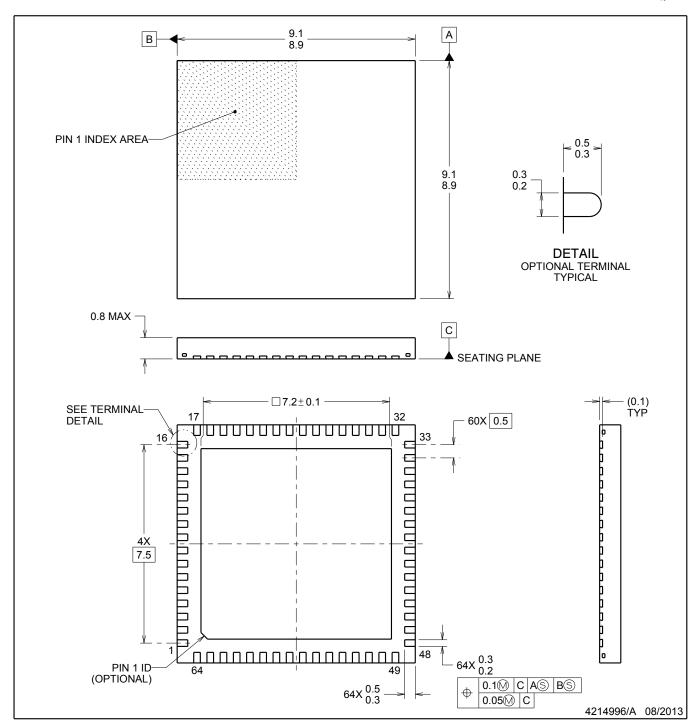
- (3) MSL, Peak Temp. The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead/Ball Finish Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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WQFN

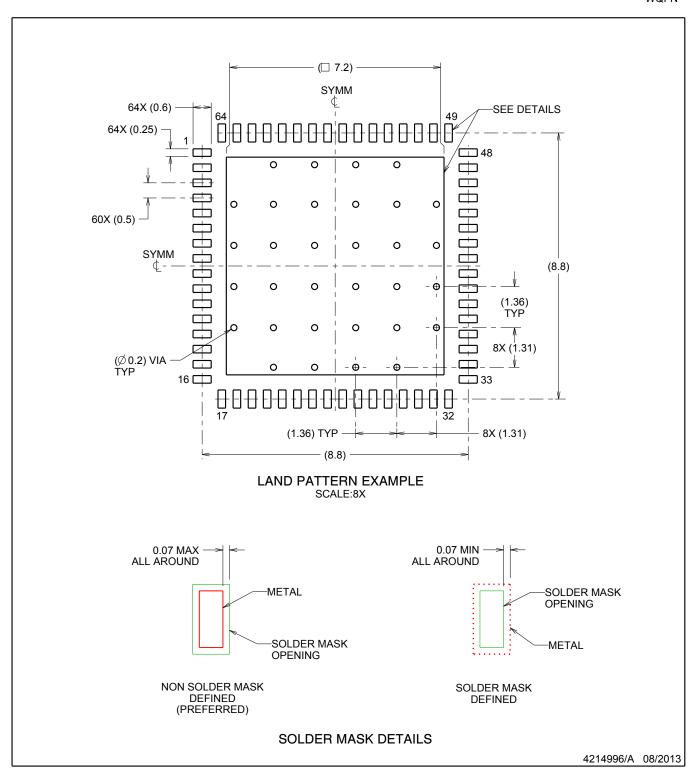


NOTES:

- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



WQFN

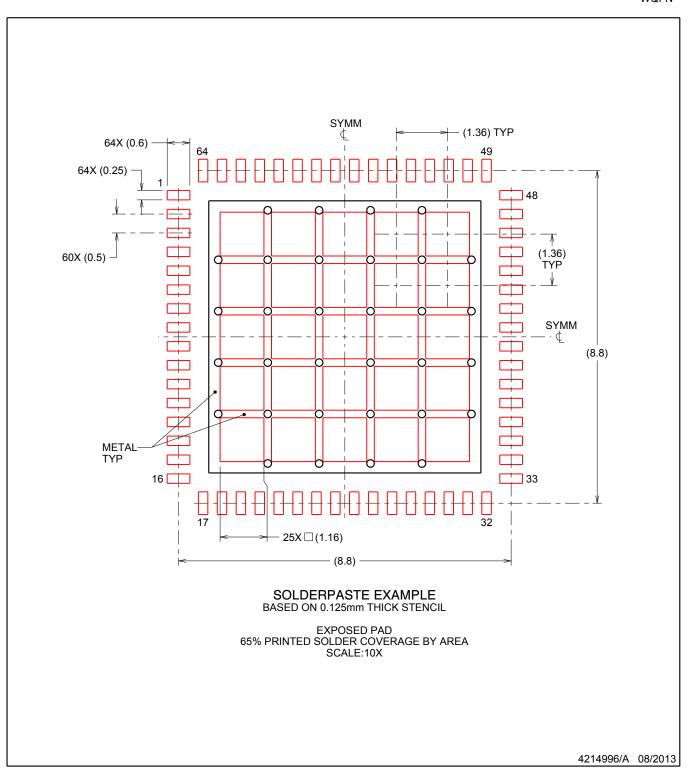


NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 (www.ti.com/lit/slua271).



WQFN



NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



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