

DMN4026SSDQ-13-VB Datasheet

Dual N-Channel 40-V (D-S) MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A) ^a	Q_g (Typ.)
40	0.010 at $V_{GS} = 10$ V	12	5.9 nC
	0.015 at $V_{GS} = 4.5$ V	10	

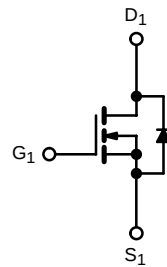
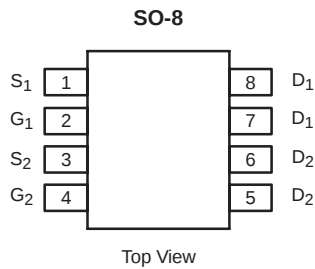
FEATURES

- Halogen-free
- Trench Power MOSFET
- Optimized for High-Side Synchronous Rectifier Operation
- 100 % R_g Tested
- 100 % UIS Tested

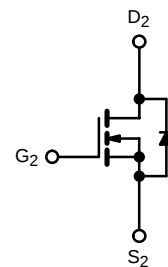

RoHS
 COMPLIANT

APPLICATIONS

- Notebook CPU Core
- High-Side Switch



N-Channel MOSFET



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS $T_A = 25^\circ\text{C}$, unless otherwise noted

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	40	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ($T_J = 150^\circ\text{C}$)	$T_C = 25^\circ\text{C}$	12	A
	$T_C = 70^\circ\text{C}$	10	
	$T_A = 25^\circ\text{C}$	10 ^{b, c}	
	$T_A = 70^\circ\text{C}$	8 ^{b, c}	
Pulsed Drain Current	I_{DM}	45	A
Continuous Source-Drain Diode Current	$T_C = 25^\circ\text{C}$	3.2	
	$T_A = 25^\circ\text{C}$	1.6 ^{b, c}	
Single Pulse Avalanche Current	I_{AS}	17	mJ
Avalanche Energy	E_{AS}	21	
Maximum Power Dissipation	$T_C = 25^\circ\text{C}$	4.1	W
	$T_C = 70^\circ\text{C}$	2.5	
	$T_A = 25^\circ\text{C}$	2.1 ^{b, c}	
	$T_A = 70^\circ\text{C}$	1.2 ^{b, c}	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{b, d}	R_{thJA}	39	53	$^\circ\text{C/W}$
Maximum Junction-to-Foot (Drain)	R_{thJF}	25	29	

Notes:

 a. Base on $T_C = 25^\circ\text{C}$.

b. Surface Mounted on 1" x 1" FR4 board.

 c. $t = 10$ s.

 d. Maximum under Steady State conditions is 85°C/W .

SPECIFICATIONS $T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted							
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$	40			V	
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$		28		mV/ $^{\circ}\text{C}$	
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			- 6			
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	1.2		2.5	V	
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 20\text{ V}$			± 100	nA	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 40\text{ V}$, $V_{GS} = 0\text{ V}$			1	μA	
		$V_{DS} = 40\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 55\text{ }^{\circ}\text{C}$			10		
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}$, $V_{GS} = 10\text{ V}$	20			A	
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$, $I_D = 10\text{ A}$		0.010		Ω	
		$V_{GS} = 4.5\text{ V}$, $I_D = 9\text{ A}$		0.015			
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15\text{ V}$, $I_D = 10\text{ A}$		52		S	
Dynamic ^b							
Input Capacitance	C_{iss}	$V_{DS} = 15\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$		641		pF	
Output Capacitance	C_{oss}			175			
Reverse Transfer Capacitance	C_{rss}			73			
Total Gate Charge	Q_g	$V_{DS} = 15\text{ V}$, $V_{GS} = 10\text{ V}$, $I_D = 10\text{ A}$		15	23	nC	
Gate-Source Charge	Q_{gs}	$V_{DS} = 15\text{ V}$, $V_{GS} = 5\text{ V}$, $I_D = 10\text{ A}$		5.9	10.2		
Gate-Drain Charge	Q_{gd}			2.5			
Gate Resistance	R_g			2.3			
Turn-On Delay Time	$t_{d(on)}$	$f = 1\text{ MHz}$	0.36	1.8	3.6	Ω	
Rise Time	t_r		$V_{DD} = 15\text{ V}$, $R_L = 1.4\text{ }\Omega$ $I_D \cong 9\text{ A}$, $V_{GEN} = 4.5\text{ V}$, $R_g = 1\text{ }\Omega$		16	24	ns
Turn-Off Delay Time	$t_{d(off)}$				12	18	
Fall Time	t_f				16	24	
Turn-On Delay Time	$t_{d(on)}$			10	20		
Rise Time	t_r	$V_{DD} = 15\text{ V}$, $R_L = 1.4\text{ }\Omega$ $I_D \cong 9\text{ A}$, $V_{GEN} = 10\text{ V}$, $R_g = 1\text{ }\Omega$		8	16		
Turn-Off Delay Time	$t_{d(off)}$			10	20		
Fall Time	t_f			16	24		
				8	15		
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^{\circ}\text{C}$			17	A	
Pulse Diode Forward Current ^a	I_{SM}				45		
Body Diode Voltage	V_{SD}	$I_S = 9\text{ A}$		0.8	1.2	V	
Body Diode Reverse Recovery Time	t_{rr}	$I_F = 9\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $T_J = 25\text{ }^{\circ}\text{C}$		15	30	ns	
Body Diode Reverse Recovery Charge	Q_{rr}			6	12	nC	
Reverse Recovery Fall Time	t_a			8		ns	
Reverse Recovery Rise Time	t_b			7			

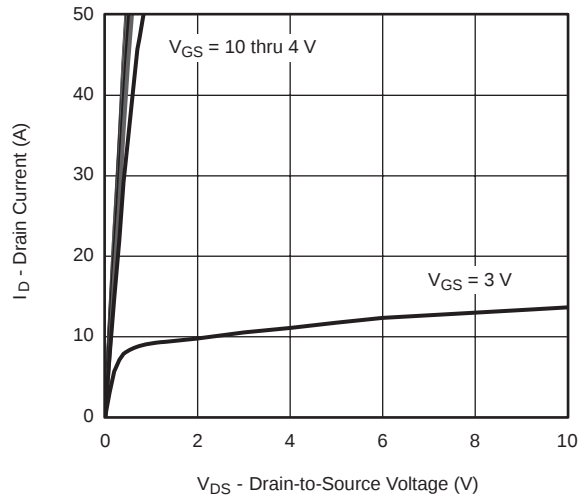
Notes:

a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

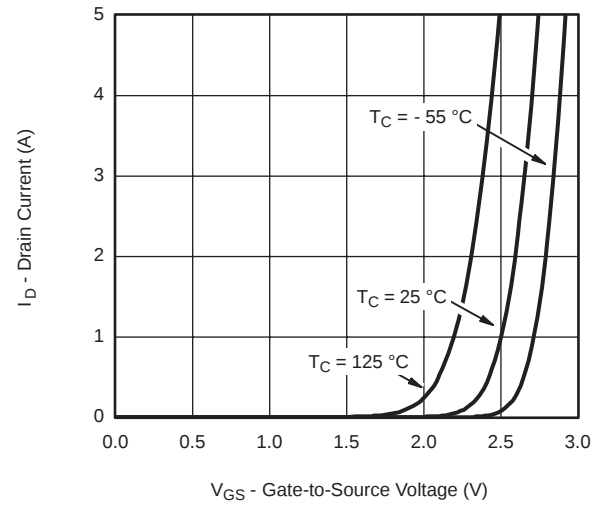
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

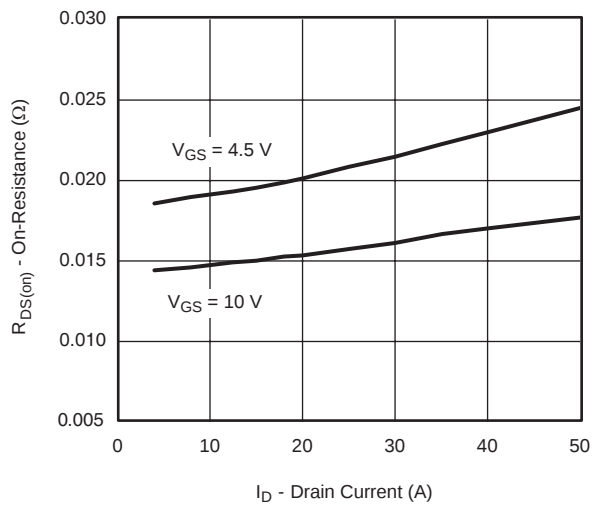
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



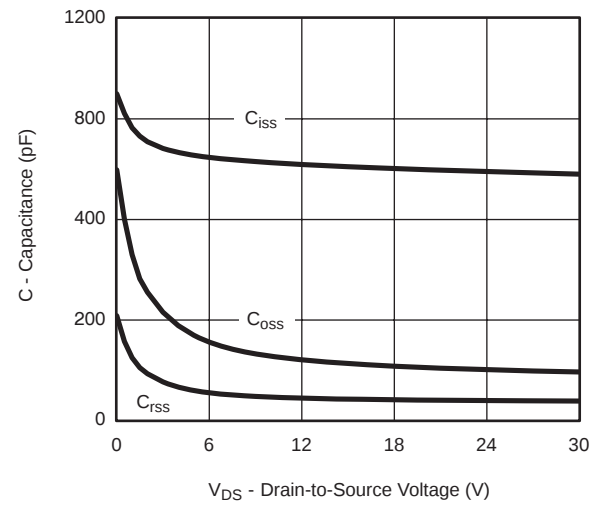
Output Characteristics



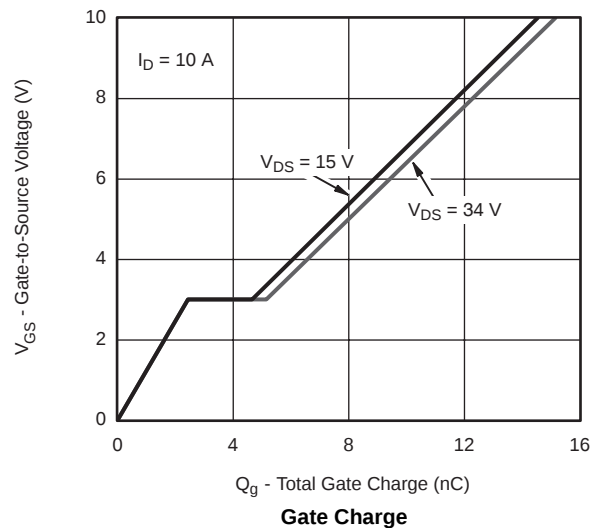
Transfer Characteristics



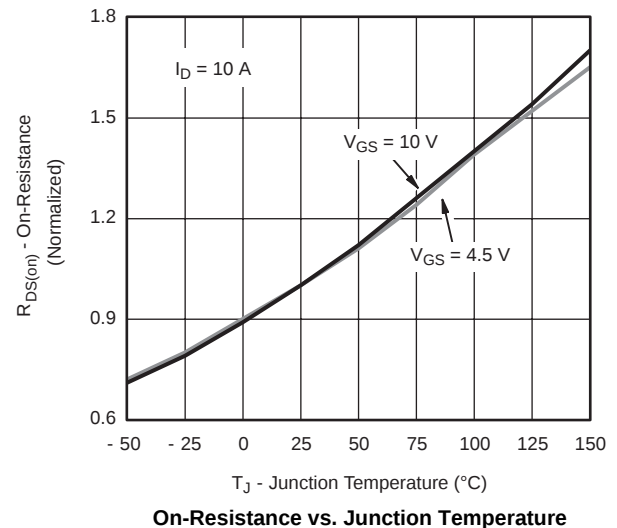
On-Resistance vs. Drain Current and Gate Voltage



Capacitance

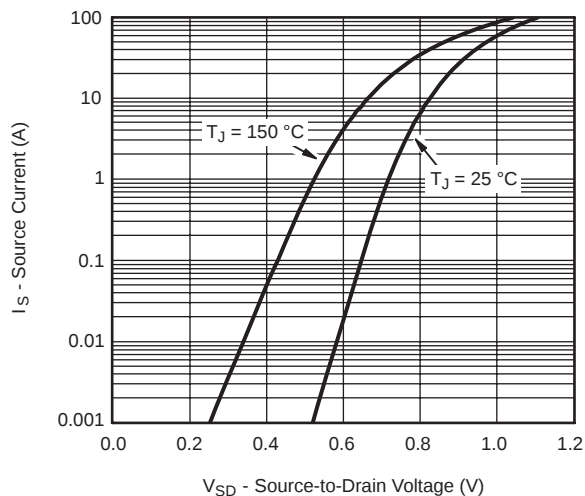


Gate Charge

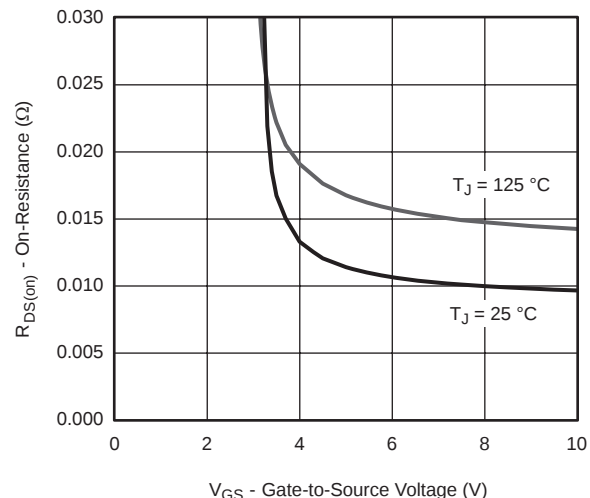


On-Resistance vs. Junction Temperature

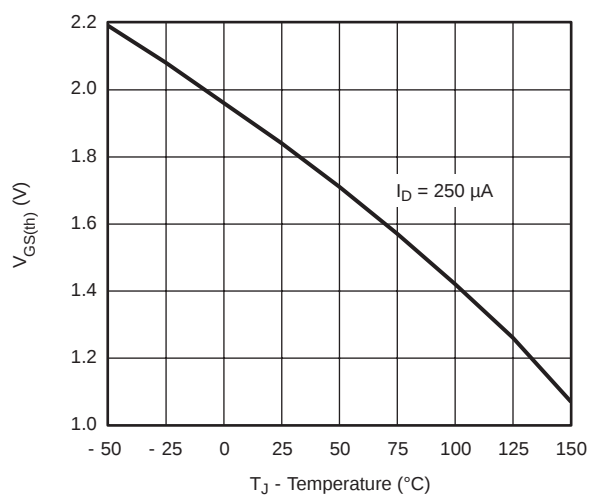
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



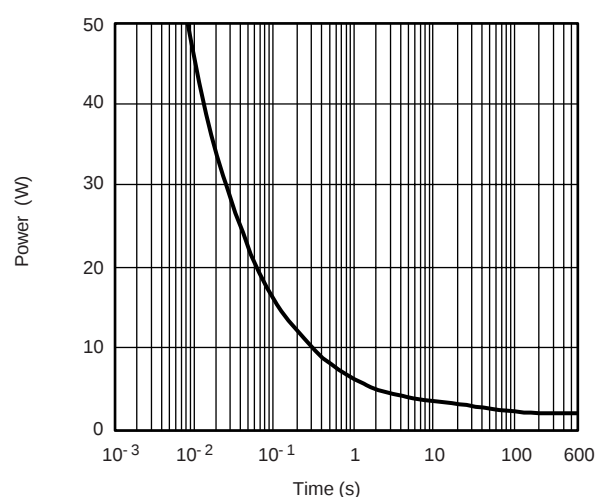
Source-Drain Diode Forward Voltage



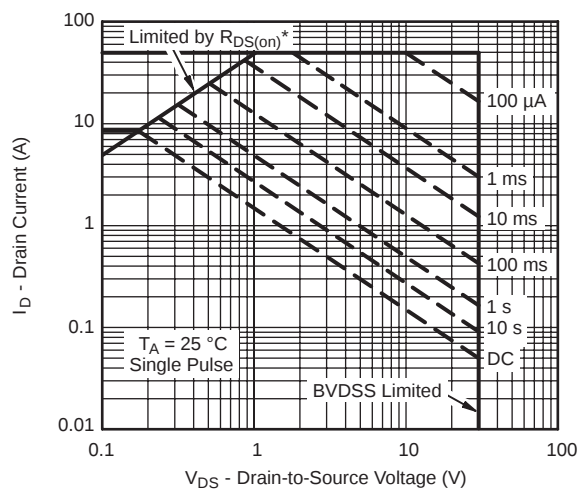
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

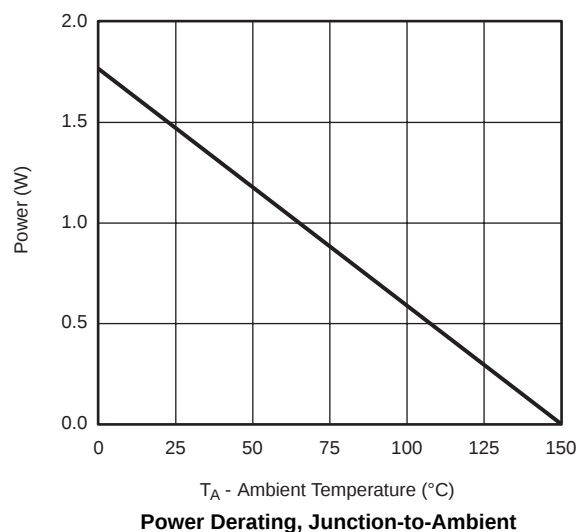
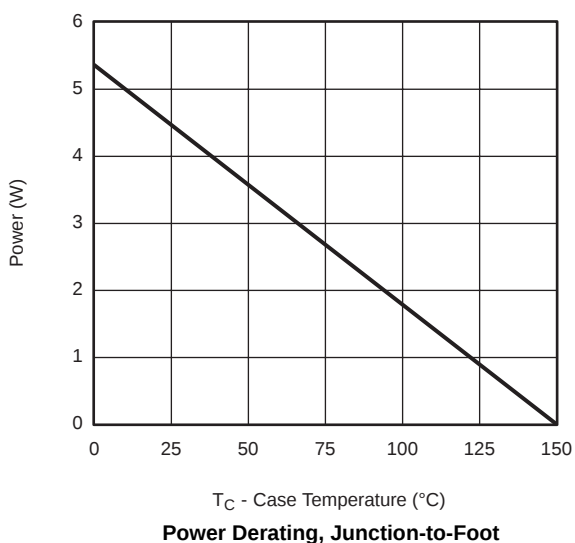
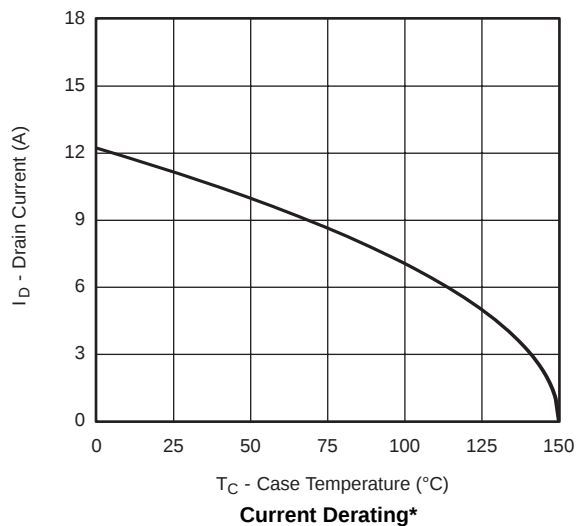


Single Pulse Power, Junction-to-Ambient



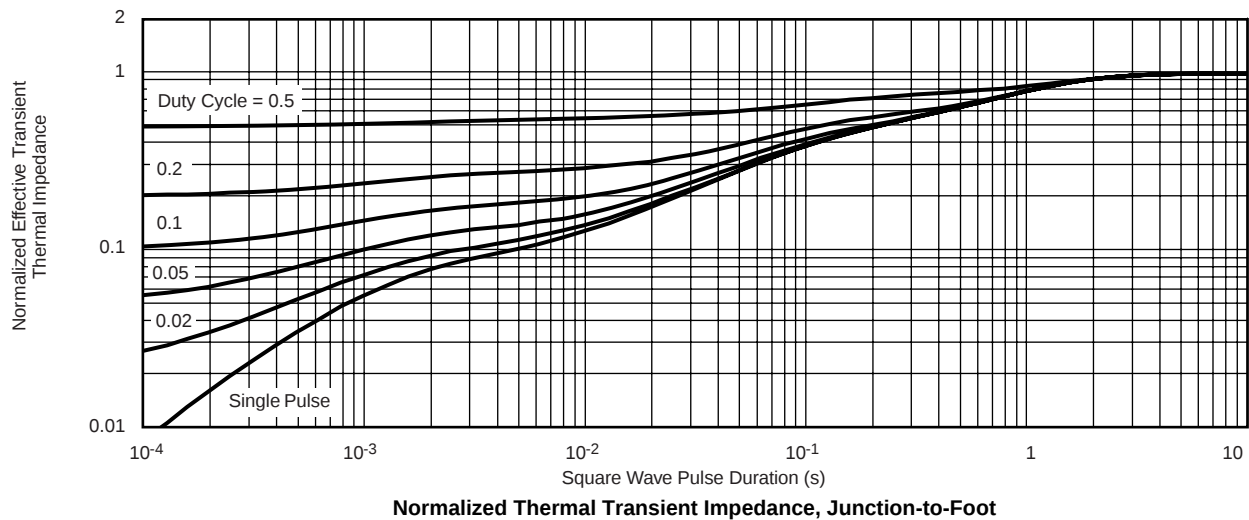
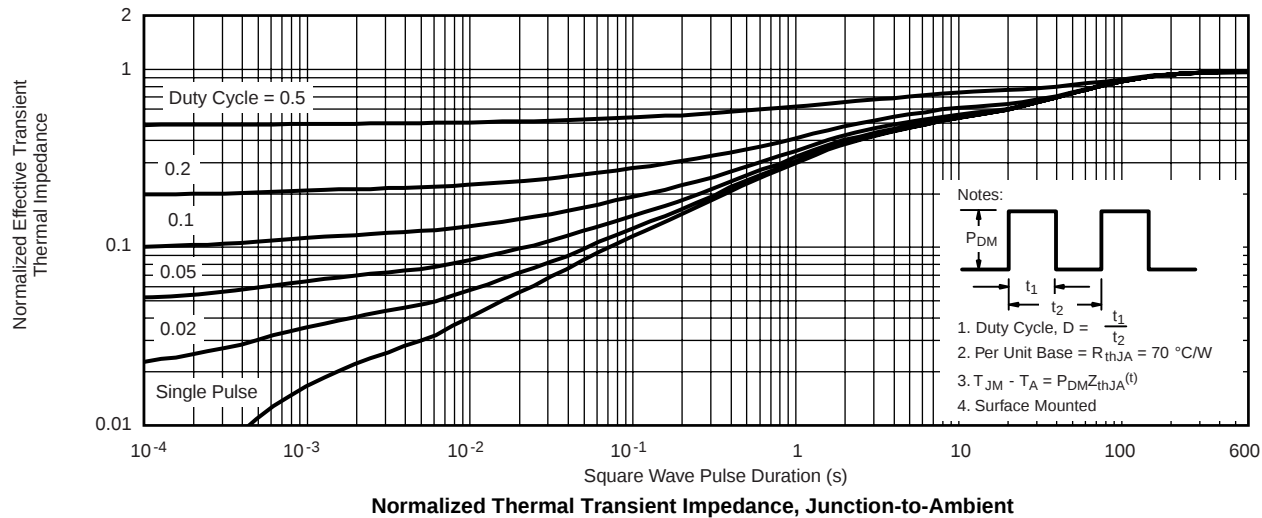
* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted


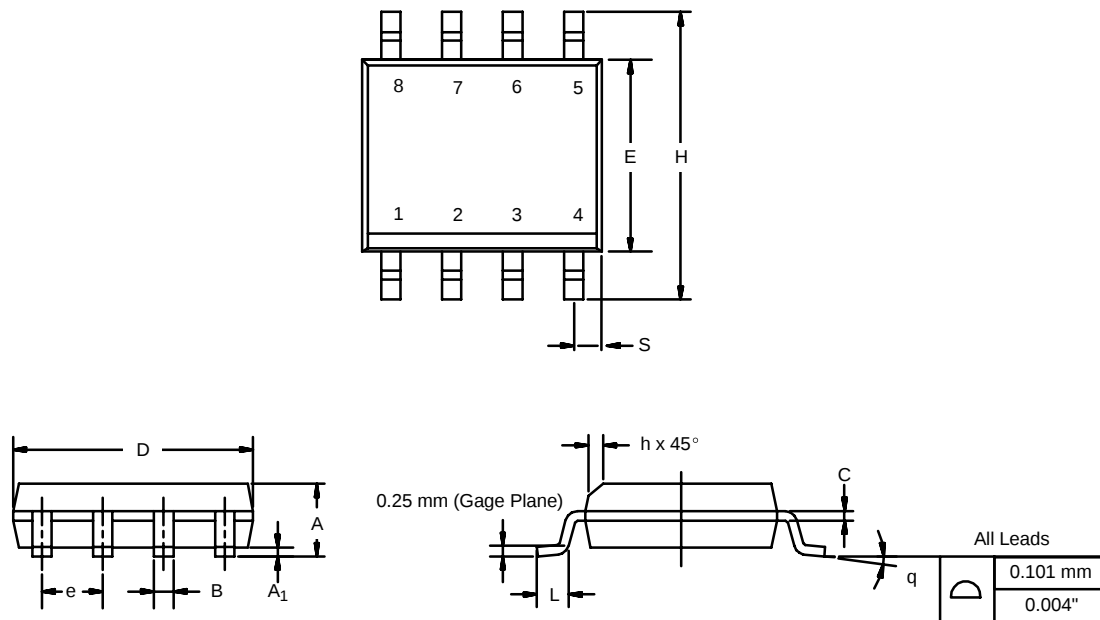
* The power dissipation P_D is based on $T_{J(max)} = 150\text{ °C}$, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



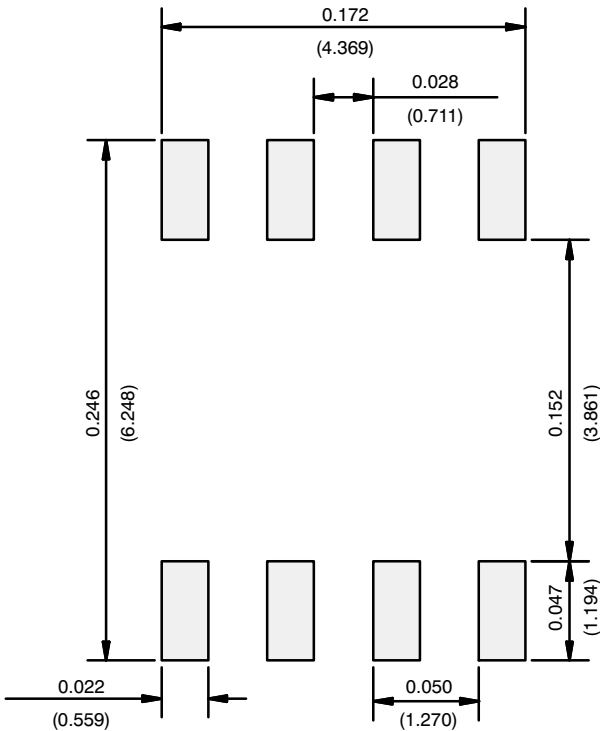
SOIC (NARROW): 8-LEAD

JEDEC Part Number: MS-012



DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A ₁	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026
ECN: C-06527-Rev. I, 11-Sep-06				
DWG: 5498				

RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads
Dimensions in Inches/(mm)

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