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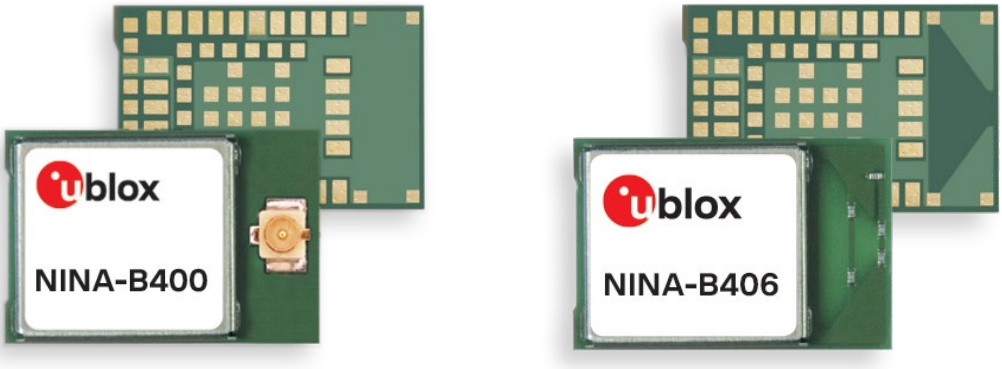
NINA-B4 series

Stand-alone Bluetooth 5.1 low energy modules

Data Sheet



Abstract

This technical data sheet describes the stand-alone NINA-B4 series Bluetooth® 5.1 low energy modules. The NINA-B4 series includes two sub-series – the NINA-B40 and NINA-B41 series. The NINA-B40 series provides an open CPU architecture with a powerful MCU for customer applications, while the NINA-B41 series are delivered with u-connectXpress software pre-flashed.

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Initial Production	Early Production Information	Data from product verification. Revised and supplementary data may be published later.
Mass Production / End of Life	Production Information	Document contains the final product specification.

This document applies to the following products:

Product name	Type number	Software	Hardware version	PCN reference	Product status
NINA-B400	NINA-B400-00B-00	Open CPU	01	N/A	Prototype
NINA-B406	NINA-B406-00B-00	Open CPU	01	N/A	Prototype
NINA-B410	NINA-B410-00B-00	u-connectXpress	01	N/A	In Development
NINA-B416	NINA-B416-00B-00	u-connectXpress	01	N/A	In Development

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1 Functional description

1.1 Overview

The NINA-B4 series are small stand-alone Bluetooth low energy (LE) modules with Bluetooth 5.1 functionality. They are based on the Nordic Semiconductor nRF52833 chip, which has an integrated RF core and powerful Arm® Cortex®-M4 with FPU processor. Only the NINA-B40 modules can operate in all Bluetooth 5.1 modes as well as 802.15.4 (Thread and Zigbee) and Nordic proprietary modes.

Direction Finding feature (AoA/AoD) is supported. The module needs only a single supply voltage that can range from 1.7 – 3.6 V. The supply voltage level is also used as the I/O reference level, so that the module can be easily implemented in a simple, single voltage rail system, and the broad supply voltage range makes it useful in battery powered systems.

The mechanical design of NINA-B4 has the same size and pinout as the NINA-B3 module, see [6].

The summary of the product can be seen in the NINA-B4 Product Summary, see [5].

The NINA-B4 series includes the following two sub-series, as listed in the table below:

Model	Description
NINA-B40 series	Bluetooth 5.1 module with a powerful Arm® Cortex®-M4 with FPU, and state-of-the-art power performance. All the variants of NINA-B40 are open CPU modules that enable customer applications to run on the built-in Arm® Cortex®-M4 with FPU. With 512 kB flash and 128 kB RAM, they offer sufficient capacity for customer applications on top of the Bluetooth low energy stack. NINA-B400 has an U.FL connector for use with an external antenna and NINA-B406 has an internal PCB antenna integrated in the module PCB. The internal antennas are specifically designed for embedded devices and provide an extensive range.
NINA-B41 series	Bluetooth 5.1 module with a powerful Arm® Cortex®-M4 with FPU and u-connect software pre-flashed. The u-connect software in NINA-B41 modules provides support for u-blox Bluetooth low energy Serial Port Service, GATT client and server, beacons, NFC™, and simultaneous peripheral and central roles – all configurable from a host using AT commands. NINA-B410 has an U.FL connector for use with an external antenna and NINA-B416 has an internal PCB antenna integrated in the module PCB. The internal antennas are specifically designed for embedded devices and provide an extensive range.

Table 1: NINA-B4 series

The NINA-B4 series modules are globally certified for use with the internal antenna or a range of external antennas. This greatly reduces time, cost, and effort for customers integrating these modules in their designs.

1.2 Applications

- Industrial automation
- Smart buildings and cities
- Low power sensors
- Wireless-connected and configurable equipment
- Point-of-sales
- Health devices
- Real-time Location, RTLS
- Indoor positioning
- Asset tracking

1.3 Block diagram

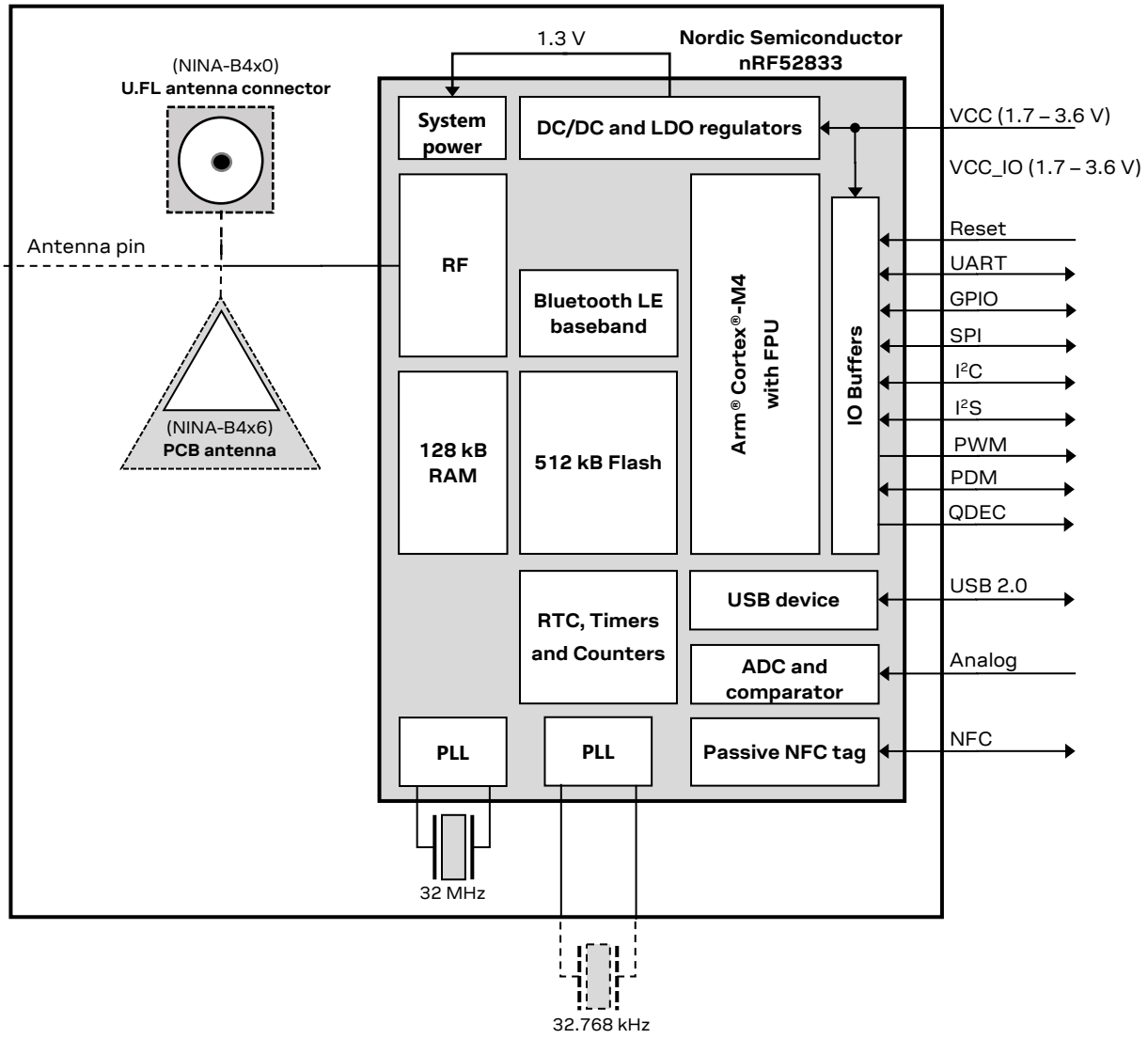


Figure 1: Block diagram of NINA-B4 series

1.3.1 NINA-B4x0

The NINA-B4x0 modules do not include an internal antenna, but have an U.FL connector to allow for an external antenna where the RF signal is available. The module size is 10 x 15 x 1.9 mm.

1.3.2 NINA-B4x6

The NINA-B4x6 modules include an internal PCB antenna integrated in the module PCB, using antenna technology from Proant AB. The RF signal pin is not connected to any signal path. The module size is 10 x 15 x 1.9 mm.

1.4 Product description

Item	NINA-B4x0	NINA-B4x6
Bluetooth version	5.1	5.1
Band support	2.4 GHz, 40 channels	2.4 GHz, 40 channels
Typical conducted output power	+8 dBm	+8 dBm
Radiated output power (EIRP)	+10 dBm (with approved antennas)	+10 dBm
RX sensitivity (conducted)	-95 dBm	-95 dBm
RX sensitivity, long range mode (conducted)	-103 dBm	-103 dBm
Supported 2.4 GHz radio modes	Bluetooth low energy IEEE 802.15.4 Proprietary 2.4 GHz modes	Bluetooth low energy IEEE 802.15.4 Proprietary 2.4 GHz modes
Supported Bluetooth LE data rates	1 Mbps 2 Mbps 500 kbps 125 kbps	1 Mbps 2 Mbps 500 kbps 125 kbps
Module size	10.0 x 15.0mm	10.0 x 15.0 mm

Table 2: NINA-B4 series characteristics summary

1.5 Hardware options

Except for the different antenna solutions, the NINA-B4 series modules use an identical hardware configuration. The integrated DC/DC converter is available for higher efficiency under heavy load situations (see section 2.1.1 for more information).

1.6 Software options

The integrated application processor of the NINA-B4 module is an Arm® Cortex®-M4 with FPU that has 512 kB flash memory and 128 kB RAM. The software structure of any program running on the module can be broken down into the following components:

- Radio stack
- Bootloader (optional)
- Application

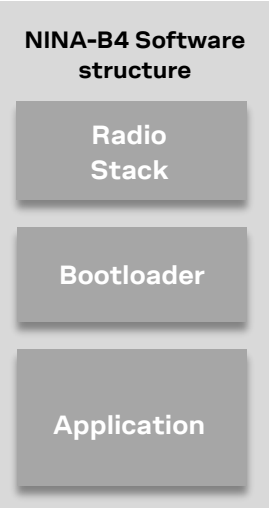


Figure 2: NINA-B4 software structure

Table 3 describes the different software options available.

Software
u-connectXpress
Open CPU, Nordic Semiconductors software preferred

Table 3: NINA-B4 series software options summary

1.6.1 u-connectXpress software

The NINA-B41x-0xB modules are pre-flashed with u-connectXpress software, and are delivered with u-blox secure boot loader.

The u-connectXpress software enables use of the Bluetooth low energy functions, controlled by AT commands over the UART interface. Examples of supported features are u-blox Low Energy Serial Port Service, GATT server and client, central and peripheral roles, and multi-drop connections. The NINA-B41 modules can be configured using the u-blox s-center evaluation software, which can be downloaded from the u-blox website and is available free of charge.

Much more information on the features and capabilities of the u-connectXpress software and how to use it can be found in the u-blox Short Range AT Commands Manual [2] and the u-connectXpress software User guide [4].

1.6.2 Open CPU

The open CPU architecture in the NINA-B40 series modules allows module integrators to build their own applications. u-blox recommends the following development approach to speed up the process:

1.6.2.1 Nordic software

The Nordic Semiconductor's software provides a rich and well-tested software development environment for nRF52 based devices. It includes a broad selection of drivers, libraries, and example applications. It also includes other radio stacks.

1.7 Bluetooth device address

Each NINA-B41 module is pre-programmed with a unique 48-bit Bluetooth device address. For NINA-B40 series modules, or if the memory of a NINA-B41 module is corrupted or otherwise lost, the address can be recovered from the data matrix barcode printed on the module label.

2 Interfaces

2.1 Power management

2.1.1 Module supply input (VCC)

The NINA-B4 series uses integrated step-down converters to transform the supply voltage presented at the **VCC** pin into a stable system voltage. Because of this, the NINA-B4 modules are compatible for use in battery powered designs without the use of an additional voltage converter. You can choose one of the following two on-board voltage converter options:

- A low-dropout (LDO) converter
- A DC/DC buck converter

Normally, the module will automatically switch between these options depending on the current consumption of the module. Under high loads such as when the radio is active, the DC/DC converter is more efficient, while the LDO converter is more efficient in the power saving modes.

2.1.2 Digital I/O interfaces reference voltage (VCC_IO)

All modules in the u-blox NINA series provide an additional voltage supply input for setting the I/O voltage level. In NINA-B4 series modules, the I/O voltage level is similar to the supply voltage and **VCC_IO** is internally connected to the supply input. Therefore, only a single supply voltage is needed for NINA-B4, which makes it ideal for battery powered designs.

☞ This may not be the case for other modules in the NINA series. A design that should be pin compatible with other NINA-series modules should keep the **VCC** and **VCC_IO** supply rails separate.

2.2 RF antenna interfaces

2.2.1 2.4 GHz radio (ANT)

The NINA-B4 model versions have their own 2.4 GHz antenna solutions respectively:

- The NINA-B4x0 modules use an U.FL connector solution for external antenna. The **ANT** pin is internally disconnected on these models.
- The NINA-B4x6 modules use an internal PCB antenna integrated into the module PCB. This low profile antenna solution is useful in space constrained designs. The **ANT** pin is internally disconnected on these models. This solution uses antenna technology licensed from Proant AB.

☞ See the NINA-B4 System Integration Manual [3] for Antenna reference designs and integration instructions.

2.2.2 Near Field Communication (NFC)

The NINA-B4 series modules include a Near Field Communication interface, capable of operating as a 13.56 MHz NFC tag at a bit rate of 106 kbps. As an NFC tag, the data can be read from or written to the NINA-B4 modules using an NFC reader; however, the NINA-B4 modules are not capable of reading other tags or initiating NFC communications. The NFC interface can be used to wake the module from sleep mode, meaning that the module can be kept in the deepest power save mode and wake up and properly react to an NFC field.

Two pins are available for connecting to an external NFC antenna: **NFC1** and **NFC2**.

2.2.3 Direction Finding (AoA/AoD)

The NINA-B4 has support for a location service called Bluetooth Direction Finding feature which is part of the Bluetooth 5.1 specification. It can be used to for example track assets, for indoor positioning and wayfinding. These phase-based functions require an antenna array, estimation algorithms and processing power to make it possible to triangulate and detect the direction of a Bluetooth signal down to a sub-meter accuracy. It's available for 1 Mbps and 2 Mbps Bluetooth LE modes. The Angle of Arrival, AoA, receiver and Angel of Departure, AoD, transmitter are using the antenna arrays, switched on one by one, to be able to calculate the direction of a peer device. The received IQ samples are used to determine the relative path lengths between the antenna pairs, thus the location of the transmitter is found.

2.3 System functions

2.3.1 Module power-on

You can switch on or reboot the NINA-B4 modules in one of the following ways:

- Rising edge on the VCC pin to a valid supply voltage
- Issuing a reset of the module (see section 2.3.4)

An event to wake up from the sleep mode to the active mode can be triggered by:

- Programmable digital or analog sensor event, e.g, rising voltage level on an analog comparator pin
- Detecting an NFC field
- Supplying 5 V to the **VBUS** pin (plugging in the USB interface)

While waking up from the standby mode to active mode, an event can also be triggered by:

- The on-board Real Time Counter (RTC)
- The radio interface
- Detection of an NFC field

2.3.2 Module power off

There is no dedicated pin to power off the NINA-B4 modules. You can configure any GPIO pin to enter or exit the sleep mode (see section 2.3.3.2), which essentially powers down the module.

An under-voltage (brown-out) shutdown occurs on the NINA-B4 modules when the **VCC** supply drops below the operating range minimum limit. If this occurs, it is not possible to store the current parameter settings in the module's non-volatile memory.

2.3.3 Power modes

The NINA-B4 series modules are power efficient devices capable of operating in different power saving modes and configurations. Different sections of the module can be powered off when not needed and complex wake-up events can be generated from different external and internal inputs. The radio part of the module operates independently from the CPU. The three main power modes are:

- Active
- Standby
- Sleep

Depending on the application, the module should spend most of its time in either standby or sleep mode to minimize current consumption.

2.3.3.1 Standby mode

Standby mode is one of the power saving modes in NINA-B4 modules that essentially powers down the module but keeps the system RAM and configurations intact. It also allows for complex, autonomous power-up events including periodic RTC events and radio events.

The following events can be used to bring the module out of the standby mode:

- Internal wake-up events from the RTC, radio, NFC and so on.
- Analog or digital sensor events (programmable voltage level or edge detection)

During standby mode, the module is clocked at 32.768 kHz, which is generated by an internal RC-oscillator.

2.3.3.2 Sleep mode

Sleep mode is the deepest power saving mode of NINA-B4 modules. During sleep mode, all functionality is stopped to ensure minimum power consumption. The module needs an external event in order to wake up from the sleep mode. The module will always reboot after waking up from the sleep mode; however, different sections of the RAM can be configured to remain intact during and after going to the sleep mode.

The following events can be used to wake up the module out of the sleep mode:

- External event on a digital pin
- External analog event on a low power comparator pin
- Detection of an NFC field

When using the u-connectXpress software, the module can be manually switched on or off with proper storage of the current settings using the UART **DSR** pin.

The module can be programmed to latch the digital values present at its GPIO pins during sleep. The module will keep the values latched, and a change of state on any of these pins will trigger a wake-up to active mode.

2.3.4 Module reset

The NINA-B4 modules can be reset using one of the following ways:

- Low level on the **RESET_N** input pin, normally kept high using an internal pull-up. This causes an “external” or “hardware” reset of the module. The current parameter settings are not saved in the module’s non-volatile memory and a proper network detach is not performed.
- With the NINA-B41 modules, using the AT+CPWROFF command. This causes an “internal” or “software” reset of the module. The current parameter settings are saved in the module’s non-volatile memory.

2.3.5 CPU and memory

The Nordic Semiconductor nRF52833 chip in the NINA-B4 series modules includes a powerful Arm® Cortex®-M4 with FPU processor. The processor works with a superset of 16 and 32-bit instructions (Thumb-2) at 64 MHz clock speed. It can use up to 37 interrupt vectors and 3 priority bits.

The nRF52833 chip has 512 MB of flash and 128 KB of RAM for code and data storage.

2.3.6 Direct Memory Access

All interfaces described in this data sheet support Direct Memory Access (DMA) to move any data generated from the interface directly into the RAM, without involving the CPU. This ensures fluent operation of the CPU with minimal need for interruption. To reduce the overall power consumption, DMA should be used as often as possible.

2.3.7 Programmable Peripheral Interconnect

The Nordic Semiconductor nRF52833 chip in the NINA-B4 series modules includes a programmable peripheral interconnect (PPI), which is a switch matrix that connects various control signals between different interfaces and system functions. This allows most interfaces to bypass the CPU in order to trigger a system function, that is, an incoming data packet may trigger a counter or a falling voltage level on an ADC, might toggle a GPIO, all without having to send an interrupt to the CPU. This enables smart applications that are extremely power efficient that wake up the CPU only when it is needed.

2.3.8 Real Time Counter (RTC)

A key system feature available on the module is the Real Time Counter. This counter can generate multiple interrupts and events to the CPU and radio as well as internal and external hardware blocks. These events can be precisely timed ranging from microseconds up to hours, and allows for periodic Bluetooth LE advertising events etc., without involving the CPU. The RTC can be operated in the active and standby modes.

2.4 Serial interfaces

NINA-B4 modules provide the following serial communication interfaces:

- 2x UART interfaces: 4-wire universal asynchronous receiver/transmitter
- 4x SPI interfaces: Up to four serial peripheral interfaces can be used simultaneously
- 2x I^2C interfaces: Inter-Integrated Circuit (I^2C) interface for communication with digital sensors
- 1x I^2S interface: Used to communicate with external audio devices
- 1x USB 2.0 device interface: The USB device interface to connect to the upstream host.

☞ Most digital interface pins on the module are shared between the digital, analog interfaces and GPIOs. Unless otherwise stated, all functions can be assigned to any pin that is not already occupied.

☞ Two of the SPI interfaces share common hardware with the I^2C interfaces and they cannot be used simultaneously. That is, if both the I^2C interfaces are in use then only one SPI interface will be available.

2.4.1 Universal Asynchronous Receiver/Transmitter (UART)

The 4-wire UART interface supports hardware flow control and baud rates up to 1 Mbps. Other characteristics of the UART interface are listed below:

- Pin configuration:
  - TXD, data output pin
  - RXD, data input pin
  - RTS, Request To Send, flow control output pin (optional)
  - CTS, Clear To Send, flow control input pin (optional)
- Hardware flow control or no flow control is supported.
- Power saving indication available on the hardware flow control output (**RTS** pin): The line is driven to the OFF state when the module is not ready to accept data signals.
- Programmable baud rate generator allows most industry standard rates, as well as non-standard rates up to 1 Mbps.
- Frame format configuration:
  - 8 data bits
  - Even or no-parity bit
  - 1 stop bit
- Default frame configuration is 8N1, meaning eight (8) data bits, no (N) parity bit, one (1) stop bit.
- Frames are transmitted in such a way that the least significant bit (LSB) is transmitted first.

2.4.2 Serial peripheral interface (SPI)

NINA-B4 supports up to four Serial Peripheral Interfaces with serial clock frequencies of up to 32 MHz. Characteristics of the SPI interfaces are listed below:

- Pin configuration in master mode:
  - SCLK, Serial clock output, up to 32 MHz
  - MOSI, Master Output Slave Input data line
  - MISO, Master Input Slave Output data line
  - CS, Chip/Slave select output, active low, selects which slave on the bus to talk to. Only one select line is enabled by default but more can be added by customizing a GPIO pin.
  - DCX, Data/Command signal, this signal is optional but is sometimes used by the SPI slaves to distinguish between SPI commands and data
- Pin configuration in slave mode:
  - SCLK, Serial clock input
  - MOSI, Master Output Slave Input data line
  - MISO, Master Input Slave Output data line
  - CS, Chip/Slave select input, active low, connects/disconnects the slave interface from the bus.
- Both master and slave modes are supported on all the interfaces.
- The serial clock supports both normal and inverted clock polarity (CPOL) and data should be captured on rising or falling clock edge (CPHA).

2.4.3 Inter-Integrated Circuit interface (I^2C)

The Inter-Integrated Circuit (I^2C) interfaces can be used to transfer and/or receive data on a 2-wire bus network. The NINA-B4 modules can operate as both master and slave on the I^2C bus using standard (100 kbps), fast (400 kbps), and 250 kbps transmission speeds. The interface supports clock stretching, thus allowing NINA-B4 to temporarily pause any I^2C communications. Up to 127 individually addressable I^2C devices can be connected to the same two signals.

- Pin configuration:
  - SCL, clock output in master mode, input in slave mode
  - SDA, data input/output pin

This interface requires external pull-up resistors to work properly in the master mode; see section 4.2.7 for suggested resistor values. The pull-up resistors are required in the slave mode as well but should be placed at the master end of the interface.

2.4.4 Inter-IC Sound interface (I^2S)

The Inter-IC Sound (I^2S) interface can be used to transfer audio sample streams between NINA-B4 and external audio devices such as codecs, DACs, and ADCs. It supports original I^2S and left or right-aligned interface formats in both master and slave modes.

- Pin configuration:
  - MCK, master clock
  - LRCK, left right/word/sample clock
  - SCK, serial clock
  - SDIN, serial data in
  - SDOUT, serial data out

The master side of an I^2S interface always provides the **LRCK** and **SCK** clock signals, but some master devices cannot generate a **MCK** clock signal. NINA-B4 can supply a **MCK** clock signal in both master and slave modes to provide to those external systems that cannot generate their own clock signal. The two data signals - **SDIN** and **SDOUT** allow for simultaneous bi-directional audio streaming. The interface supports 8, 16, and 24-bit sample widths with up to 48 kHz sample rate.

2.4.5 USB 2.0 interface

The NINA-B4 series modules include a full speed Universal Serial Bus (USB) device interface which is compliant to version 2.0 of the USB specification. Characteristics of the USB interface include:

- Full speed device, up to 12 Mbit/s transfer speed
- MAC and PHY implemented in the hardware
- Pin configuration:
  - VBUS, 5 V supply input, required to use the interface
  - USB_DP, USB_DM, differential data pair
- Automatic or software controlled pull-up of the **USB_DP** pin

The USB interface has a dedicated power supply that requires a 5 V supply voltage to be applied to the **VBUS** pin. This allows the USB interface to be used even though the rest of the module might be battery powered or supplied by a 1.8 V supply etc.

2.5 Digital interfaces

2.5.1 Pulse Width Modulation (PWM)

The NINA-B4 modules provide up to 16 independent PWM channels that can be used to generate complex waveforms. These waveforms can be used to control motors, dim LEDs, or as audio signals if connected to the speakers. Duty-cycle sequences may be stored in the RAM to be chained and looped into complex sequences without CPU intervention. Each channel uses a single GPIO pin as output.

2.5.2 Pulse Density Modulation (PDM)

The pulse density modulation interface is used to read signals from external audio frontends like digital microphones. It supports single or dual-channel (left and right) data input over a single GPIO pin. It supports up to 16 kHz sample rate and 16 bit samples. The interface uses the DMA to automatically move the sample data into RAM without CPU intervention. The interface uses two signals - **CLK** to output the sample clock and **DIN** to read the sample data.

2.5.3 Quadrature Decoder (QDEC)

The quadrature decoder is used to read quadrature encoded data from mechanical and optical sensors in the form of digital waveforms. Quadrature encoded data is often used to indicate rotation of a mechanical shaft in either a positive or negative direction. The QDEC uses two inputs - **PHASE_A** and **PHASE_B**, and an optional **LED** output signal. The interface has a selectable sample period ranging from 128 µs to 131 ms.

2.6 Analog interfaces

10 out of the 38 digital GPIOs can be multiplexed to analog functions. The following analog functions are available:

- 1x 8-channel ADC
- 1x Analog comparator*
- 1x Low-power analog comparator*

*Only one comparator can be used at any given point of time.

2.6.1 Analog to Digital Converter (ADC)

The Analog to Digital Converter (ADC) is used to sample analog voltage on the analog function enabled pins of the NINA-B4. Any of the 8 analog inputs can be used. Characteristics of the ADC include:

- Full swing input range of 0 V to **VCC**.
- 8/10/12-bit resolution
- 14-bit resolution while using oversampling
- Up to 200 kHz sample rate
- Single shot or continuous sampling
- Two operation modes: Single-ended or Differential
- Single-ended mode:
  - A single input pin is used
- Differential mode:
  - Two inputs are used and the voltage level difference between them is sampled

If the sampled signal level is much lower than the **VCC**, it is possible to lower the input range of the ADC to better encompass the wanted signal, and achieve a higher effective resolution. Continuous sampling can be configured to sample at a configurable time interval, or at different internal or external events, without CPU involvement.

2.6.2 Comparator

The analog comparator compares the analog voltage on one of the analog enabled pins in NINA-B4 with a highly configurable internal or external reference voltage. Events can be generated and distributed to the rest of the system when the voltage levels cross. Further characteristics of the comparator include:

- Full swing input range of 0 V to VCC
- Two operation modes: Single-ended or Differential
- Single-ended mode:
  - A single reference level or an upper and lower hysteresis selectable from a 64-level reference ladder with a range from 0 V to VREF (described in Table 4)
- Differential mode:
  - Two analog pin voltage levels are compared, optionally with a 50 mV hysteresis
- Three selectable performance modes - High speed, balanced, or power save

See section 4.2.8 for a comparison of the various analog comparator options.

2.6.3 Low power comparator

In addition to the power save mode available for the comparator, there is a separate low power comparator available on the NINA-B4 module. This allows for even lower power operation, at a slightly lower performance and with less configuration options. Characteristics of the low power comparator include:

- Full swing input range of 0 to **VCC**
- Two operation modes - Single-ended or Differential
- Single-ended mode:
  - The reference voltage LP_VIN- is selected from a 15-level reference ladder
- Differential mode:
  - Pin **GPIO_16** or **GPIO_18** is used as reference voltage LP_VIN-
- Can be used to wake the system from sleep mode

See section 4.2.8 for the electrical specifications of the different analog comparator options. See Table 4 for a summary of the analog pin options. Since the run current of the low power comparator is

very low, it can be used in the module sleep mode as an analog trigger to wake up the CPU. See section 2.3.3.2 for additional information.

2.6.4 Analog pin options

Table 4 shows the supported connections of the analog functions.

☞ An analog pin may not be simultaneously connected to multiple functions.

Symbol	Analog function	Can be connected to
ADCP	ADC single-ended or differential positive input	Any analog pin or **VCC**
ADCN	ADC differential negative input	Any analog pin or **VCC**
VIN+	Comparator input	Any analog pin
VREF	Comparator single-ended mode reference ladder input	Any analog pin, **VCC**, 1.2 V, 1.8V or 2.4V
VIN-	Comparator differential mode negative input	Any analog pin
LP_VIN+	Low-power comparator IN+	Any analog pin
LP_VIN-	Low-power comparator IN-	**GPIO_16** or **GPIO_18**, 1/16 to 15/16 **VCC** in steps of 1/16 **VCC**

Table 4: Possible uses of the analog pins

2.7 GPIO

The NINA-B4 series modules have a versatile pin-out. In an un-configured state, there will be 38 GPIO pins in total and no analog or digital interfaces. All interfaces or functions must then be allocated to a GPIO pin before use. 10 out of the 38 GPIO pins are analog enabled, meaning that they can have an analog function allocated to them. In addition to the serial interfaces, Table 5 shows the number of digital and analog functions that can be assigned to a GPIO pin. Two of the GPIOs are optional NFC and two GPIOs optional for external an LFCLK crystal, namely XL1 and XL2.

2.7.1 Drive strength

All GPIO pins are normally configured for low current consumption. Using this standard drive strength, a pin configured as output can only source or sink a certain amount of current. If the timing requirements of a digital interface cannot be met or if an LED requires more current, a high drive strength mode is available so the digital output can draw more current. See section 4.2.6.

Function	Description	Default NINA pin	Configurable GPIOs
General purpose input	Digital input with configurable pull-up, pull-down, edge detection and interrupt generation		Any
General purpose output	Digital output with configurable drive strength, push-pull, open collector or open emitter output		Any
Pin disabled	Pin is disconnected from the input and output buffers	All*	Any
Timer/ counter	High precision time measurement between two pulses/ Pulse counting with interrupt/event generation		Any
Interrupt/ Event trigger	Interrupt/event trigger to the software application/ Wake up event		Any
HIGH/LOW/Toggle on event	Programmable digital level triggered by internal or external events without CPU involvement		Any
ADC input	8/10/12/14-bit analog to digital converter		Any analog
Analog comparator input	Compare two voltages, capable of generating wake-up events and interrupts		Any analog
PWM output	Output simple or complex pulse width modulation waveforms		Any
Connection status indication	Indicates if a Bluetooth LE connection is maintained	BLUE**	Any

* = If left unconfigured ** = While using the u-connectXpress software

Table 5: GPIO custom functions configuration

2.8 u-connectXpress software features

This section describes some of the system related features in the u-connectXpress software pre-loaded in the NINA-B41 modules. For additional information, see the u-blox Short Range AT Commands Manual [2] and u-connectXpress software User guide [4].

2.8.1 u-blox Serial Port Service (SPS)

The serial port service feature enables serial port emulation over Bluetooth LE.

2.8.2 System status signals

The **RED, GREEN, and BLUE** pins are used to signal the system status as shown in Table 6. They are active low and are intended to be routed to an RGB LED.

Mode	Status	RGB LED Color	RED	GREEN	BLUE
Data mode/Extended Data mode (EDM)	IDLE	Green	HIGH	LOW	HIGH
Command mode	IDLE	Orange	LOW	LOW	HIGH
EDM/Data mode, Command mode	CONNECTING	Purple	LOW	HIGH	LOW
EDM/Data mode, Command mode	CONNECTED**	Blue	HIGH	HIGH	LOW

* = LED flashes on data activity

Table 6: System status indication

⚠ Green LED not supported initially.

☞ The CONNECTING and CONNECTED statuses indicate u-blox SPS connections.

2.8.3 System control signals

The following input signals are used to control the system:

- **RESET_N** is used to reset the system. See section 2.3.4 for detailed information.
- If **SWITCH_2** is driven low during start up, the UART serial settings are restored to their default values.
- The **SWITCH_2** can be used to open a Bluetooth LE connection with a peripheral device.
- If both **SWITCH_1** and **SWITCH_2** are driven low during startup, the system will enter bootloader mode.
- If both **SWITCH_1** and **SWITCH_2** are driven low during start up and held low for 10 seconds, the system will exit the bootloader mode and restore all settings to their factory default.

2.8.4 UART signals

In addition to the normal **RXD**, **TXD**, **CTS,** and **RTS** signals, the u-connectXpress software adds the **DSR** and **DTR** pins to the UART interface. Note that they are not used as originally intended, but to control the state of the NINA module. For example, depending on the current configuration:

The **DSR** pin can be used to:

- Enter the command mode
- Disconnect and/or toggle connectable status
- Enable/disable the rest of the UART interface
- Enter/wake up from the sleep mode.

The **DTR** pin can be used to indicate:

- The System mode
- If the SPS peers are connected
- If a Bluetooth LE bonded device is connected
- A Bluetooth LE GAP connection.

☞ See the u-blox Short Range AT Commands Manual [2] for more information.

2.9 Debug interfaces

2.9.1 SWD

The NINA-B40 series modules provide an SWD interface for flashing and debugging. The SWD interface consists of two pins - **SWDCLK** and **SWDIO**. The SWD interface is disabled on the NINA-B41 series modules.

2.9.2 Trace – Serial Wire Output

A serial trace option is available on the NINA-B40 series modules as an additional pin- **SWO**. The Serial Wire Output (SWO) is used to:

- Support printf style debugging
- Trace OS and application events
- Emit diagnostic system information

A debugger that supports Serial Wire Viewer (SWV) is required.

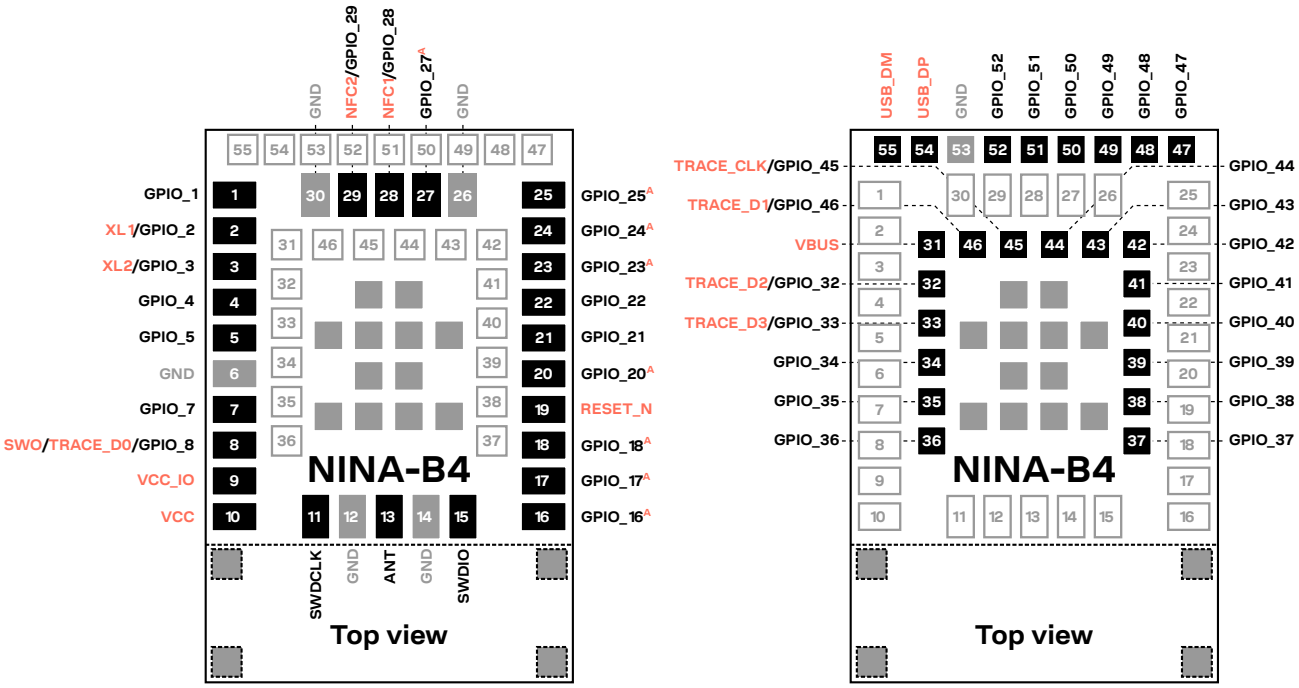
2.9.3 Parallel Trace

The NINA-B40 series modules support parallel trace output as well. This allows output from the Embedded Trace Macrocell (ETM) and Instrumentation Trace Macrocell (ITM) embedded in the Arm® Cortex®-M4 core of the nRF52833 chip in the NINA-B4. The ETM trace data allows a user to record exactly how the application goes through the CPU instructions in real time. The parallel trace interface uses 1 clock signal and 4 data signals respectively - **TRACE_CLK**, **TRACE_D0**, **TRACE_D1**, **TRACE_D2** and **TRACE_D3**.

3 Pin definition

3.1 NINA-B40 series pin assignment

The pin-out described in Figure 3 is an example assignment that shows the module in an unconfigured state.



A = Analog function capable pin

Figure 3: NINA-B40 series pin assignment (top view)

The grey pins in the center of the modules are GND pins. The outline below the dotted line as shown in Figure 3, the antenna area of the NINA- B400 and NINA-B406 begins. The four grey pins with dotted outlines in the antenna area are GND pins and are only present on NINA-B406.

Most of the digital or analog functions described in this data sheet may be freely assigned to any GPIO pin. Analog functions are limited to analog capable pins. Signals that are highlighted in red in Figure 3 are not freely assignable but locked to a specific pin.

Some GPIO pins are connected to the pins located close to the radio part of the RF chip. Digital noise on these pins can reduce the radio sensitivity.

Do not apply an NFC field to the NFC pins when they are configured as GPIOs as this can cause permanent damage to the module. When driving different logic levels on these pins in the GPIO mode, a small current leakage will occur. Ensure that they are set to the same logic level before entering into any power saving modes. See section 4.2.6 for more information.

No.	Name	I/O	Description	nRF52 pin	Remarks
1	GPIO_1	I/O	General purpose I/O	P0.13	
2	XL1/GPIO_2	I/O	General purpose I/O Analog function enabled GPIO Connection for 32.768 kHz crystal	P0.00	May be used as a GPIO. If not used ground XL1 and XL2. If an external clock source is used instead of a crystal:
3	XL2/GPIO_3	I/O	General purpose I/O Analog function enabled GPIO	P0.01	Apply external low swing signal to XL1, ground XL2.

No.	Name	I/O	Description	nRF52 pin	Remarks
			Connection for 32.76analog kHz crystal		Apply external full swing signal to XL1, leave XL2 grounded or unconnected.
4	GPIO_4	I/O	General purpose I/O	P0.16	
5	GPIO_5	I/O	General purpose I/O	P0.17	
6	GND	-	Ground		
7	GPIO_7	I/O	General purpose I/O	P1.01	[1] Standard drive, low frequency GPIO only
8	SWO/TRACE_D0/ GPIO_8	I/O	General purpose I/O	P1.00	May be used for parallel/serial trace debug
9	VCC_IO	I	Module I/O level voltage input		Must be connected to VCC on NINA-B1
10	VCC	I	Module supply voltage input		1.7-3.6 V range
11	SWDCLK	I	Serial Wire Debug port clock signal	SWDCLK	
12	GND	-	Ground		
13	ANT	I/O	Tx/Rx antenna interface		50 Ω nominal characteristic impedance
14	GND	-	Ground		
15	SWDIO	I/O	Serial Wire Debug port data signal	SWDIO	
16	GPIO_16	I/O	Analog function enabled GPIO	P0.03	[1] Standard drive, low frequency GPIO only Pin is analog capable
17	GPIO_17	I/O	Analog function enabled GPIO	P0.28	[1] Standard drive, low frequency GPIO only Pin is analog capable
18	GPIO_18	I/O	Analog function enabled GPIO	P0.02	[1] Standard drive, low frequency GPIO only Pin is analog capable
19	RESET_N	I/O	System reset input	P0.18	Active low
20	GPIO_20	I/O	Analog function enabled GPIO	P0.31	[1] Standard drive, low frequency GPIO only Pin is analog capable, radio sensitive pin
21	GPIO_21	I/O	General purpose I/O	P0.23	[1] Standard drive, low frequency GPIO only
22	GPIO_22	I/O	General purpose I/O	P1.05	[1] Standard drive, low frequency GPIO only
23	GPIO_23	I/O	Analog function enabled GPIO	P0.29	[1] Standard drive, low frequency GPIO only Pin is analog capable
24	GPIO_24	I/O	Analog function enabled GPIO	P0.30	[1] Standard drive, low frequency GPIO only Pin is analog capable
25	GPIO_25	I/O	Analog function enabled GPIO	P0.04	Pin is analog capable
26	GND	-	Ground		
27	GPIO_27	I/O	Analog function enabled GPIO	P0.05	Pin is analog capable
28	NFC1/GPIO_28	I/O	NFC pin 1 (default)	P0.09	May be used as a GPIO [1] Standard drive, low frequency GPIO only
29	NFC2/GPIO_29	I/O	NFC pin 2 (default)	P0.10	May be used as a GPIO [1] Standard drive, low frequency GPIO only
30	GND	-	Ground		
31	VBUS	I	USB interface 5 V input	VBUS	Is required for USB interface to work
32	TRACE_D2/GPIO_32	I/O	General purpose I/O	P0.11	May be used for parallel trace debug
33	TRACE_D3/GPIO_33	I/O	General purpose I/O	P1.09	May be used for parallel trace debug
34	GPIO_34	I/O	General purpose I/O	P0.14	
35	GPIO_35	I/O	General purpose I/O	P1.04	[1] Standard drive, low frequency GPIO only
36	GPIO_36	I/O	General purpose I/O	P1.02	[1] Standard drive, low frequency GPIO only
37	GPIO_37	I/O	General purpose I/O	P1.06	[1] Standard drive, low frequency GPIO only
38	GPIO_38	I/O	General purpose I/O	P0.25	[1] Standard drive, low frequency GPIO only
39	GPIO_39	I/O	General purpose I/O	P1.07	[1] Standard drive, low frequency GPIO only

No.	Name	I/O	Description	nRF52 pin	Remarks
40	GPIO_40	I/O	General purpose I/O	P0.19	[1] Standard drive, low frequency GPIO only
41	GPIO_41	I/O	General purpose I/O	P1.03	[1] Standard drive, low frequency GPIO only
42	GPIO_42	I/O	General purpose I/O	P0.26	
43	GPIO_43	I/O	General purpose I/O	P0.15	
44	GPIO_44	I/O	General purpose I/O	P0.27	
45	TRACE_CLK/GPIO_45	I/O	General purpose I/O	P0.07	May be used for parallel or serial trace debug
46	TRACE_D1/GPIO_46	I/O	General purpose I/O	P0.12	May be used for parallel trace debug
47	GPIO_47	I/O	General purpose I/O	P0.06	
48	GPIO_48	I/O	General purpose I/O	P0.21	
49	GPIO_49	I/O	General purpose I/O	P0.22	
50	GPIO_50	I/O	General purpose I/O	P0.20	
51	GPIO_51	I/O	General purpose I/O	P1.08	
52	GPIO_52	I/O	General purpose I/O	P0.08	
53	GND	-	Ground		
54	USB_DP	I/O	USB differential data signal	USB_DP	
55	USB_DM	I/O	USB differential data signal	USB_DM	
	EGP	-	Exposed Ground Pins		The exposed pins in the center of the module should be connected to GND
	EAGP	-	Exposed Antenna Ground Pins		The exposed pins underneath the antenna area should be connected to GND

Table 7: NINA-B40 series pin-out

[1] It is recommended to keep frequencies below 10 kHz, and only use standard drive strength on these digital pins.

3.2 NINA-B41 series pin assignment (with u-connectXpress)

The pin-out as shown in Figure 4 describes the pin configuration used by the u-connectXpress software.

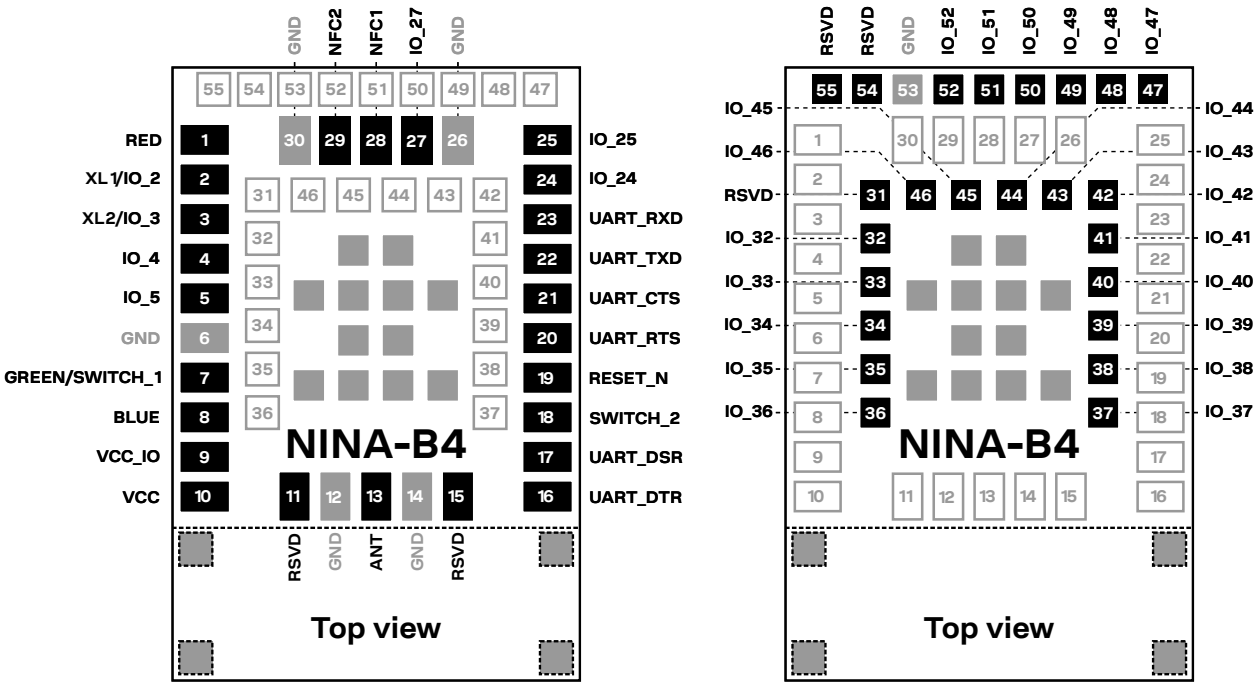


Figure 4: NINA-B41 series pin assignment (top view)

The grey pins in the center of the modules are GND pins. The outline below the dotted line as shown in Figure 4, the antenna area of the NINA- B410 and NINA-B416 begins. The four grey pins with dotted outlines in the antenna area are GND pins and are only present on NINA-B416.

⚠ Follow this pin layout when using the u-connectXpress software. No interfaces can be moved or added.

⚠ Do not apply an NFC field to the NFC pins when they are configured as GPIOs as it can cause permanent damage to the module. While using the u-connectXpress software, these pins will always be set to the NFC mode. See section 4.2.6 for more information.

No.	Name	I/O	Description	Remarks
1	RED	O	RED system status signal	Active low, should be routed to an RGB LED
2	XL1/IO_2	I/O	u-connectXpress (uX) IO pin Connection for 32.768 kHz crystal	Can be used for manual digital I/O. If not used ground XL1 and XL2. If an external clock source is used instead of a crystal: Apply external low swing signal to XL1, ground XL2. Apply external full swing signal to XL1, leave XL2 grounded or unconnected.
3	XL2/IO_3	I/O	uX IO pin Connection for 32.768 kHz crystal	
4	IO_4	I/O	uX IO pin	Can be used for manual digital I/O
5	IO_5	I/O	uX IO pin	Can be used for manual digital I/O
6	GND	-	Ground	
7	GREEN/SWITCH_1	I/O	This signal is multiplexed: GREEN: System status signal. SWITCH_1: Multiple functions	Active low. GREEN: Should be routed to an RGB LED. SWITCH_1: See section 2.8.3 for more information.
8	BLUE	O	BLUE system status signal	Active low, should be routed to an RGB LED
9	VCC_IO	I	Module I/O level voltage input	Must be connected to VCC on NINA-B4
10	VCC	I	Module supply voltage input	1.7-3.6 V range
11	RSVD	-	RESERVED pin	Leave unconnected
12	GND	-	Ground	
13	ANT	I/O	Tx/Rx antenna interface	50 Ω nominal characteristic impedance, only used with NINA-B410 modules

No.	Name	I/O	Description	Remarks
14	GND	-	Ground	
15	RSVD	-	RESERVED pin	Leave unconnected
16	UART_DTR	O	UART data terminal ready signal	Used to indicate system status
17	UART_DSR	I	UART data set ready signal	Used to change the system modes
18	SWITCH_2	I	Multiple functions	Active low, see section 2.8.3 for more information.
19	RESET_N	I	External system reset input	Active low
20	UART_RTS	O	UART request to send control signal	Used only when hardware flow control is enabled
21	UART_CTS	I	UART clear to send control signal	Used only when hardware flow control is enabled
22	UART_TXD	O	UART data output	Also used by the bootloader
23	UART_RXD	I	UART data input	Also used by the bootloader
24	IO_24	I/O	uX IO pin	Can be used for manual digital I/O
25	IO_25	I/O	uX IO pin	Can be used for manual digital I/O
26	GND	-	Ground	
27	IO_27	I/O	uX IO pin	Can be used for manual digital I/O
28	NFC1	I/O	NFC pin 1	
29	NFC2	I/O	NFC pin 2	
30	GND	-	Ground	
31	RSVD	-	RESERVED pin	Leave unconnected
32	IO_32	I/O	uX IO pin	Can be used for manual digital I/O
33	IO_33	I/O	uX IO pin	Can be used for manual digital I/O
34	IO_34	I/O	uX IO pin	Can be used for manual digital I/O
35	IO_35	I/O	uX IO pin	Can be used for manual digital I/O
36	IO_36	I/O	uX IO pin	Can be used for manual digital I/O
37	IO_37	I/O	uX IO pin	Can be used for manual digital I/O
38	IO_38	I/O	uX IO pin	Can be used for manual digital I/O
39	IO_39	I/O	uX IO pin	Can be used for manual digital I/O
40	IO_40	I/O	uX IO pin	Can be used for manual digital I/O
41	IO_41	I/O	uX IO pin	Can be used for manual digital I/O
42	IO_42	I/O	uX IO pin	Can be used for manual digital I/O
43	IO_43	I/O	uX IO pin	Can be used for manual digital I/O
44	IO_44	I/O	uX IO pin	Can be used for manual digital I/O
45	IO_45	I/O	uX IO pin	Can be used for manual digital I/O
46	IO_46	I/O	uX IO pin	Can be used for manual digital I/O
47	IO_47	I/O	uX IO pin	Can be used for manual digital I/O
48	IO_48	I/O	uX IO pin	Can be used for manual digital I/O
49	IO_49	I/O	uX IO pin	Can be used for manual digital I/O
50	IO_50	I/O	uX IO pin	Can be used for manual digital I/O
51	IO_51	I/O	uX IO pin	Can be used for manual digital I/O
52	IO_52	I/O	uX IO pin	Can be used for manual digital I/O
53	GND	-	Ground	
54	RSVD	-	RESERVED pin	Leave unconnected
55	RSVD	-	RESERVED pin	Leave unconnected
	EGP	-	Exposed Ground Pins	Connect exposed center to GND
	EAGP	-	Exposed Antenna Ground Pins	Connect exposed pins underneath the antenna to GND

Table 8: NINA-B41 series with u-connectXpress software pin-out

4 Electrical specifications

⚠ Stressing the device above one or more of the ratings listed in the Absolute maximum rating section may cause permanent damage. These are stress ratings only. Operating the module at these or at any conditions other than those specified in the Operating conditions section of this document should be avoided. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

☞ Operating condition ranges define those limits within which the functionality of the device is guaranteed. Where application information is given, it is advisory only and does not form part of the specification.

4.1 Absolute maximum ratings

Symbol	Description	Condition	Min	Max	Unit
VCC	Module supply voltage	Input DC voltage at VCC pin	–0.3	3.9	V
V_DIO	Digital pin voltage	Input DC voltage at any digital I/O pin, VCC ≤ 3.6 V	–0.3	VCC + 0.3	V
		Input DC voltage at any digital I/O pin, VCC > 3.6 V	–0.3	3.9	V
P_ANT	Maximum power at receiver	Input RF power at antenna pin		+10	dBm

Table 9: Absolute maximum ratings

⚠ The product is not protected against overvoltage or reversed voltages. The voltage spikes exceeding the power supply voltage specification, provided in Table 9, must be limited to the values within the specified boundaries by using appropriate protection devices.

4.1.1 Maximum ESD ratings

Parameter	Min	Typical	Max	Unit	Remarks
ESD sensitivity for all pins except **ANT** pin			4	kV	Human body model class 3A according to JEDEC JS001
			500	V	Charged device model according to JESD22-C101
ESD indirect contact discharge			±8	kV	According to EN 301 489-1

Table 10: Maximum ESD ratings

⚠ NINA-B4 series modules are Electrostatic Sensitive Devices and require special precautions while handling. See section 8.4 for ESD handling instructions.

4.2 Operating conditions

☞ Unless otherwise specified, all operating condition specifications are at an ambient temperature of 25 °C and a supply voltage of 3.3 V.

⚠ Operation beyond the specified operating conditions is not recommended and extended exposure beyond them may affect device reliability.

4.2.1 Operating temperature range

Parameter	Min	Max	Unit
Storage temperature	–40	+125	°C
Operating temperature	–40	+105	°C

Table 11: Temperature range

4.2.2 Supply/Power pins

Symbol	Parameter	Min	Typ	Max	Unit
VCC	Input supply voltage	1.7	3.3	3.6	V
t_RVCC	Supply voltage rise time			60	ms
VCC_ripple	VCC input noise peak to peak, 10 - 100 KHz			TBD	mV
	VCC input noise peak to peak, 100 KHz - 1 MHz			TBD	mV
	VCC input noise peak to peak, 1 - 3 MHz			TBD	mV
VCC_IO	I/O reference voltage		VCC		V

Table 12: Input characteristics of voltage supply pins

4.2.3 Current consumption

Table 13 shows the typical current consumption of a NINA-B4 module at 3V supply, independent of the software used.

Condition	Typical	Peak
No clocks running, no RAM data retention	600 nA	
No clocks running, 128 kB RAM data retention	1.3 µA	
RTC and 128 kB RAM data retention. System running on 32.768 kHz clock from internal oscillator.	2.4 µA	
CPU running CoreMark benchmarking tests @ 64 MHz from flash, DC/DC	3.70 mA	
Radio RX only @ 1 Mbps Bluetooth LE mode	4.6 mA	
Radio TX only, 0 dBm output power	4.8 mA	
Radio TX only, +8 dBm output power	14.8 mA	
CPU running benchmarking tests, 1 Mbps, Radio TX 0 dBm output power	8.9 mA	

Table 13: Module VCC current consumption

Table 14 shows the current consumption during some typical use cases when using the u-connectXpress software:

⚠ The current values hereafter are temporary and not yet confirmed.

		3.3 V VCC		1.8 V VCC	
Mode	**Condition**	**Average**	**Peak**	**Average**	**Peak**
Active	Advertising (u-blox Serial Service, Apple iBeacon etc.) at 1 s intervals with +8 dBm output power and 31 bytes payload, CPU and UART interface is running				
	1 Mbit/s PHY	0.93 mA	20 mA	1.0 mA	37 mA
	CODED PHY	1.0 mA	20 mA	1.3 mA	37 mA
Standby	Advertising (u-blox Serial Service, Apple iBeacon etc.) at 1 s intervals with +8 dBm output power and 31 bytes payload				
	1 Mbit/s PHY	50 µA	19 mA	65 µA	36 mA
	CODED PHY	150 µA	19 mA	230 µA	36 mA
Active	Connected as peripheral, 50 ms connection interval, +8 dBm output power, no data throughput, CPU and UART interface is running				
	1 Mbit/s PHY	0.98 mA	20 mA	1.2 mA	37 mA
	2 Mbit/s PHY	0.95 mA	20 mA	1.2 mA	37 mA
	CODED PHY	1.2 mA	20 mA	1.6 mA	37 mA
Standby	Connected as peripheral, 50 ms connection interval, +8 dBm output power, no data throughput				
	1 Mbit/s PHY	110 µA	19 mA	150 µA	36 mA

Mode	Condition	3.3 V VCC Average	3.3 V VCC Peak	1.8 V VCC Average	1.8 V VCC Peak
	2 Mbit/s PHY	99 µA	19 mA	130 µA	36 mA
	CODED PHY	380 µA	19 mA	590 µA	36 mA
Sleep	UART DSR pin is used to enter the sleep mode. No RAM retention.	400 nA	4 mA	400 nA	4 mA

Table 14: Current consumption during typical use cases.

The standby mode advertising and connected use cases described in Table 14 list the average current consumption of a NINA-B4 module when using the typical configuration of a 1 s Bluetooth advertising interval and a 50 ms connection interval. The graphs in Figure 5 and Figure 6 have been calculated, based on NINA-B4 measurement data, to show the average current consumption if different advertising or connection intervals have been configured. They also show a comparison of different output power configurations.

⚠ Make sure that the configured output power of your product does not exceed the maximum allowed limits of your intended target market(s). See the 'Regulatory information and requirements' section of the NINA-B4 Series System Integration Manual [3] for information.

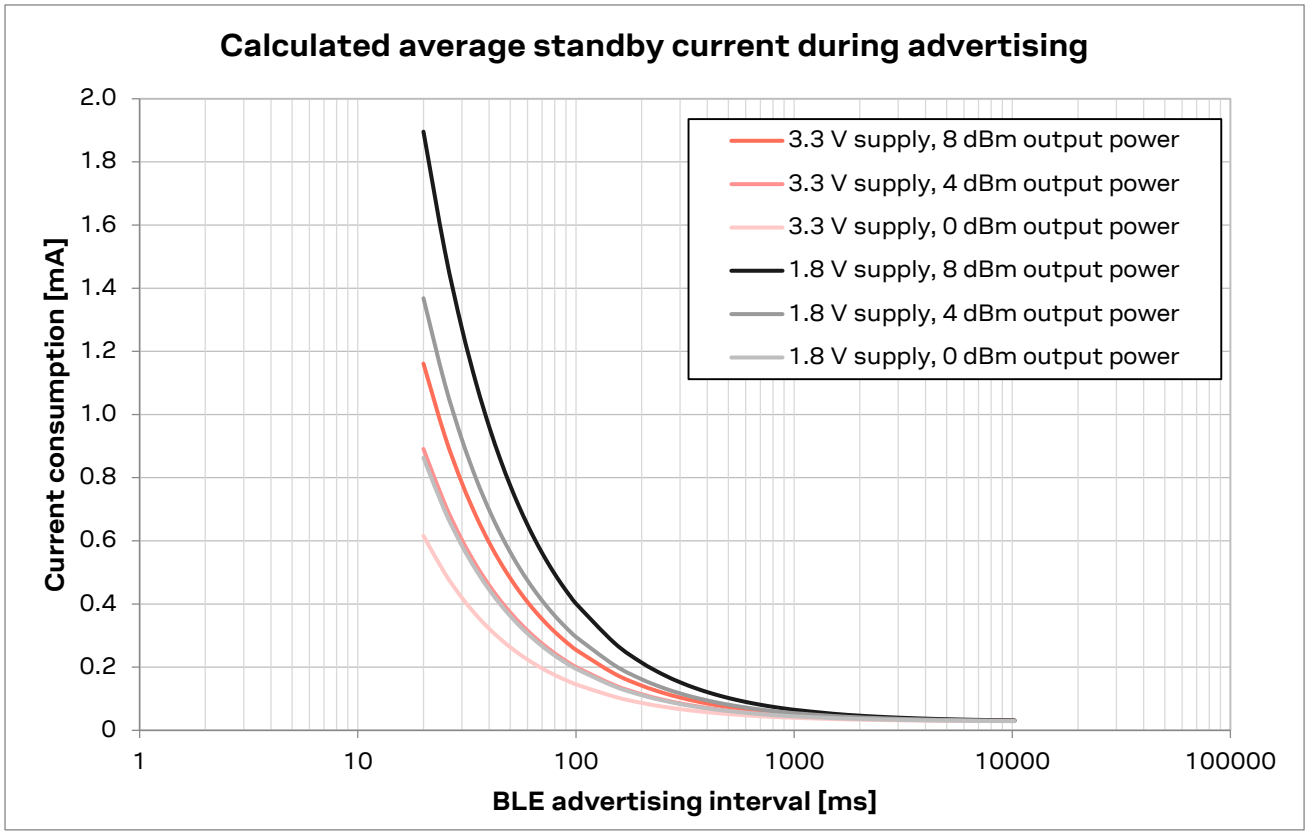


Figure 5: The average standby current for various module configurations and advertising intervals, 1 Mbit/s PHY is used. ***All values are temporary and not yet confirmed.***

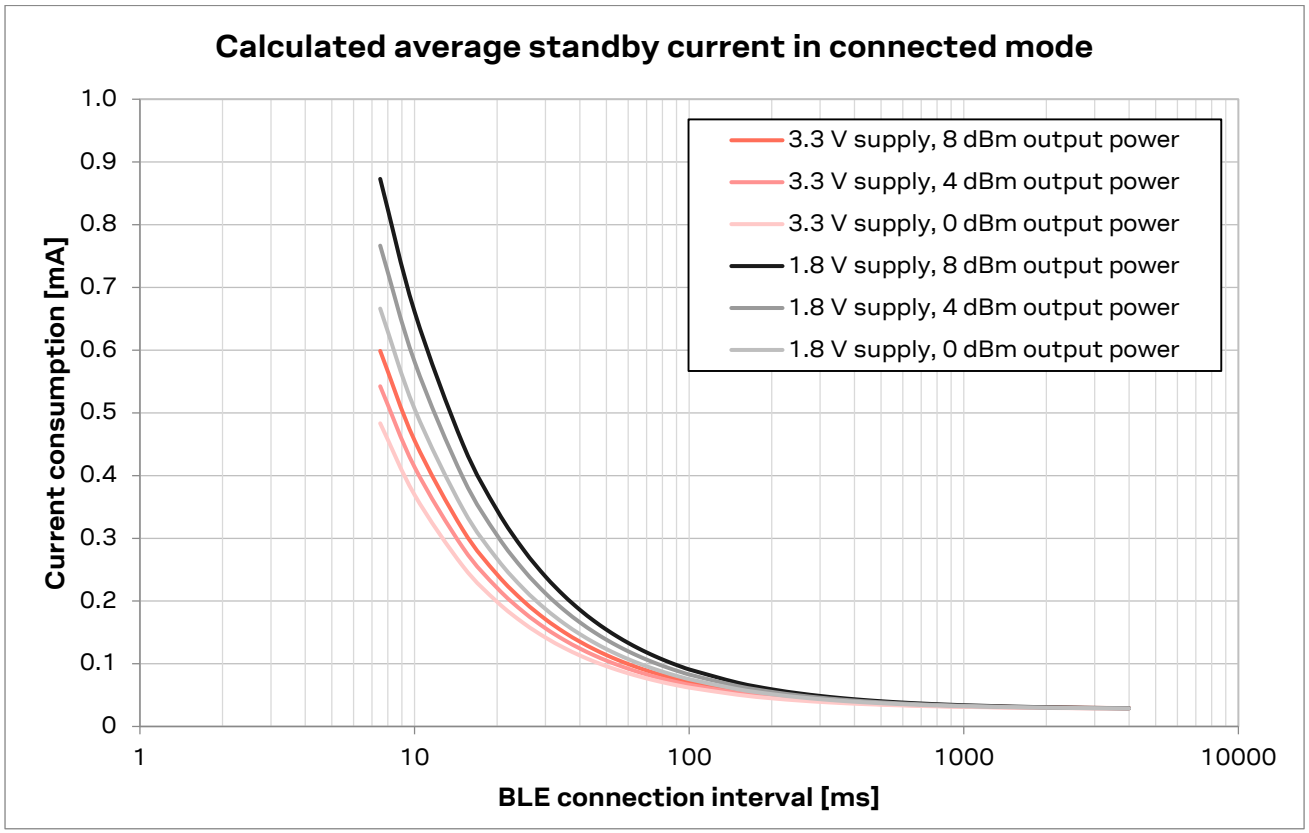


Figure 6: The average standby current for various module configurations and connection intervals, 1 Mbit/s PHY is used and no data is being sent over the link. ***All values are temporary and not yet confirmed.***

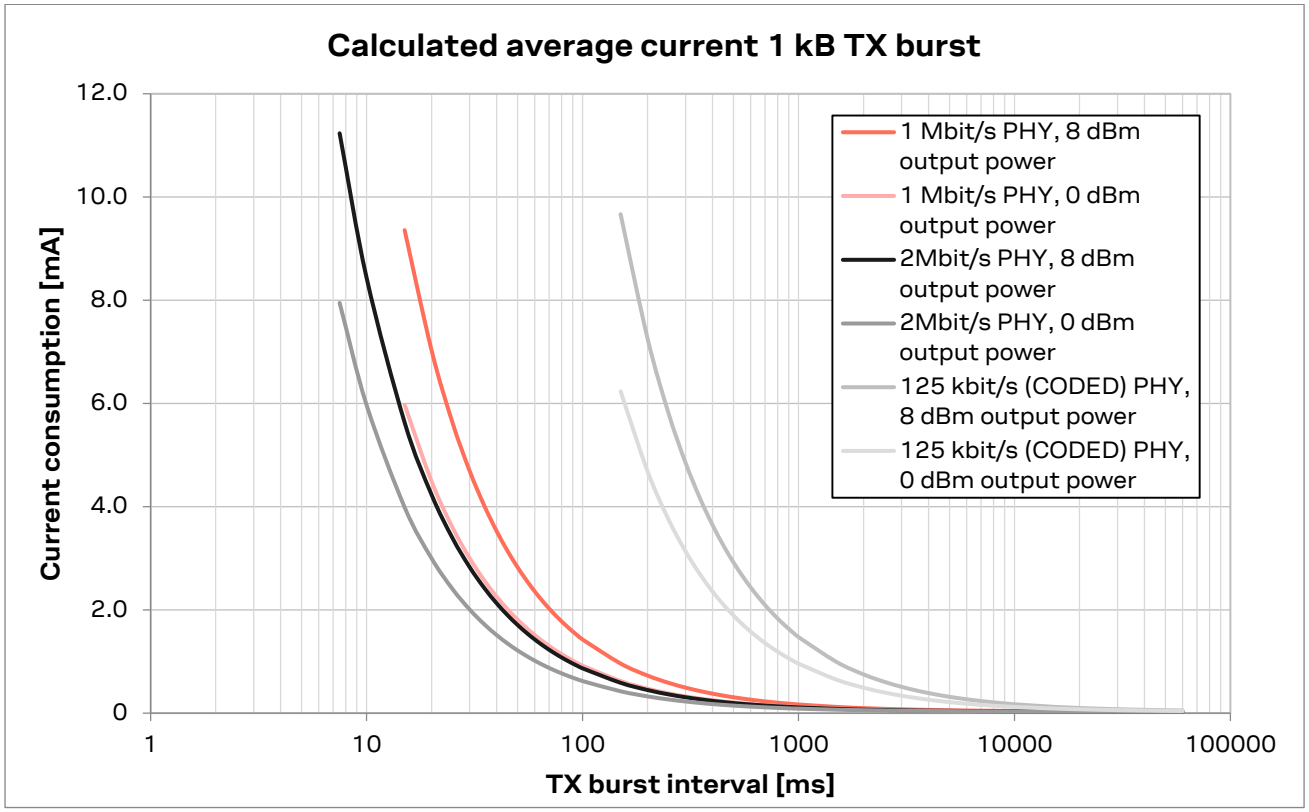


Figure 7: The average standby and TX current for different Bluetooth LE PHY configurations when transmitting a 1 kB data packet at various intervals. ***All values are temporary and not yet confirmed.***

The graph in Figure 7 has been calculated to show the current consumption of a NINA-B4 module in connected standby mode, waking up to transmit a 1 kB data packet at various intervals. The test case has been repeated using different Bluetooth LE PHYs and output power configurations.

Mode	Condition	Typical	Peak
Active	USB interface active, current drawn from the VBUS supply	2.4 mA	
Suspended	USB interface suspended, the CPU is sleeping, current drawn from the VBUS supply	262 µA	

Table 15: USB VBUS current consumption valid for unconfigured state.

4.2.4 RF performance

Parameter	Test condition	Min	Typ	Max	Unit
Receiver input sensitivity	Conducted at 25 °C, 1 Mbit/s Bluetooth LE mode		–95		dBm
	Conducted at 25 °C, 2 Mbit/s Bluetooth LE mode		–92		dBm
	Conducted at 25 °C, 500 kbit/s Bluetooth LE mode		–98		dBm
	Conducted at 25 °C, 125 kbit/s Bluetooth LE mode		–103		dBm
Maximum output power	Conducted at 25 °C		+8		dBm
NINA-B4x6 antenna gain	Mounted on an EVB-NINA-B4		+2		dBi

Table 16: RF performance.

4.2.5 RESET_N pin

Pin name	Parameter	Min	Typ	Max	Unit	Remarks
RESET_N	Low-level input	0		0.3*VCC	V	
	Internal pull-up resistance		13		kΩ	
	RESET duration			55	ms	Time taken to release a pin reset.

Table 17: RESET_N pin characteristics

4.2.6 Digital pins

Pin name	Parameter	Min	Typ	Max	Unit	Remarks
Any digital pin	Input characteristic: Low-level input	0		0.3*VCC	V	
	Input characteristic: high-level input	0.7*VCC		VCC	V	
	Output characteristic: Low-level output	0		0.4	V	Standard drive strength
		0		0.4	V	High drive strength
	Output characteristic: High-level output	VCC-0.4		VCC	V	Standard drive strength
		VCC-0.4		VCC	V	High drive strength
	Sink/Source current	1	2	4	mA	Standard drive strength
		3			mA	High drive strength, VCC < 2.7 V
		6	10	15	mA	High drive strength, sink, VCC ≥ 2.7 V
		6	9	14	mA	High drive strength, source, VCC ≥ 2.7 V
	Rise/Fall time		9 – 25		ns	Standard drive strength, depending on load capacitance
			4 – 8		ns	High drive strength, depending on load capacitance
	Input pull-up resistance	11	13	16	kΩ	Can be added to any GPIO pin configured as input
	Input pull-down resistance	11	13	16	kΩ	Can be added to any GPIO pin configured as input
GPIO_28, GPIO_29	Leakage current		1	10	µA	When not configured for NFC and driven to different logic levels

Table 18: Digital pin characteristics

4.2.7 I²C pull-up resistor values

Symbol	Parameter	Bus capacitance	Min	Typ	Max	Unit
R_PUstandard	External pull-up resistance required on I²C interface in standard mode (100 Kbps)	10 pF	1	-	115	kΩ
		50 pF	1	-	23	kΩ
		200 pF	1	-	6	kΩ
		400 pF	1	-	3	kΩ
R_PUfast	External pull-up resistance required on I²C interface in fast mode (400 Kbps)	10 pF	1	-	35	kΩ
		50 pF	1	-	7	kΩ
		200 pF	1	-	1.5	kΩ
		400 pF	1	-	1	kΩ

Table 19: Suggested pull-up resistor values

4.2.8 Analog comparator

Symbol	Parameter	Min	Typ	Max	Unit
t_powersave	Time to generate interrupt/event when the comparator is in 'power save' mode		0.6		µs
t_balanced	Time to generate interrupt/event when the comparator is in 'balanced' mode		0.2		µs
t_speed	Time to generate interrupt/event when the comparator is in 'high speed' mode		0.1		µs

Table 20: Electrical specification of the two analog comparators.

5 Mechanical specifications

5.1 NINA-B4x0 Mechanical specification

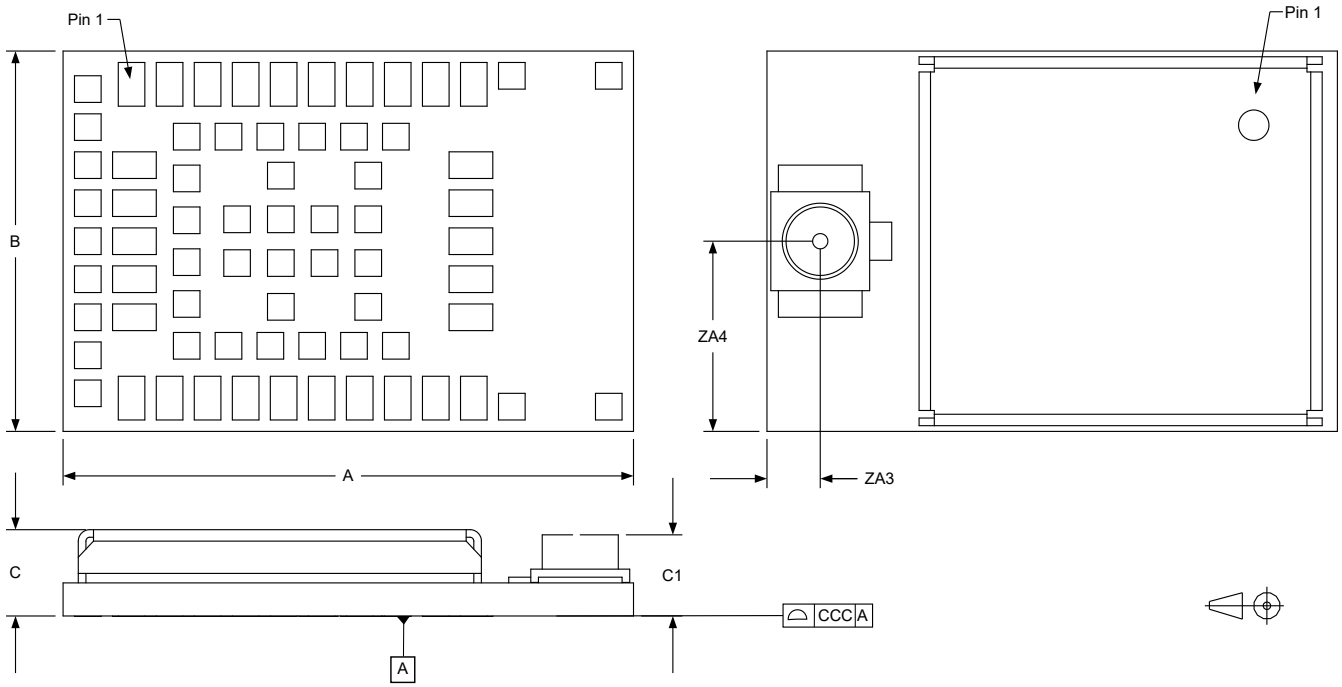


Figure 8: NINA-B4x0 mechanical outline. The footprint is equivalent to NINA-B4x6 in Figure 9 and Figure 10.

Parameter	Description	Typical [mm]	[mil]	Tolerance [mm]	[mil]
A	Module PCB length	15.0	456.7	+0.20/–0.10	+7.9/–3.9
B	Module PCB width	10.0	393.7	+0.20/–0.10	+7.9/–3.9
C	Module thickness	2.23	87.8	+0.40/–0.20	+15.8/–7.9
C1	Module thickness at U.FL antenna connector	2.13	83.9	+0.40/–0.20	+15.8/–7.9
ccc	Seating plane coplanarity	0.10	3.9	+0.02/–0.10	+0.8/–3.9
ZA3	Horizontal pin of U.FL antenna connector center to left lower corner	1.40	55.1	±0.20	±7.9
ZA4	Vertical pin of U.FL antenna connector center to left lower corner	5.00	196.8	±0.20	±7.9
	Module weight [g]	<1.0			

Table 21: NINA-B4x0 mechanical outline data. For more data see NINA-B4x6 in Table 22.

5.2 NINA-B4x6 Mechanical specification

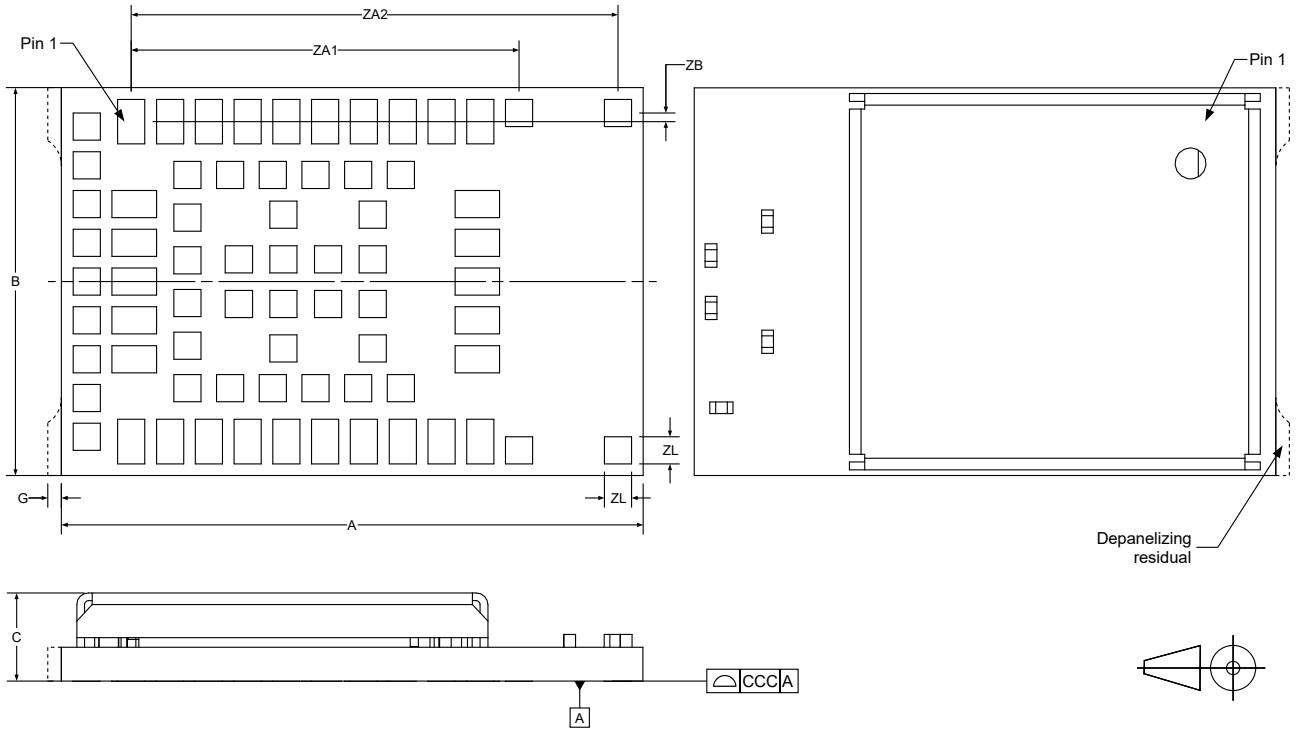


Figure 9: NINA-B4x6 mechanical outline

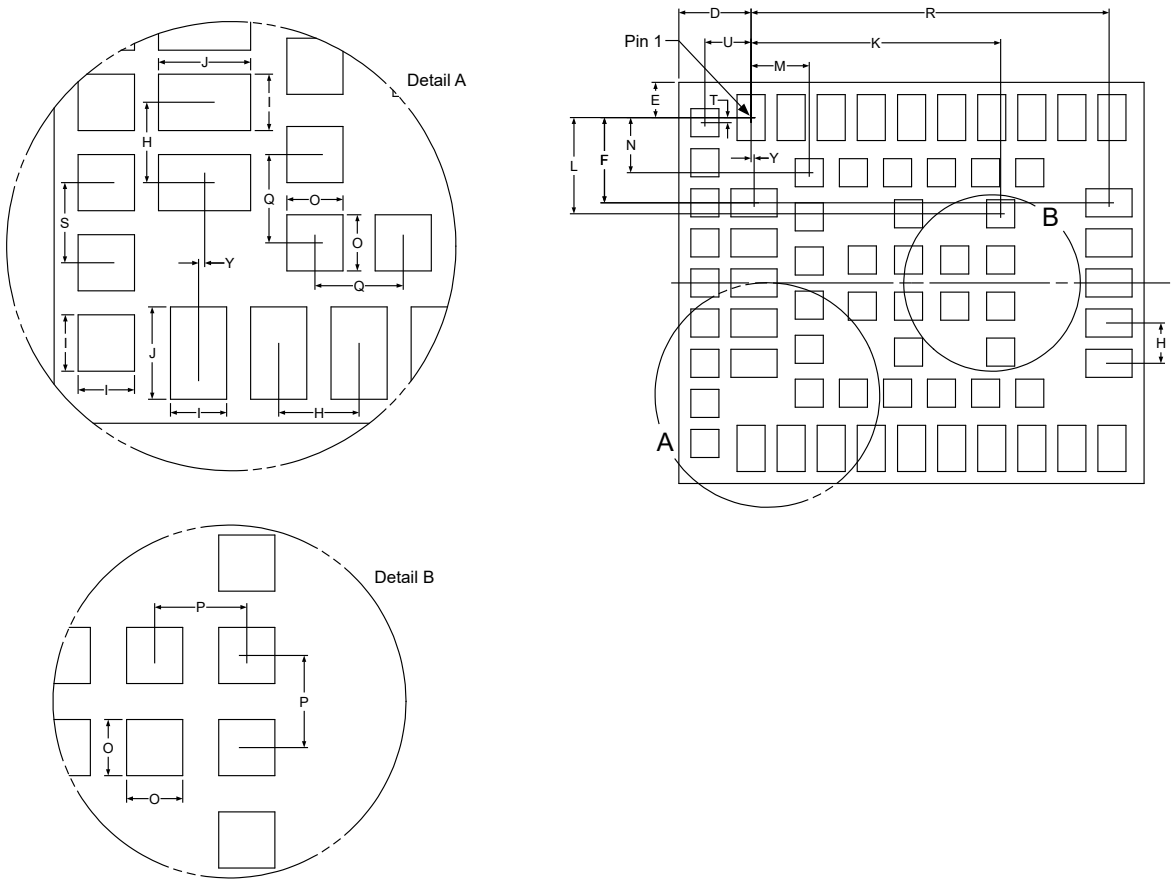


Figure 10: NINA-B4 pad dimensions. The drawing originates from pin compatible NINA-B301/B311 versions without antenna.

Parameter	Description	Typical [mm]	[mil]	Tolerance [mm]	[mil]
A	Module PCB length	15.0	456.7	+0.20/–0.10	+7.9/–3.9
B	Module PCB width	10.0	393.7	+0.20/–0.10	+7.9/–3.9
C	Module thickness	2.23	87.8	+0.40/–0.20	+15.8/–7.9
ccc	Seating plane coplanarity	0.10	3.9	+0.02/–0.10	+0.8/–3.9
D	Horizontal edge to pin no. 1 center	1.80	70.9	±0.10	±3.9
E	Vertical edge to pin no. 1 center	0.875	34.5	±0.10	±3.9
F	Vertical pin no. 1 center to lateral pin center	2.125	87.9	±0.05	±2.0
G	Depanelizing residual	0.10	3.9	+0.25/-0.1	+9.8/-3.9
H	Lateral and antenna row pin to pin pitch	1.00	39.4	±0.05	±2.0
I	Lateral, antenna row and outer pin width	0.70	27.6	±0.05	±2.0
J	Lateral and antenna row pin length	1.15	45.3	±0.05	±2.0
K	Horizontal pin no. 1 center to central pin center	6.225	245.1	±0.05	±2.0
L	Vertical pin no. 1 center to central pin center	2.40	94.5	±0.05	±2.0
M	Horizontal pin no. 1 center to inner row pin center	1.45	57.1	±0.05	±2.0
N	Vertical pin no. 1 center to inner row pin center	1.375	54.1	±0.05	±2.0
O	Central, inner and outer row pin width and length	0.70	27.6	±0.05	±2.0
P	Central pin to central pin pitch	1.15	45.3	±0.05	±2.0
Q	Inner row pin to pin pitch	1.10	43.3	±0.05	±2.0
R	Horizontal pin no. 1 center to antenna row pin center	8.925	351.4	±0.05	±2.0
S	Outer row pin to pin pitch	1.00	39.4	±0.05	±2.0
T	Vertical pin no. 1 center to outer row pin center	0.125	4.9	±0.05	±2.0
U	Horizontal pin no. 1 center to outer row pin center	1.15	45.3	±0.05	±2.0
Y	Horizontal pin no. 1 center to lateral pin center	0.075	3.0	±0.05	±2.0
ZA1	Horizontal pin no. 1 center to first set of antenna GND pins pin center	10.0	393.7	±0.05	±2.0
ZA2	Horizontal pin no. 1 center to second set of antenna GND pins pin center	12.55	494.1	±0.05	±2.0
ZB	Vertical pin no.1 center to antenna GND pin center	0.225	8.9	±0.05	±2.0
ZL	Antenna GND pin width and length	0.70	27.6	±0.05	±2.0
	Module weight [g]	<1.0			

Table 22: NINA-B4x6 mechanical outline data

6 Qualification and approvals

⚠ Approvals are pending.
The NINA-B4 series modules are in development status as mentioned in the table on page 2. Hence, the information in this section will be valid and available only when the module is fully tested and approved in the Initial Production stage.

6.1 Country approvals

The NINA-B4x0 and NINA-B4x6 modules are certified for use in the following countries/regions:

Country/region	NINA-B4x0	NINA-B4x6
Europe	Pending	Pending
USA	Pending	Pending
Canada	Pending	Pending
Japan	Pending	Pending
Taiwan	Pending	Pending
South Korea	Pending	Pending
Brazil	Pending	Pending
Australia	Pending	Pending
New Zealand	Pending	Pending
South Africa	Pending	Pending

☞ See the Regulatory information application note [7] for detailed information about the regulatory requirements that must be met when using NINA-B4 modules in an end product.

6.2 Bluetooth qualification

The NINA-B4 module series will be qualified as an end product according to the Bluetooth 5.1 specification.

Product type	QD ID	Listing Date
End product	TBD	TBD

Table 23: NINA-B4 series Bluetooth qualified design ID

7 Antennas

See the Regulatory information application note [7] for information of approved antennas.

8 Product handling

8.1 Packaging

The NINA-B4 series modules are delivered as hermetically sealed, reeled tapes to enable efficient production, production lot set-up and tear-down. For more information about packaging, see the u-blox Package Information Guide [1].

8.1.1 Reels

The NINA-B4 modules are deliverable in quantities of 500 pieces on a reel. The reel types for the NINA-B4 modules are provided in Table 24 and detailed information about the reel types are described in the u-blox Package Information Guide [1].

Model	Reel Type
NINA-B4x0	A3
NINA-B4x6	A3

Table 24: Reel types for different models of the NINA-B4 series

8.1.2 Tapes

Figure 11 shows the position and orientation of the NINA-B3 modules representing the NINA-B4 modules as they are delivered on tape.

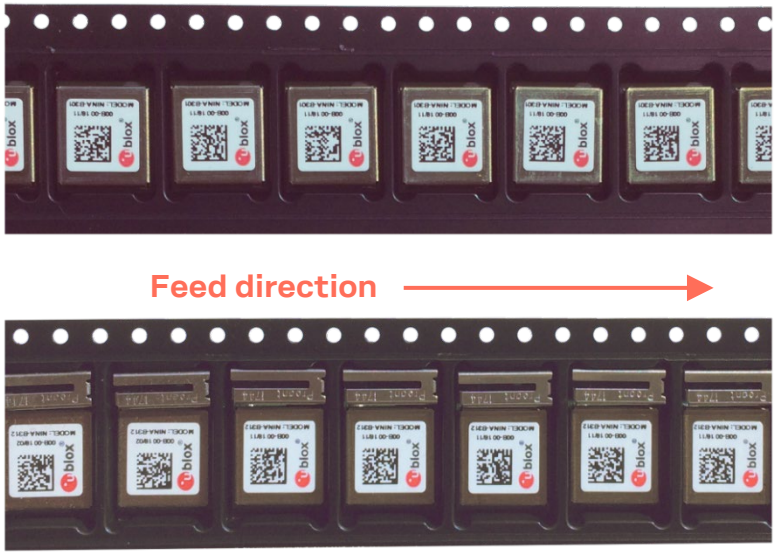


Figure 11: Orientation of NINA-B3 modules on tape representing the same orientation for NINA-B4 modules

8.2 Moisture sensitivity levels

⚠ The NINA-B4 series modules are Moisture Sensitive Devices (MSD) in accordance with the IPC/JEDEC specification.

The Moisture Sensitivity Level (MSL) relates to the required packaging and handling precautions. The NINA-B4 series modules are rated at MSL level 4. For more information regarding moisture sensitivity levels, labeling and storage, see the u-blox Package Information Guide [1].

☞ For MSL standards, see IPC/JEDEC J-STD-020, which can be downloaded from www.jedec.org.

8.3 Reflow soldering

Reflow profiles are selected according to u-blox recommendations. See NINA-B4 series System Integration Manual [3] for more information.

⚠ Failure to follow these recommendations can result in severe damage to the device.

8.4 ESD precautions

⚠ The NINA-B4 series modules contain highly sensitive electronic circuitry and are Electrostatic Sensitive Devices (ESD). Handling the NINA-B4 series modules without proper ESD protection may destroy or damage them permanently.

The NINA-B4 series modules are electrostatic sensitive devices (ESD) and require special ESD precautions typically applied to the ESD sensitive components. Section 4.1.1 provides the maximum ESD ratings of the NINA-B4 series modules.

Proper ESD handling and packaging procedures must be applied throughout the processing, handling and operation of any application that incorporates the NINA-B4 series module. Failure to observe these recommendations can result in severe damage to the device.

9 Labeling and ordering information

9.1 Product labeling

The labels of the NINA-B4 series modules include important product information as described in this section.

Figure 13 illustrates the label of the NINA-B4 series modules, which includes the u-blox logo, production lot, product type number, and certification numbers (if applicable).

Figure 13: Location of product type number on the NINA-B4 series module label

Reference	Description
1	Date of unit production (year/week)
2	Product version
3	Product name
4	Data Matrix with unique serial number of 19 alphanumeric symbols. The first 3 symbols represent module type number unique to each module variant, the next 12 symbols represent the unique hexadecimal Bluetooth address of the module AABBCCDDEEFF, and the last 4 symbols represent the hardware and firmware version encoded HHFF.

Table 25: NINA-B4 series label description

9.2 Explanation of codes

Three different product code formats are used. The **Product Name** is used in documentation such as this data sheet and identifies all u-blox products, independent of packaging and quality grade. The **Ordering Code** includes options and quality, while the **Type Number** includes the hardware and software versions. Table 26 below details these three different formats:

Format	Structure
Product Name	PPPP-TGVV
Ordering Code	PPPP -TGVV-TTQ
Type Number	PPPP -TGVV-TTQ-XX

Table 26: Product code formats

Table 27 explains the parts of the product code.

Code	Meaning	Example
PPPP	Form factor	NINA
TG	Platform (Technology and Generation) T – Dominant technology, for example, W: Wi-Fi, B: Bluetooth G - Generation	B4: Bluetooth Generation 4
VV	Variant based on the same platform; range [00…99]	11: default configuration, with antenna pin
TT	Major product version	00: first revision
Q	Quality grade A: Automotive B: Professional C: Standard	B: professional grade
XX	Minor product version (not relevant for certification)	Default value is 00

Table 27: Part identification code

9.3 Ordering information

Ordering Code	Product
NINA-B400-00B	NINA-B4 module with antenna connector U.FL, open CPU for custom applications
NINA-B406-00B	NINA-B4 module with internal PCB antenna, open CPU for custom applications
NINA-B410-00B	NINA-B4 module with antenna connector U.FL, pre-flashed with software version 1.0.0 and locked for use with u-connectXpress
NINA-B416-00B	NINA-B4 module with internal PCB antenna, pre-flashed with software version 1.0.0 and locked for use with u-connectXpress

Table 28: Product ordering codes

Appendix

A Glossary

Abbreviation	Definition
ADC	Analog to Digital Converter
Bluetooth LE	Bluetooth low energy
BPF	Band Pass Filter
CTS	Clear To Send
EDM	Extended Data mode
ESD	Electro Static Discharge
FCC	Federal Communications Commission
GATT	Generic ATTribute profile
GPIO	General Purpose Input/Output
IC	Industry Canada
I^2C	Inter-Integrated Circuit
MCU	Micro Controller Unit
MSD	Moisture Sensitive Device
RTS	Request To Send
SPI	Serial Peripheral Interface
TBD	To be Defined
UART	Universal Asynchronous Receiver/Transmitter

Table 29: Explanation of the abbreviations and terms used

Related documents

[1] u-blox Package Information Guide, document number UBX-14001652
[2] u-blox Short Range AT Commands Manual, document number UBX-14044127
[3] NINA-B4 System Integration Manual, document number UBX-19052230
[4] u-connectXpress software User guide, document number UBX-16024251
[5] NINA-B4 Product Summary, document number UBX-19047297
[6] NINA-B3 Data sheet, document number UBX-17052099
[7] Regulatory information application note, document number TBD

For regular updates to u-blox documentation and to receive product change notifications, register on our homepage (www.u-blox.com).

Revision history

Revision	Date	Name	Comments
R01	17-Dec-2019	hekf	Initial release.
R02	25-Mar-2020	asoh, hisa, hekf	Updated NINA-B400 status from “In Development” to “Prototype”. GPIO pins updated to 38. EIRP value updated to 10 dBm.

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