

# JLHF4MR120RD3E7DN

LD3 Half-Bridge Module with SiC Trench MOSFET

#### **Features**

- · Electrical features
  - Silicon Carbide MOSFET
  - Maximum junction temperature 175°C
  - Low Inductive Layout
  - High current density
  - Low switching losses
- Mechanical features
  - Package with CTI >200
  - Solderable Pins
  - Isolated copper baseplate using AMB technology



### LD3 Pack

#### MARKING DIAGRAM



### **Typical Applications**

- EV Chargers
- Industrial Automation & Testing
- Solar

JINLAN = Company Name

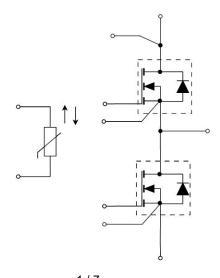
JLHF4MR120RD3E7DN = Specific Device Code

YYWW = Year and Work Week Code

XXXXX = Serial Number

QR code = Custom Assembly Information

### **Description**





# Package Insulation coordination

Parameter	Symbol	Note or test condition	Values	Unit
Isolation test voltage	V <sub>ISOL</sub>	RMS,f=50Hz,t=60s	4.0	kV
Internal isolation		basic insulation(class 1,IEC 61140)	Si <sub>3</sub> N <sub>4</sub>	
Comparative tracking index (electrical)	СТІ		>200	
RTI Elec.	RTI	housing	140	${\mathbb C}$

# Package Characteristic values

		Note and an allet an		Values			
Parameter	Parameter Symbol Note or test condition		Min.	Тур.	Max.	Unit	
Stray Inductance	L <sub>CE</sub>				20		nH
Module Lead Resistance, Terminal to Chip	R <sub>cc'+EE'</sub>	T <sub>C</sub> =25°C, per swi	tch		0.80		mΩ
Storage Temperature Range	T <sub>STG</sub>			-40		125	$^{\circ}$
М	Mounting torque for module mounting	-Mounting according to valid application note	M5, Screw	3.0		6.0	Nm
М	Terminal connection torque	-Mounting according to valid application note	M6, Screw	2.5		5.0	Nm
Weight	G				340	I	g



# **SIC MOSFET**

### **Absolute Maximum Ratings** (Tc = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Value	Unit
V <sub>DSS</sub>	Drain-source voltage	T <sub>vj</sub> =25℃	1200	٧
I <sub>DN</sub>	Implemented drain current	V <sub>GS</sub> =18V T <sub>c</sub> = 25℃	450	Α
I <sub>DDC</sub>	Continuous DC drain current	Collector Current @T <sub>vl</sub> =175℃,V <sub>GS</sub> =18V,T <sub>c</sub> =65℃	400	Α
I <sub>DRM</sub>	Repetitive peak drain current	verified by design, $t_p$ limited by $T_{v_jmax}$	900	Α
V <sub>GS max</sub>	Gate-source voltage, max. transient voltage	AC (f >1Hz)	-8 / +21	٧
V <sub>GS OP</sub>	Gate-source voltage, max.static voltage (Recommended)		-3 / +18	V

### Characteristics (Tc = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Тур	Max	Unit
	Drain acurae en resistante	V <sub>GS</sub> = 18 V, I <sub>DN</sub> =400A, T <sub>vj</sub> = 25°C		2.65		mΩ
R <sub>DS(on)</sub> Drain-source on-resistance		V <sub>GS</sub> = 18 V, I <sub>DN</sub> = 400 A, T <sub>vj</sub> =150°C		3.45		11122
V <sub>GS(TH)</sub>	Gate Threshold Voltage	VGS = VDS, ID =100 mA,T <sub>vj</sub> = 25°C	2.0		3.0	V
I <sub>DSS</sub>	Drain-Source Leakage Current	V <sub>GS</sub> = -3V, V <sub>DS</sub> =1200V		30	100	μA
less	Gate-Source Leakage Current	V <sub>GS</sub> = -4V, V <sub>DS</sub> = 0V		4	<del>100</del> -	nA
I <sub>GSS</sub>	Gate-Source Leakage Current	$V_{GS}$ = $+18V$ , $V_{DS}$ = $0V$		1	100	nA
R <sub>Gint</sub>	Internal Gate Resistance	f=1 MHz		1.1		Ω
C <sub>ISS</sub>	Input Capacitance			27.2		pF
Coss	Output capacitance	V <sub>GS</sub> = 0 V, f = 100kHz, V <sub>DS</sub> = 800V		1.76		pF
C <sub>RSS</sub>	Reverse Transfer Capacitance	VGS - 0 V, 1 - 100M 12, VDS - 000V		95.2		pF
Q <sub>G</sub>	Total Gate Charge	V <sub>GS</sub> = -3/18 V, V <sub>DS</sub> = 800 V, I <sub>DS</sub> = 400 A		304.8		nC
td(on)	Turn-On Delay Time			102.4		
tr	Rise Time	T <sub>J</sub> = 25°C		180		ne
td(off)	Turn-off Delay Time	$V_{GS} = -5/15V$ , $V_{DS} = 600 V$ , $I_{DS} = 400 A$ , $R_{Gon} = 4.7 \Omega$ ,		223.2		ns
tf	Fall Time	$R_{Goff} = 4.7\Omega$ Inductive load		77.6		
Eon	Turn-On Switching Loss per Pulse	muuciive loau		12.8		mJ
Eoff	Turn Off Switching Loss per Pulse			20		1110
td(on)	Turn-On Delay Time			TBD		
tr	Rise Time	T 450°0		TBD		
td(off)	Turn-off Delay Time	$T_J = 150$ °C $V_{GS} = -5/15V$ , $V_{DS} = 600$ V,		TBD		ns
tf	Fall Time	$I_{DS} = 400 \text{ A}, R_{Gon} = 4.7\Omega,$ $R_{Goff} = 4.7\Omega$		TBD		
Eon	Turn-On Switching Loss per Pulse	Inductive load		TBD		
Eoff	Turn Off Switching Loss per Pulse			TBD		- mJ
RthJC	Thermal resistance	Junction-to-Case (per MOS)		0.104		K/W
T <sub>vj op</sub>		Temperature under switching conditions	-40		175 <sup>1)</sup>	°C

<sup>1)</sup>  $T_{vj\,op}$  > 175  $^\circ\!\mathbb{C}$  is only allowed for operation at overload conditions.



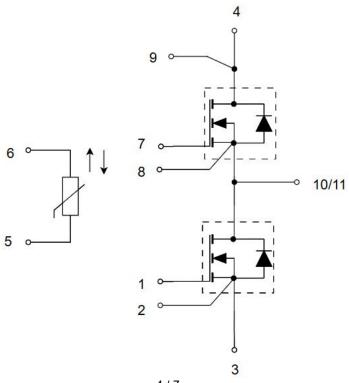
### Reverse Diode Characteristics (Tc=25°C unless otherwise noted)

Cumbal	Dovomatov	Took Condition		Value			Linit
Symbol Parameter		Test Condition		Min	Тур	Max	Unit
.,	Die de Fernand Velte ne	VOD 0V 1 000A	T <sub>v</sub> j = 25 °C		4.7		V
V <sub>SD</sub>	Diode Forward Voltage	VGS= -3V, I <sub>SD</sub> = 200A	T <sub>v</sub> j = 150 °C		4.3		V

## **NTC Characteristics**

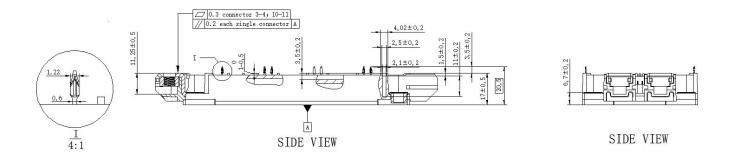
Symbol	Parameter	Note or Test Condition	Value			Unit
Syllibol	Farameter	Parameter Note of Test Condition	Min	Тур	Max	UIIIL
R <sub>25</sub>	Rated Resistance	T <sub>C</sub> = 25°C		5		kΩ
ΔR/R	Deviation of R100	T <sub>C</sub> =100 ℃,R <sub>100</sub> =493Ω	-5		5	%
P <sub>25</sub>	Power Dissipation	T <sub>C</sub> = 25°C			20	mW
B <sub>25/50</sub>	B-value	R <sub>2</sub> =R <sub>25</sub> exp[B <sub>25/50</sub> (1/T <sub>2</sub> - 1/(298.15K))]		3375		К
B <sub>25/80</sub>	B-value	R <sub>2</sub> =R <sub>25</sub> exp[B <sub>25/80</sub> (1/T <sub>2</sub> - 1/(298.15K))]		3411		К
B <sub>25/100</sub>	B-value	$R_2=R_{25} \exp[B_{25/100}(1/T_2-1/(298.15K))]$		3433		К

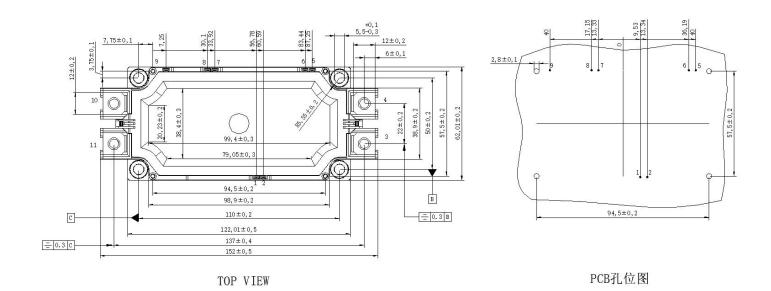
### **CIRCUIT DIAGRAM**





### **PACKAGE DIMENSION**







### **REVISION HISTORY**

Document version	Date of release	Description of changes
Rev.00	2025-05-27	Preliminary Data



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