

Features

- 2.5V to 5.5V Input Voltage
- Adjust Output Voltage Range Up to 30V
- 1.23V Feedback Voltage
- 1.2MHz Fixed Switching Frequency
- 1.4A Switch Peak Current Limit
- Internal Compensation
- Thermal Shutdown Protection
- Over Voltage Protection
- -40°C to 125°C Operating Junction Temperature
- Available in SOT23-5 package

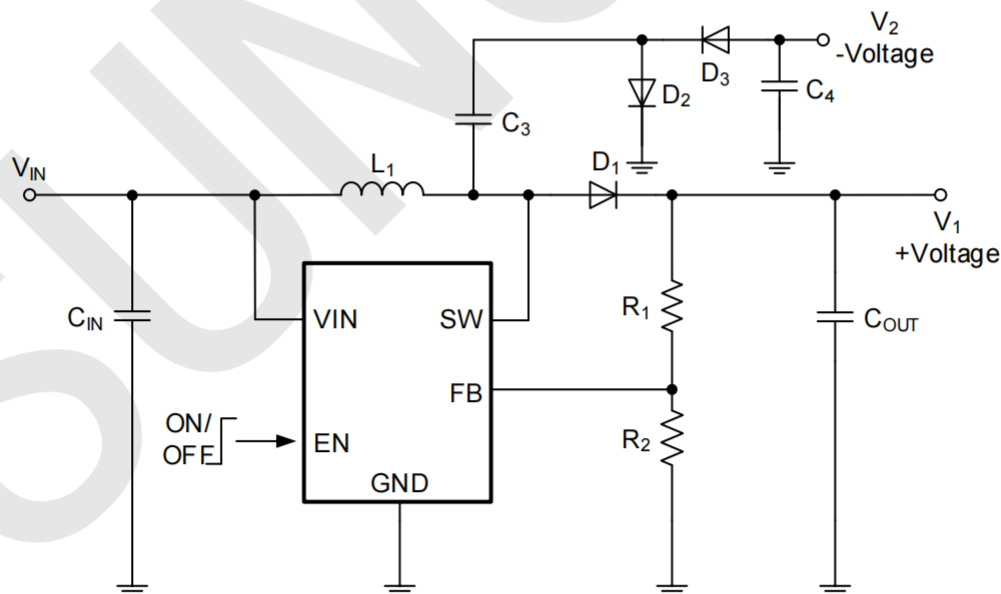
Applications

- LCD Bias Supply
- Digital still cameras
- White-LED Supply for LCD Backlights
- PDAs, Organizers, and Handheld PCs

General Description

The TPS61040 is a high-frequency boost converter dedicated for small to medium LCD bias supply. The device is ideal to generate output voltages up to 30V from a dual-cell NiMH/NiCd or a single-cell Li-Ion battery. The part can also be used to generate standard 3.3V or 5V to 12V power conversions. Optimized operation frequency can meet the requirement of small LC filters value and low operation current with high efficiency. Internal soft start function can reduce the inrush current. The device has a 1.4A switch current limit, offering lower output voltage ripple and allows the use of a smaller form factor inductor for lower power applications. Low quiescent current allows device operation at very high efficiencies over the entire load current range. The TPS61040 is available in SOT23-5 package.

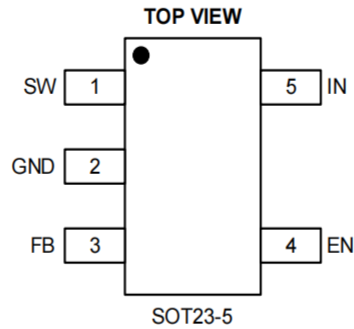
Typical Application Circuit



Typical Positive and Negative Output LCD Bias Supply Circuit

Package and Pin Description

Pin Configuration



Pin Description

Pin	Name	Function
1	SW	Power Switch Output. SW is the drain of the internal MOSFET switch. Connect the power inductor and output rectifier to SW. SW can swing between GND and 30V.
2	GND	Ground Pin.
3	FB	Feedback Input. The FB voltage is 1.23V. Connect a resistor divider to FB.
4	EN	EN pin of the boost converter. It is a multi-functional pin which can be used for enable control and PWM dimming. Should not be left floating.
5	IN	Input Supply Pin. Must be locally bypassed.

Order Information ⁽¹⁾

Marking	Part No.	Model	Description	Package	T/R Qty
KFYLL	00090005	TPS61040DBVR	TPS61040DBVR Bias Driver, V_{IN} 2.5-5.5V, V_{OUT} 30V, 1.2MHz, VFB 1.23V, SOT23-5	SOT23-5	3000PCS

Note (1): All SUNGOOD parts are Pb-Free and adhere to the RoHS directive.

Specifications

Absolute Maximum Ratings ^{(1) (2)}

Item	Min	Max	Unit
V _{IN} , V _{EN} voltage	-0.3	6	V
V _{SW} voltage	-0.3	32	V
V _{SW} voltage (10ns transient)	-5	33	V
All Other Pins	-0.3	6	V
Power dissipation ⁽³⁾	Internally Limited		
Operating junction temperature, T _J	-40	150	°C
Storage temperature, T _{stg}	-65	150	°C
Lead Temperature (Soldering, 10sec.)		260	°C

Note (1): Exceeding these ratings may damage the device.

Note (2): The device is not guaranteed to function outside of its operating conditions.

Note (3): The maximum allowable power dissipation is a function of the maximum junction temperature, T_{J(MAX)}, the junction-to-ambient thermal resistance, R_{θJA}, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is calculated using: P_{D(MAX)} = (T_{J(MAX)} - T_A)/R_{θJA}. Exceeding the maximum allowable power dissipation causes excessive die temperature, and the regulator goes into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J=160°C (typical) and disengages at T_J= 130°C (typical).

ESD Ratings

Item	Description	Value	Unit
V _(ESD-HBM)	Human Body Model (HBM) ANSI/ESDA/JEDEC JS-001-2014 Classification, Class: 2	±2000	V
V _(ESD-CDM)	Charged Device Mode (CDM) ANSI/ESDA/JEDEC JS-002-2014 Classification, Class: C0b	±200	V
I _{LATCH-UP}	JEDEC STANDARD NO.78E APRIL 2016 Temperature Classification, Class: I	±150	mA

Recommended Operating Conditions

Item	Min	Max	Unit
Operating junction temperature ⁽¹⁾	-40	125	°C
Operating temperature range	-40	85	°C
Input voltage V _{IN}	2.5	5.5	V
Output voltage V _{OUT}	V _{IN}	28	V

Note (1): All limits specified at room temperature (T_A = 25°C) unless otherwise specified. All room temperature limits are 100% production tested. All limits at temperature extremes are ensured through correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).

Thermal Information

Item	Description	Value	Unit
$R_{\theta JA}$	Junction-to-ambient thermal resistance ⁽¹⁾⁽²⁾	180	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	130	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	45	°C/W
ψ_{JT}	Junction-to-top characterization parameter	35	°C/W
ψ_{JB}	Junction-to-board characterization parameter	45	°C/W

Note (1): The package thermal impedance is calculated in accordance to JESD 51-7.

Note (2): Thermal Resistances were simulated on a 4-layer, JEDEC board

Electrical Characteristics ^{(1) (2)}

$V_{IN}=5V$, $T_A=25^{\circ}C$, unless otherwise specified.

Parameter	Test Conditions	Min	Typ.	Max	Unit
Input voltage range		2.5		5.5	V
Output voltage range		V_{IN}		28	V
Supply Current (Quiescent)	$V_{FB}=110\%$		150	300	μA
Supply Current (Shutdown)	$V_{EN}=0$ or $EN=GND$		0.1	1	μA
Feedback Voltage		1.20	1.23	1.26	V
SW On Resistance			400	650	m Ω
Current Limit			1.4		A
Output Over Voltage Protection Threshold			30		V
Switching Frequency			1.2		MHz
Maximum Duty Cycle	$V_{FB}=90\%$		90		%
Minimum On-Time			80		ns
EN Rising Threshold		1.2			V
EN Falling Threshold				0.7	V
Under-Voltage Lockout Threshold	Wake up V_{IN} Voltage		2.1	2.3	V
	Shutdown V_{IN} Voltage	1.7	1.9		V
	Hysteresis V_{IN} voltage		300		mV
Soft Start			600		μS
Thermal Shutdown			160		°C
Thermal Hysteresis			30		°C

Note (1): MOSFET on-resistance specifications are guaranteed by correlation to wafer level measurements.

Note (2): Thermal shutdown specifications are guaranteed by correlation to the design and characteristics analysis.

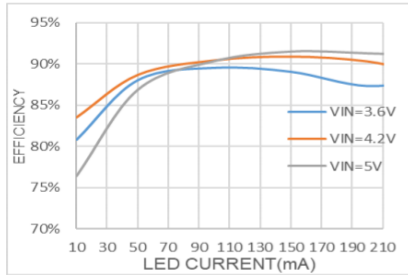
Typical Performance Characteristics (1) (2)

Note (1): Performance waveforms are tested on the evaluation board.

Note (2): $V_{IN}=5V$, $V_{OUT}=12V$, $T_A = +25^{\circ}C$, unless otherwise noted.

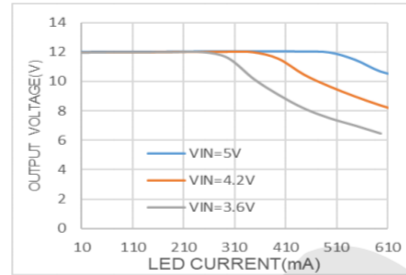
Efficiency vs. Load Current

$V_{OUT}=12V$



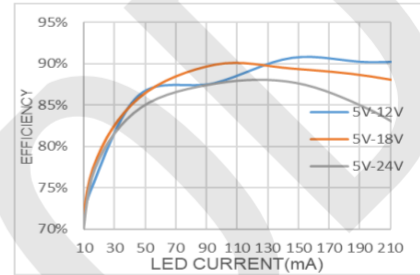
Load Regulation

$V_{OUT}=12V$



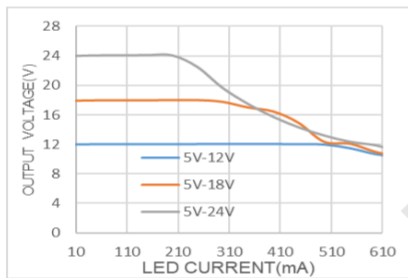
Efficiency vs. Load Current

$V_{OUT}=12V/18V/24V$



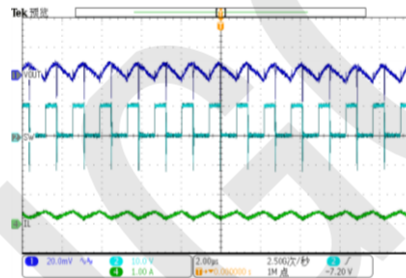
Load Regulation

$V_{OUT}=12V/18V/24V$



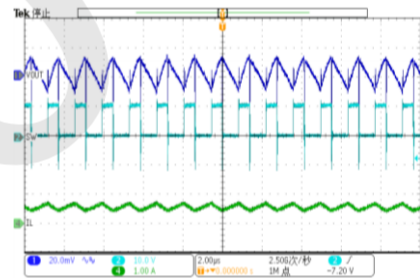
Output Ripple Voltage

$V_{IN}=5V$, $V_{OUT}=12V$, $I_{OUT}=100mA$



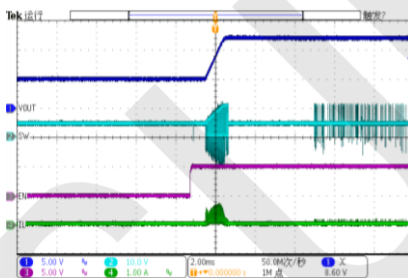
Output Ripple Voltage

$V_{IN}=5V$, $V_{OUT}=12V$, $I_{OUT}=200mA$



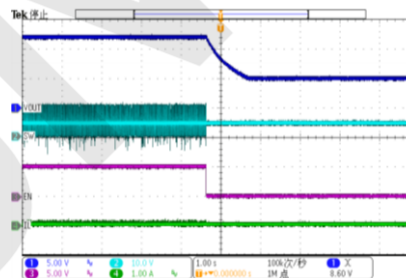
Enable Startup at No Load

$V_{IN}=5V$, $V_{OUT}=12V$



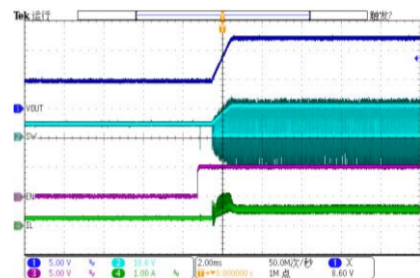
Enable Shutdown at No Load

$V_{IN}=5V$, $V_{OUT}=12V$



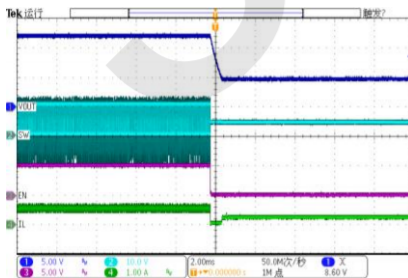
Enable Startup at Heavy Load

$V_{IN}=5V$, $V_{OUT}=12V$, $I_{OUT}=200mA$



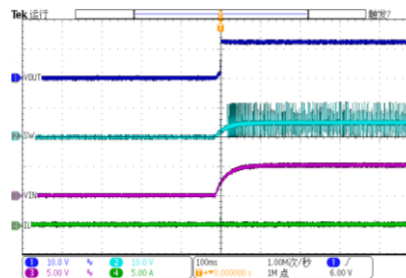
Enable Shutdown at Heavy Load

$V_{IN}=5V$, $V_{OUT}=12V$, $I_{OUT}=200mA$



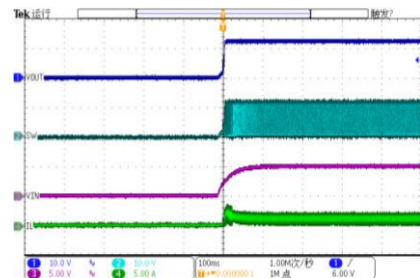
Power Up at No Load

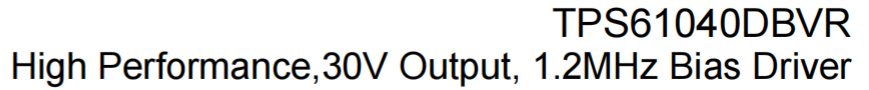
$V_{IN}=5V$, $V_{OUT}=12V$, $I_{OUT}=0A$



Power Up at Heavy Load

$V_{IN}=5V$, $V_{OUT}=12V$, $I_{OUT}=200mA$





The diagram illustrates the internal components of a Buck-Boost converter. Key blocks include:

- Current Bias** and **BandGap**: Provide reference signals i_{bias} and V_{REF} .
- Protection Circuit**: Contains **OVP** (Over-Voltage Protection) and **UVLO** (Under-Voltage Lockout) blocks.
- 1MHz OSC**: Provides a clock signal to the **PWM Logic**.
- OCF 600mA**: Over-Current Foldback block.
- PWM Logic**: Generates the PWM signal for the MOSFET driver.
- Buffer**: A MOSFET driver stage.
- Soft Start**: Controls the ramp-up of the output voltage.
- Feedback Loop**: Consists of an error amplifier (op-amp) and a voltage divider. The error amplifier compares the feedback voltage (FB) with V_{REF} . The output of the error amplifier drives the MOSFET gate.

Functions Description

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. UVLO protection monitors the internal regulator voltage. When the voltage is lower than UVLO threshold voltage, the device is shut off. When the voltage is higher than UVLO threshold voltage, the device is enabled again.

When the input voltage is above maximal UVLO rising threshold and the EN pin is pulled high, the TPS61040 is enabled. When the EN pin is pulled low, the TPS61040 goes into shutdown mode. In shutdown mode, less than 1 μA input current is consumed. Because there is a conductive path from the input to the output through the inductor and Schottky diode, the output voltage is equal to the input voltage during shutdown. The enable pin needs to be terminated and should not be left floating.

All inductive step-up converters exhibit high inrush current during start-up if no special precaution is made. This can cause voltage drops at the input rail during start up and may result in an unwanted or early system shut down. An internal soft start circuit limits the peak inductor current according to the output voltage. The switching soft start phase is about 600 μ s typically. The soft start function reduces the inrush current during startup.

Over-Voltage Protection

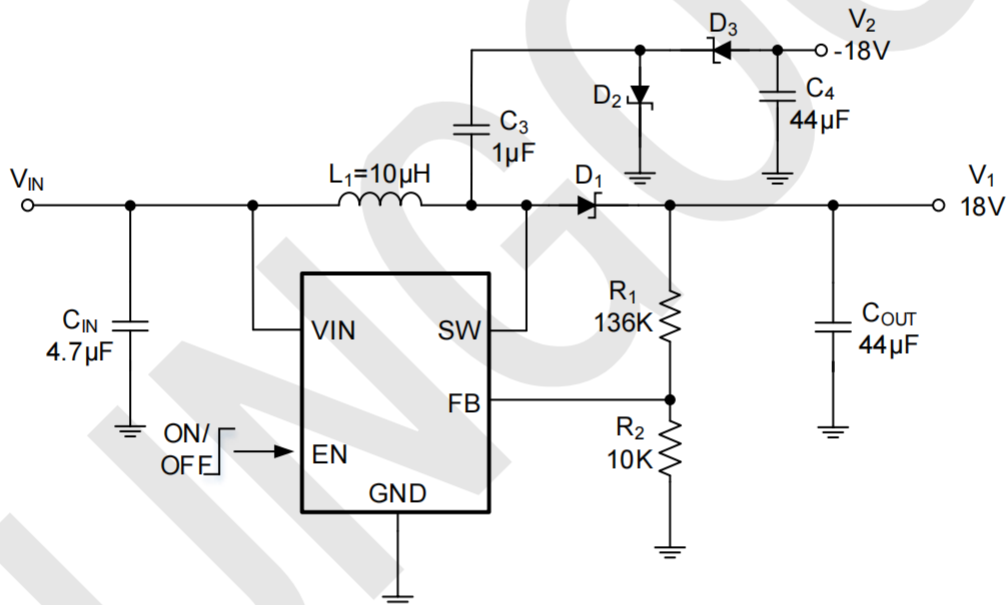
As with any current source, the output voltage rises when the output gets high impedance or disconnected. To prevent the output voltage exceeding the maximum switch voltage rating of the main switch, an overvoltage protection circuit is integrated. As soon as the output voltage exceeds the OVP threshold, the converter stops switching and the output voltage falls.

Thermal Shutdown

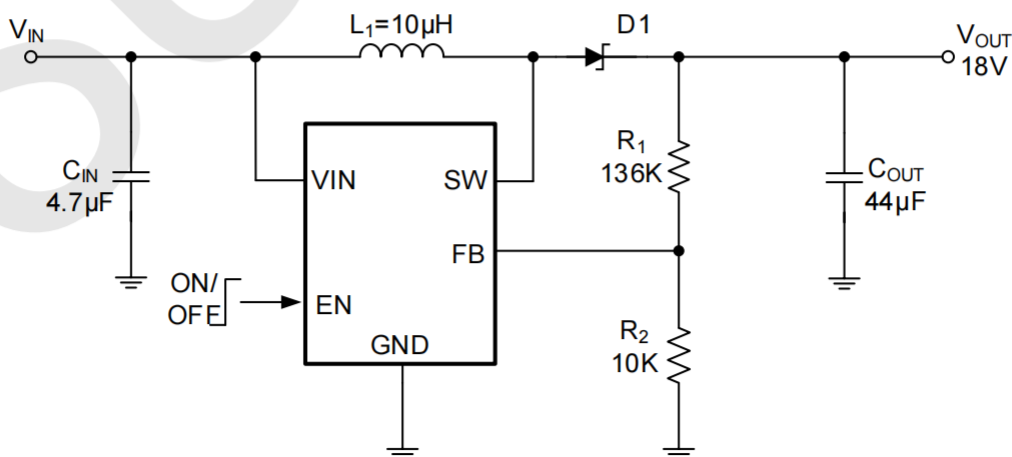
Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds 160°C, it shuts down the whole chip. When the temperature falls below its lower threshold (Typ. 130°C) the chip is enabled again.

Applications Information

Typical Application



Positive and Negative Output LCD Bias Supply Circuit



Boost Application Circuit

Setting the Output Voltage

The output voltage can be programmed by resistor divider, as shown in Equation:

$$V_{OUT} = 1.23V \times \left(1 + \frac{R1}{R2}\right)$$

Inductor Selection

The recommended value of inductor for most applications are 4.7 to 22μH. Small size and better efficiency are the major concerns for portable device, such as TPS61040 used for mobile phone. When selecting the inductor, the inductor saturation current should be rated as high as the peak inductor current at maximum load, and respectively, maximum LED current.

The inductor value determines the maximum switching frequency of the converter. Therefore, select the inductor value that ensures the maximum switching frequency at the converter maximum load current is not exceeded. The maximum switching frequency is calculated by the following formula:

$$f_{S(MAX)} = \frac{V_{IN(min)} \times (V_{OUT} - V_{IN})}{I_P \times L \times V_{OUT}}$$

Where:

I_P = Peak current.

L = Selected inductor value.

$V_{IN(min)}$ = The highest switching frequency occurs at the minimum input voltage.

If the selected inductor value does not exceed the maximum switching frequency of the converter, the next step is to calculate the switching frequency at the nominal load current using the following formula:

$$f_S(I_{load}) = \frac{2 \times I_{load} \times (V_{OUT} - V_{IN} + V_d)}{I_P^2 \times L}$$

Where:

I_P = Peak current.

L = Selected inductor value.

I_{load} = Nominal load current.

V_d = Rectifier diode forward voltage.

A smaller inductor value gives a higher converter switching frequency, but lowers the efficiency.

The inductor value has less effect on the maximum available load current and is only of secondary order. The best way to calculate the maximum available load current under certain operating conditions is to estimate the expected converter efficiency at the maximum load current.

$$I_{load(max)} = \eta \frac{I_P^2 \times L \times f_{S(max)}}{2 \times (V_{OUT} - V_{IN})}$$

Where:

I_P = Peak current.

L = Selected inductor value.

$f_{S(max)}$ = Maximum switching frequency as calculated previously.

η = Expected converter efficiency.

The selected inductor should have a saturation current that meets the maximum peak current of the converter. Another important inductor parameter is the dc resistance. The lower the dc resistance, the higher the efficiency of the converter.

Output Capacitor Selection

The device is designed to operate with a wide selection of ceramic output capacitors. The selection of the output capacitor value is a trade-off between output voltage ripple and capacitor cost and form factor. In general, capacitor values of 10 μ F up to 44 μ F can be used. For better voltage filtering, ceramic capacitors with low ESR are recommended. X5R and X7R types are suitable because of their wider voltage and temperature ranges.

Input Capacitor Selection

For good input voltage filtering, low ESR ceramic capacitors are recommended. A 4.7 μ F ceramic input capacitor is sufficient for most of the applications. For better input voltage filtering and EMI reduction, this value can be increased. The input capacitor should be placed as close as possible to the input pin of the converter.

Diode Selection

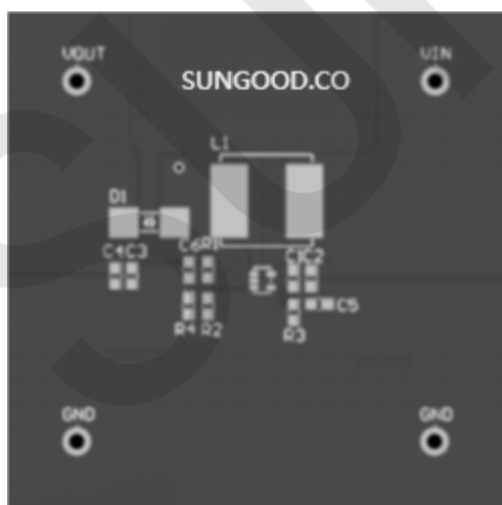
A Schottky diode should be used for the output diode. The forward current rating of the diode should be higher than the load current, and the reverse voltage rating must be higher than the output voltage. Do not use ordinary rectifier diodes, since slow switching speeds and long recovery times cause the efficiency and the load regulation to suffer.

Layout Guidelines

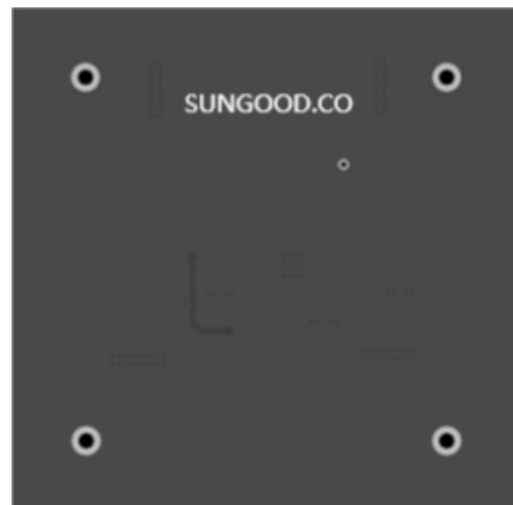
For best performance of the TPS61040, the following guidelines must be strictly followed.

1. Input and Output capacitors should be placed close to the IC and connected to ground plane to reduce noise coupling.
2. The GND should be connected to a strong ground plane for heat sinking and noise protection.
3. Keep the main current traces as possible as short and wide.
4. SW node of DC-DC converter is with high frequency voltage swing. It should be kept at a small area.
5. Place the feedback components as close as possible to the IC and keep away from the noisy devices.

Top Layer



Bottom Layer

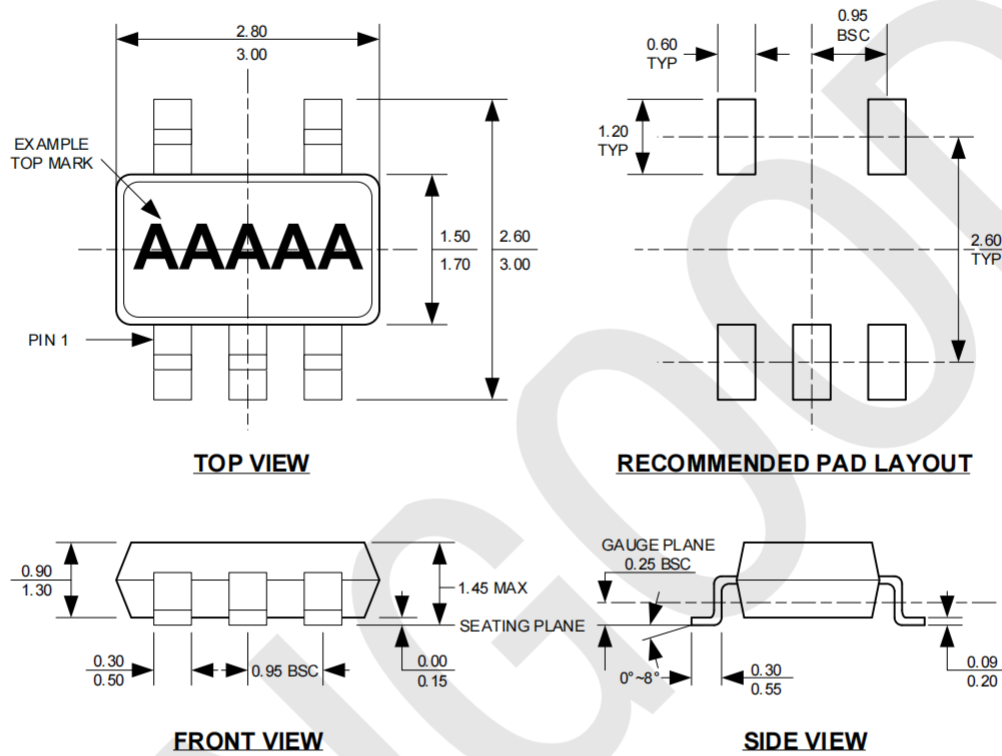


Sample Board Layout



Package Description

SOT23-5



NOTE:

1. CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2. PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3. PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5. DRAWING CONFORMS TO JEDEC MS-012, VARIATION BA.
6. DRAWING IS NOT TO SCALE.