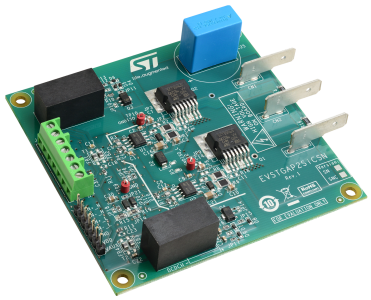
# EVSTGAP2SICSNC

Data brief

## Demonstration board for STGAP2SICSNC isolated 4 A single gate driver



## Features

- **Board**
  - Half bridge configuration, high voltage rail up to 520 V
  - SCTH35N65G2V-7: 650 V, 55 mΩ 2nd generation SiC MOSFET
  - Negative gate driving
  - On board isolated DC-DC converters to supply high-side and low-side gate drivers, fed by VAUX = 5 V, with 5.2 kV maximum isolation
  - VDD logic supplied by on-board generated 3.3 V or VAUX = 5 V
  - Easy jumper selection of driving voltage configuration: +17/0 V; +17/-3 V; +19/0 V; +19/-3 V
- **Device**
  - 1700 V functional isolation
  - Driver current capability: 4 A source/sink @ 25 °C
  - 4 A Miller Clamp
  - Short propagation delay: 75 ns
  - UVLO function
  - Gate driving voltage up to 26 V
  - 3.3 V, 5 V TTL/CMOS inputs with hysteresis
  - Temperature shut down protection
  - Stand-by function

| Product status link |
| --- |
| EVSTGAP2SICSNC |

## Description

The EVSTGAP2SICSNC is a half bridge evaluation board designed to evaluate the STGAP2SICSNC isolated single gate driver.

The gate driver is characterized by 4 A current capability and rail-to-rail outputs, making the device suitable also for high power inverter applications such as motor drivers in industrial applications equipped with SiC power switch.

The configuration featuring single output pin and Miller CLAMP function allow avoiding gate spikes during fast commutations in half-bridge topologies.

The device integrates protection functions: UVLO and thermal shut down are included to easily design high reliability systems. Dual input pins allow choosing the control signal polarity and implementing HW interlocking protection to avoid cross-conduction in case of controller's malfunction.

The device allows implementing negative gate driving, and the onboard isolated DC-DC converters allow working with optimized driving voltage for SiC.

The EVSTGAP2SICSNC board allows evaluating all the STGAP2SICSNC features while driving a half-bridge power stage with voltage rating up to 520 V. It is possible to increase bus voltage by replacing the power switches with appropriate devices in H2PACK-7L or H2PACK-2L package and the C29 capacitance if needed.

The board components are easy to access and modify to make driver performance evaluation easier under different application conditions and fine adjustment of final application components.

# 1 Schematic diagram

Figure 1. **EVSTGAP2SICSNC circuit schematic – gate drivers**

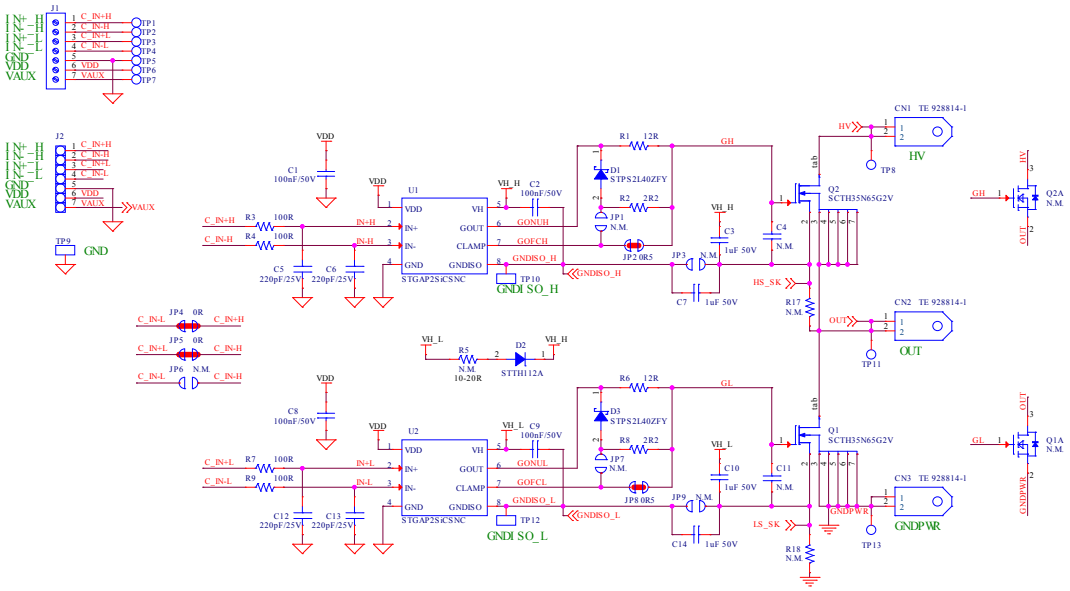
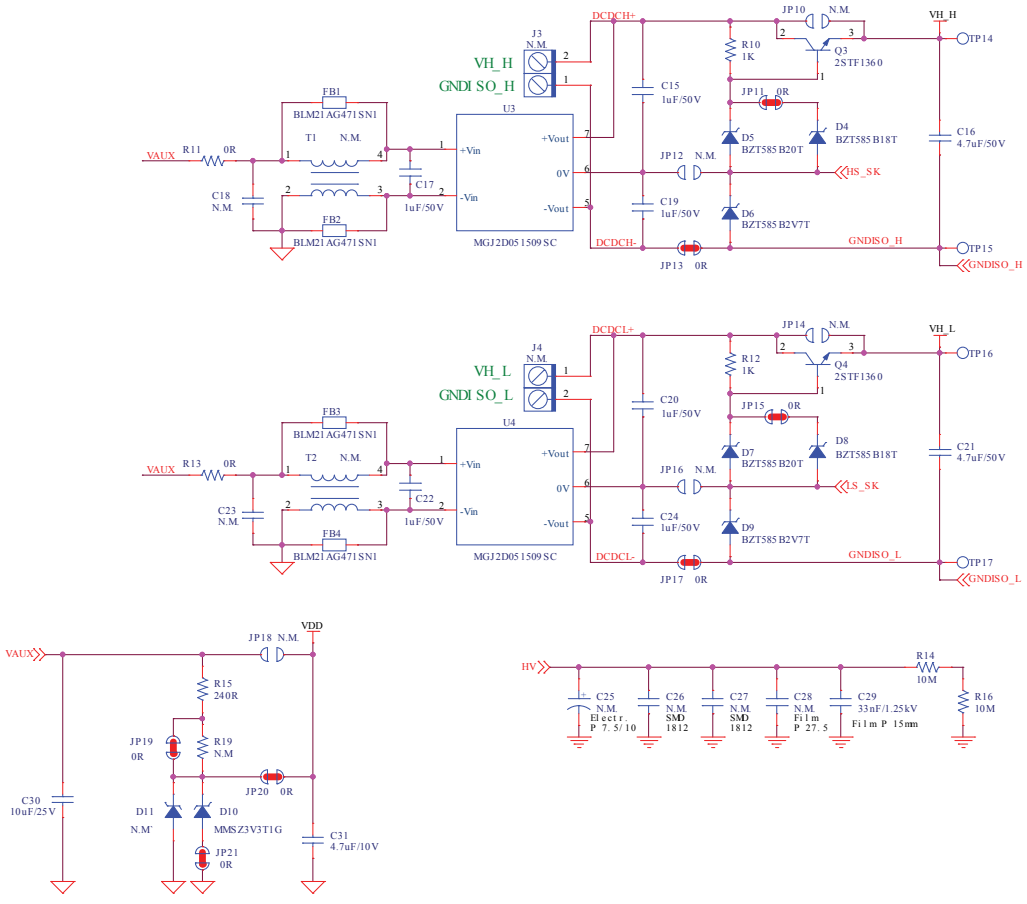


Figure 2. **EVSTGAP2SiCSNC circuit schematic – supply, connectors and decoupling**



# 2 Bill of material

Table 1. **EVSTGAP2SICSNC bill of material**

| Reference | Part Value | Part Description |
|---|---|---|
| CN1, CN2, CN3 | TE 928814-1 | Tab FASTON - Pitch 5.08 mm |
| C1, C2, C8, C9 | 100 nF / 50 V | SMT ceramic capacitor - Size 0603 |
| C3, C7, C10, C14 | 1 µF / 50 V | SMT ceramic capacitor - Size 0805 |
| C4, C11 | N.M. | SMT ceramic capacitor - Size 0805 |
| C5, C6, C12, C13 | 220 pF / 25 V | SMT ceramic capacitor - Size 0603 |
| C15, C17, C19, C20, C22, C24 | 1 µF / 50 V | SMT ceramic capacitor - Size 0603 |
| C16, C21 | 4.7 µF / 50 V | SMT ceramic capacitor - Size 1206 |
| C18, C23 | N.M. | SMT ceramic capacitor - Size 0603 |
| C25 | N.M. | THT electrolytic capacitor - Radial p7.5/10 d22 |
| C26, C27 | N.M. | SMT ceramic capacitor - Size 1812 |
| C28 | N.M. | Film capacitor - Pitch 27.5 mm |
| C29 | 33 nF / 1.25 kV | Film capacitor - Pitch 15 mm |
| C30 | 10 µF / 25 V | SMT ceramic capacitor - Size-0805 |
| C31 | 4.7 µF / 10 V | SMT ceramic capacitor - Size-0603 |
| D1, D3 | STPS2L40ZFY | Schottky rectifier - SOD123Flat |
| D2 | STTH112A | High voltage rectifier - SMA |
| D4, D8 | BZT585B18T | Surface mount precision Zener diode - SOD523 |
| D5, D7 | BZT585B20T | Surface mount precision Zener diode - SOD523 |
| D6, D9 | BZT585B2V7T | Surface mount Zener diode - SOD523 |
| D10 | MMSZ3V3T1G | Zener voltage regulator - SOD123 |
| D11 | N.M. | Zener voltage regulator - SOD123 |
| FB1, FB2, FB3, FB4 | BLM21AG471SN1 | Ferrite beads - Size 0805 |
| JP1, JP7 | OPEN | SMT jumper - Size 0402 |
| JP2, JP8 | 0.5 Ω | SMT resistor - Size 0402 |
| JP3, JP9 | CLOSED | SMT jumper - Size 0402 |
| JP4, JP5, JP11, JP13, JP15, JP17, JP19, JP20, JP21 | CLOSED | SMT jumper - Size 0402 |
| JP6, JP10, JP12, JP14, JP16, JP18 | N.M. | SMT jumper - Size 0402 |
| J1 | MORSV-350-7P_screw | 7 poles, Pitch 3.5 mm |
| J2 | Pin strip | Connector header block T.H. 2 POS 2.54 mm |
| J3, J4 | N.M. | Connector header block T.H. 2 POS 5.08 mm |
| Q1A, Q2A | N.M. | H2PAK-2 |
| Q1, Q2 | SCTH35N65G2V | Silicon carbide power MOSFET, 650V, 55mΩ 45 A - H2PAK-7 |

| Reference | Part Value | Part Description |
|---|---|---|
| Q3, Q4 | 2STF1360 | Low voltage fast-switching NPN power transistor - SOT-89 |
| R1, R6 | 39 Ω | SMT resistor - Size-1210 |
| R2, R8 | 3.3 Ω | SMT resistor - Size-1210 |
| R3, R4, R7, R9 | 100 Ω | SMT resistor - Size-0603 |
| R5 | N.M. | SMT resistor - Size-1206 |
| R10, R12 | 1 kΩ | SMT resistor - Size-0603 |
| R11, R13 | 0 Ω | SMT resistor - Size-0603 |
| R14, R16 | 10 MΩ | SMT resistor - Size-1206 |
| R15 | 240 Ω | SMT resistor - Size-0805 |
| R17, R18 | N.M. | SMT resistor - Size-0603 |
| R19 | N.M. | SMT resistor - Size-0805 |
| TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP11, TP13, TP14, TP15, TP16, TP17 | Test point | Pad test point, SMD |
| TP9, TP10, TP12 | Test point | Loop test point, THT |
| T1, T2 | N.M. | Common mode choke - SMD 4.7x4.5 mm |
| U1, U2 | STGAP2SICSNC | Galvanically isolated gate driver for SiC MOSFETs - SO-8 |
| U3, U4 | MGJ2D051509SC | 5 V to +15/-9 V Isolated DC-DC converter<br>Murata |

# 3 Layout and component placements

Figure 3. **EVSTGAP2SICSNC – Layout (component placement top view)**

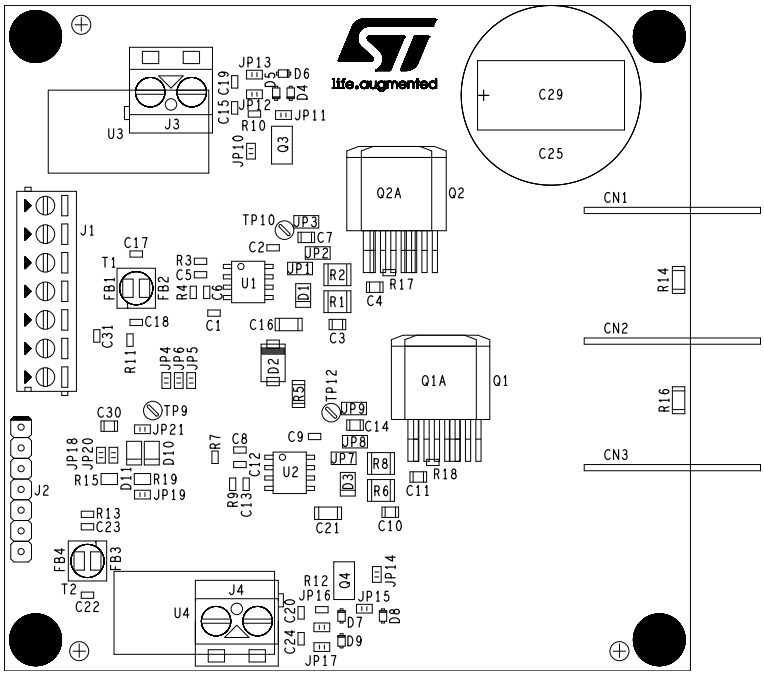



Figure 4. **EVSTGAP2SiCSN – Layout (component placement bottom view)**

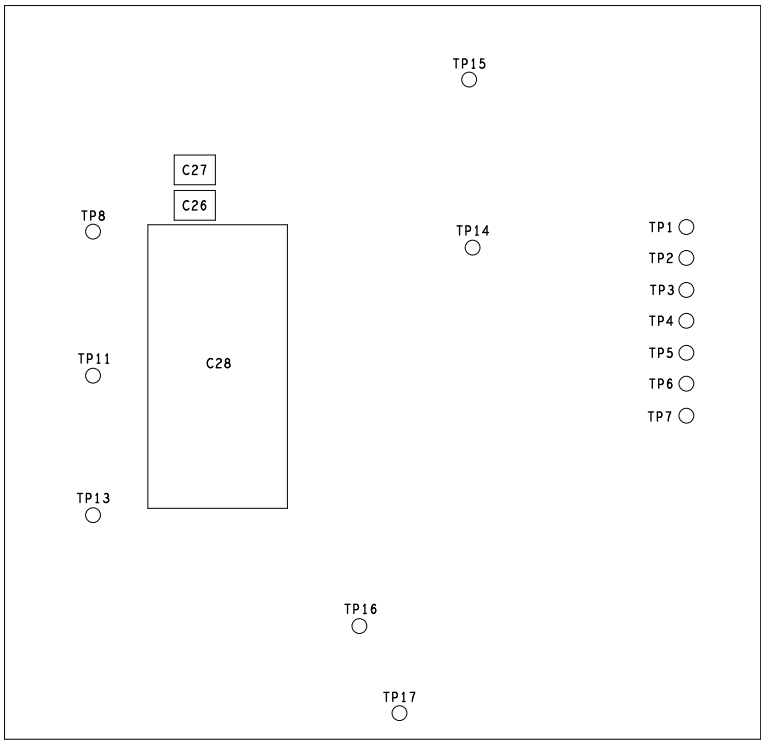


Figure 5. **EVSTGAP2SICSN – Layout (top layer)**

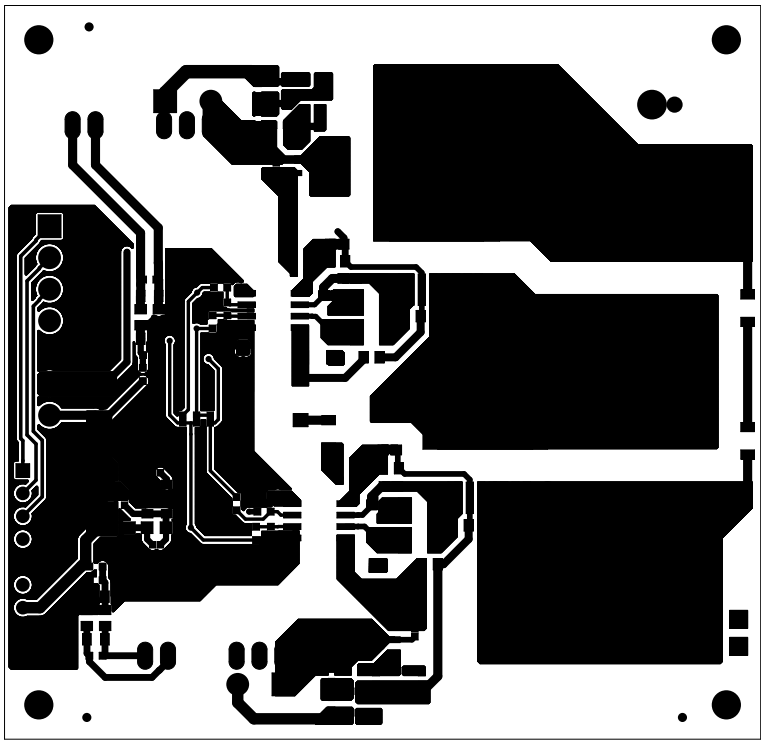
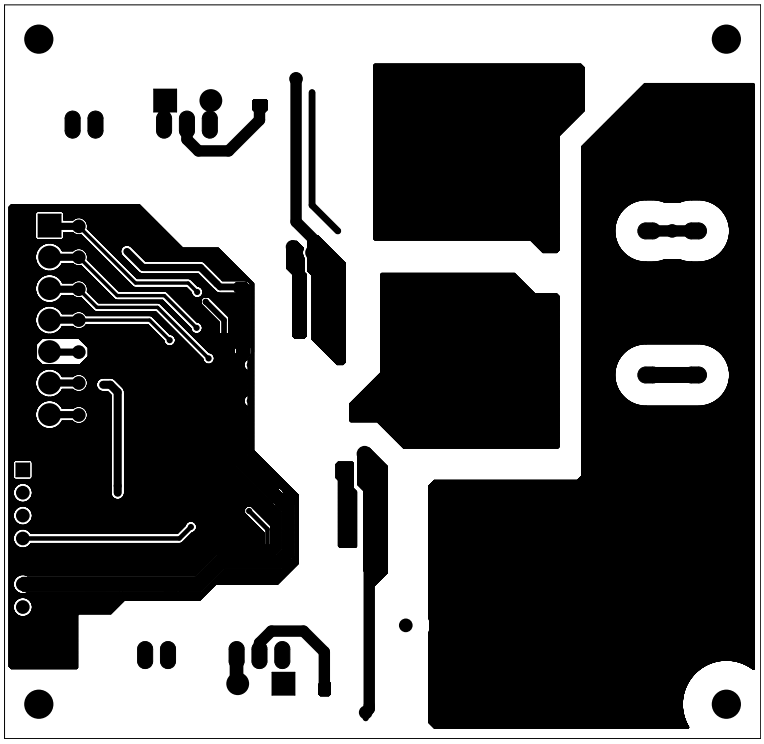


Figure 6. **EVSTGAP2SICSN – Layout (bottom layer)**



## Revision history

Table 2. **Document revision history**

| Date | Version | Changes |
|---|---|---|
| 13-Aug-2021 | 1 | Initial release. |
| 06-Dec-2022 | 2 | Updated Table 1, Figure 1 and Figure 2 |

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