

Product Specification

XBLW SN74LS163

Presettable Synchronous 4-bit
Binary Counter; Synchronous Reset

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Description

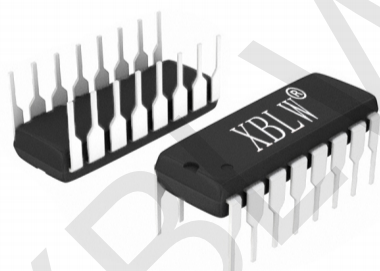
The SN74LS163 is a synchronous presettable binary counter with an internal look-ahead carry. Synchronous operation is provided by having all flip-flops clocked simultaneously on the positive-going edge of the clock (CP). The outputs (Q0 to Q3) of the counters may be preset to a HIGH or LOW. A LOW at the parallel enable input ($\overline{PE}$) disables the counting action. It causes the data at the data inputs (D0 to D3) to be loaded into the counter on the positive-going edge of the clock. Preset takes place regardless of the levels at count enable inputs (CEP and CET). A LOW at the master reset input (MR) sets Q0 to Q3 LOW after the next positive-going transition on the clock input (CP). This action occurs regardless of the levels at input pins $\overline{PE}$, CET and CEP. This synchronous reset feature enables the designer to modify the maximum count with only one external NAND gate. The look-ahead carry simplifies serial cascading of the counters. Both CEP and CET must be HIGH to count. The CET input is fed forward to enable the terminal count output (TC). The TC output thus enabled will produce a HIGH output pulse of a duration approximately equal to a HIGH output of Q0. This pulse can be used to enable the next cascaded stage. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

The CP to TC propagation delay and CEP to CP set-up time determine the maximum clock frequency for the cascaded counters according to the following formula:

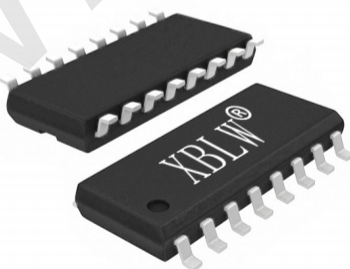
$$f_{\max} = 1 / (t_{p(\max)}(\text{CP to TC}) + t_{su}(\text{CEP to CP}))$$

Features

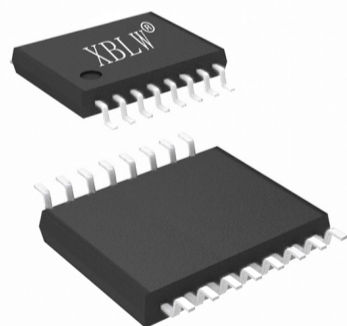
- Synchronous counting and loading
- 2 count enable inputs for n-bit cascading
- Synchronous reset
- Positive-edge triggered clock
- Specified from -20°C to +85°C
- Packaging information: DIP-16/SOP-16/TSSOP-16



DIP-16



SOP-16



TSSOP-16

Ordering Information

Product Model	Package Type	Marking	Packing	Packing Qty
XBLW SN74LS163N	DIP-16	74LS163N	Tube	1000Pcs/Box
XBLW SN74LS163DTR	SOP-16	74LS163	Tape	2500Pcs/Reel
XBLW SN74LS163TDTR	TSSOP-16	74LS163	Tape	3000Pcs/Reel

Block Diagram

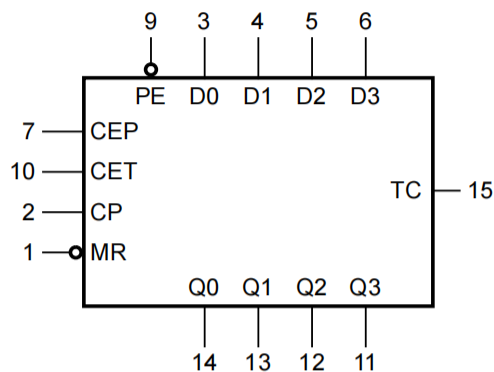


Figure 1. Logic symbol

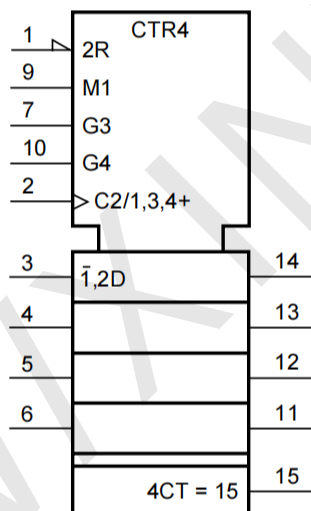


Figure 2. IEC logic symbol

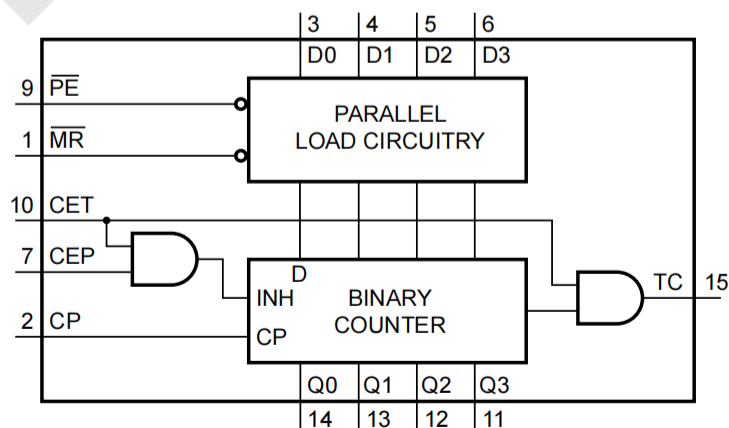


Figure 3. Functional diagram

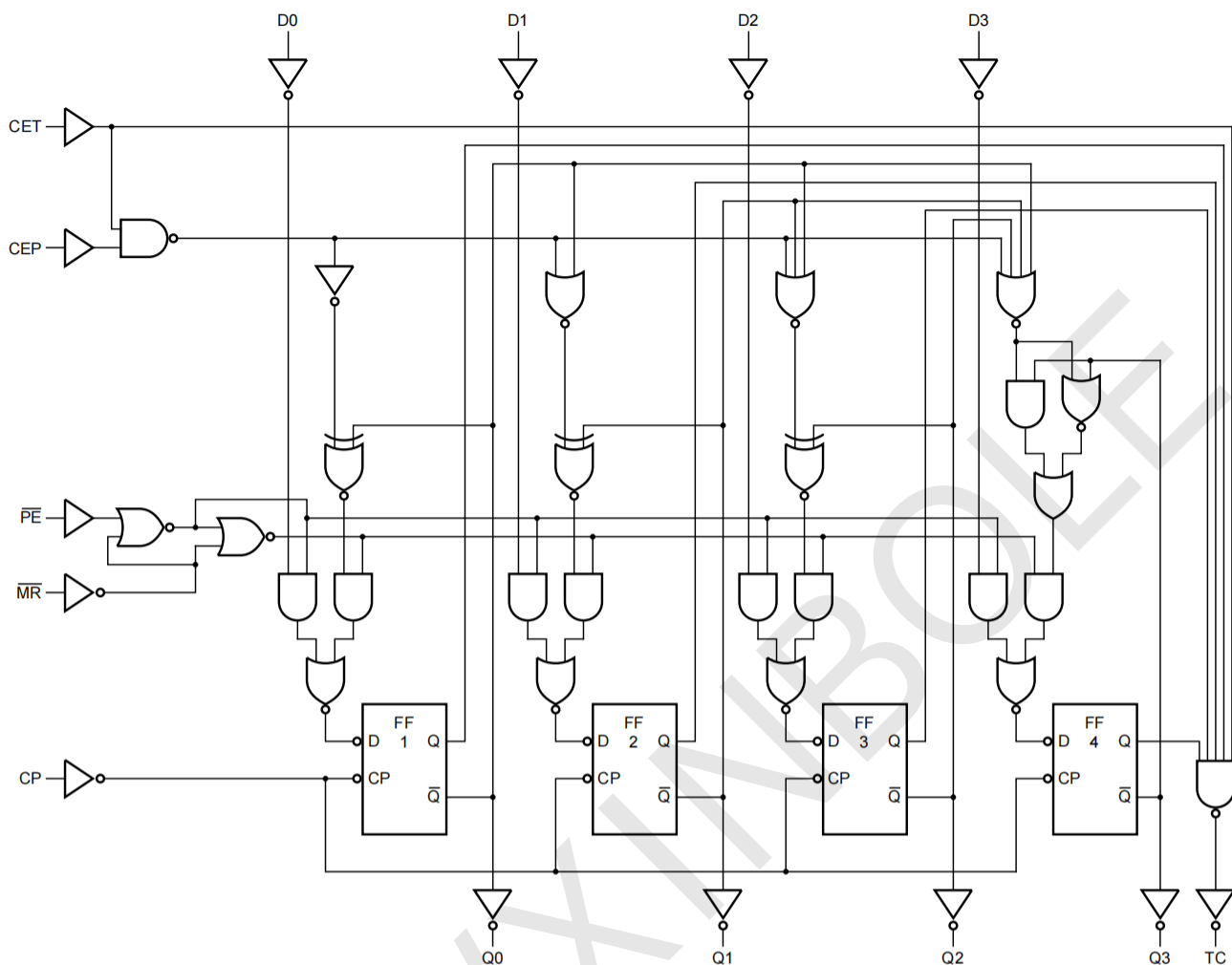


Figure 4. Logic diagram

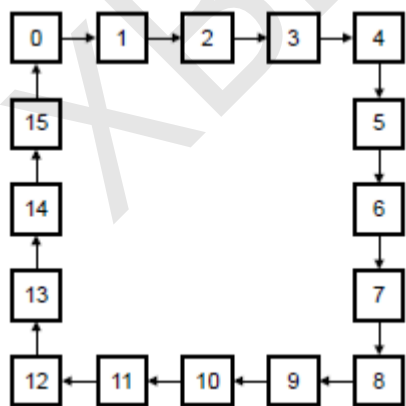


Figure 5. State diagram

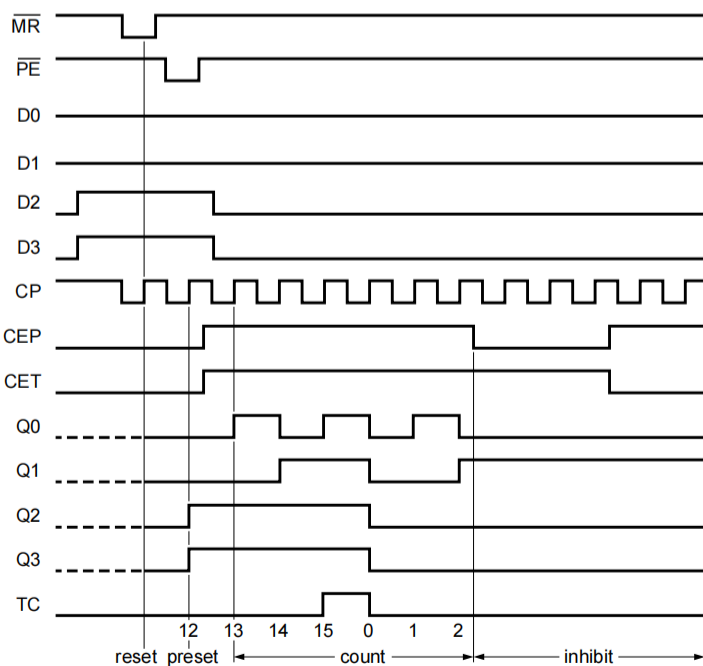
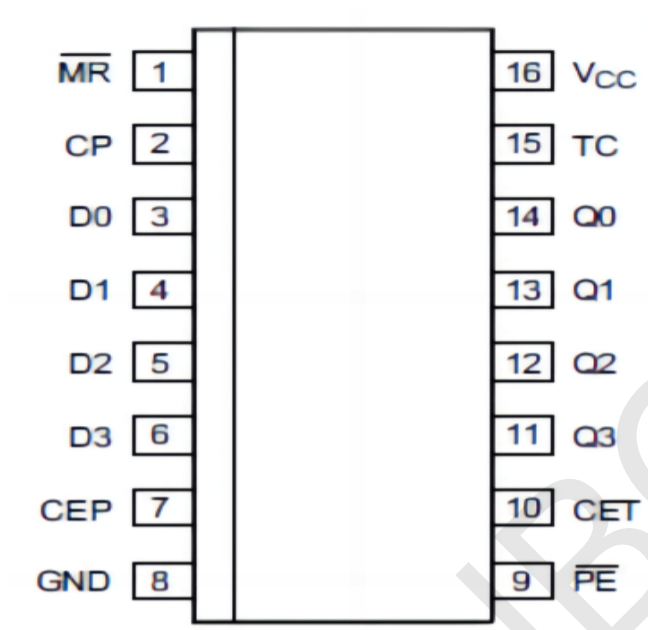


Figure 6. Typical timing sequence

Pin Configurations



Pin Description

Pin No.	Pin Name	Description
1	$\overline{\text{MR}}$	asynchronous master reset (active LOW)
2	CP	clock input (LOW-to-HIGH, edge triggered)
3	D0	data input
4	D1	data input
5	D2	data input
6	D3	data input
7	CEP	count enable input
8	GND	ground (0V)
9	$\overline{\text{PE}}$	parallel enable input (active LOW)
10	CET	count enable carry input
11	Q3	flip-flop output
12	Q2	flip-flop output
13	Q1	flip-flop output
14	Q0	flip-flop output
15	TC	terminal count output
16	V _{CC}	supply voltage

Function Table

Operating mode	Input						Output	
	$\overline{\text{MR}}$	CP	CEP	CET	$\overline{\text{PE}}$	Dn	Qn	TC
reset (clear)	L	↑	X	X	X	X	L	L
parallel load	h	↑	X	X	L	L	L	L
	h	↑	X	X	L	h	H	L
count	h	↑	h	h	h	X	count	[2]
Hold(do nothing)	h	X	L	X	h	X	q _n	L
	h	X	X	L	h	X	q _n	L

Note:

[1] H=HIGH voltage level; L=LOW voltage level; X=don't care; ↑=LOW-to-HIGH clock transition; L=LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition; h=HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition; q=lower case letters indicate the state of the referenced output one set-up time prior to the LOW- to-HIGH CP transition.

[2] The TC output is HIGH when CET is HIGH and the counter is at terminal count (HHHH).

Electrical Parameter

Absolute Maximum Ratings

(Voltages are referenced to GND(ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Max.	Unit
supply voltage	V _{CC}	-		-0.5	+7.0	V
input clamping current	I _{IK}	V _I < -0.5V or V _I > V _{CC} +0.5V		-	±20	mA
output clamping current	I _{OK}	V _O < -0.5V or V _O > V _{CC} +0.5V		-	±20	mA
output current	I _O	-0.5V < V _O < V _{CC} +0.5V		-	±25	mA
supply current	I _{CC}	-		-	+50	mA
ground current	I _{GND}	-		-50	-	mA
storage temperature	T _{stg}	-		-65	+150	°C
total power dissipation	P _{tot}	-		-	500	mW
Soldering temperature	T _L	10s	DIP	245		°C
			SOP/TSSOP	260		

Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
supply voltage	V_{CC}	-	2.0	5.0	6.0	V
input voltage	V_I	-	0	-	V_{CC}	V
output voltage	V_O	-	0	-	V_{CC}	V
input transition rise and fall rate	$\Delta t/\Delta V$	$V_{CC}=2.0V$	-	-	625	ns/V
		$V_{CC}=4.5V$	-	1.67	139	ns/V
		$V_{CC}=6.0V$	-	-	83	ns/V
ambient temperature	T_{amb}	-	-20	-	+85	°C

DC Characteristics 1

($T_{amb}=25^{\circ}C$, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
HIGH-level input voltage	V_{IH}	$V_{CC}=2.0V$		1.5	1.2	-	V
		$V_{CC}=4.5V$		3.15	2.4	-	V
		$V_{CC}=6.0V$		4.2	3.2	-	V
LOW-level input voltage	V_{IL}	$V_{CC}=2.0V$		-	0.8	0.5	V
		$V_{CC}=4.5V$		-	2.1	1.35	V
		$V_{CC}=6.0V$		-	2.8	1.8	V
HIGH-level output voltage	V_{OH}	$V_I = V_{IH} \text{ or } V_{IL}$	$I_O=-20\mu A; V_{CC}=2.0V$	1.9	2.0	-	V
			$I_O=-20\mu A; V_{CC}=4.5V$	4.4	4.5	-	V
			$I_O=-20\mu A; V_{CC}=6.0V$	5.9	6.0	-	V
			$I_O=-4.0mA; V_{CC}=4.5V$	3.98	4.32	-	V
			$I_O=-5.2mA; V_{CC}=6.0V$	5.48	5.81	-	V
LOW-level output voltage	V_{OL}	$V_I = V_{IH} \text{ or } V_{IL}$	$I_O=20\mu A; V_{CC}=2.0V$	-	0	0.1	V
			$I_O=20\mu A; V_{CC}=4.5V$	-	0	0.1	V
			$I_O=20\mu A; V_{CC}=6.0V$	-	0	0.1	V
			$I_O=4.0mA; V_{CC}=4.5V$	-	0.15	0.26	V
			$I_O=5.2mA; V_{CC}=6.0V$	-	0.16	0.26	V
input leakage current	I_I	$V_I=V_{CC} \text{ or } GND; V_{CC}=6.0V$		-	-	± 1.0	μA
supply current	I_{CC}	$V_I=V_{CC} \text{ or } GND; I_O=0A; V_{CC}=6.0V$		-	-	8.0	μA
input capacitance	C_I	-		-	3.5	-	pF

DC Characteristics 2

($T_{amb} = -20^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
HIGH-level input voltage	V _{IH}	V _{CC} =2.0V		1.5	-	-	V
		V _{CC} =4.5V		3.15	-	-	V
		V _{CC} =6.0V		4.2	-	-	V
LOW-level input voltage	V _{IL}	V _{CC} =2.0V		-	-	0.5	V
		V _{CC} =4.5V		-	-	1.35	V
		V _{CC} =6.0V		-	-	1.8	V
HIGH-level output voltage	V _{OH}	V _I = V _{IH} or V _{IL}	I _O =-20uA; V _{CC} =2.0V	1.9	-	-	V
			I _O =-20uA; V _{CC} =4.5V	4.4	-	-	V
			I _O =-20uA; V _{CC} =6.0V	5.9	-	-	V
			I _O =-4.0mA; V _{CC} =4.5V	3.84	-	-	V
			I _O =-5.2mA; V _{CC} =6.0V	5.34	-	-	V
LOW-level output voltage	V _{OL}	V _I = V _{IH} or V _{IL}	I _O =20uA; V _{CC} =2.0V	-	-	0.1	V
			I _O =20uA; V _{CC} =4.5V	-	-	0.1	V
			I _O =20uA; V _{CC} =6.0V	-	-	0.1	V
			I _O =4.0mA; V _{CC} =4.5V	-	-	0.33	V
			I _O =5.2mA; V _{CC} =6.0V	-	-	0.33	V
input leakage current	I _I	V _I =V _{CC} or GND; V _{CC} =6.0V		-	-	±1.0	uA
supply current	I _{CC}	V _I =V _{CC} or GND; I _O =0A; V _{CC} =6.0V		-	-	80	uA

AC Characteristics 1

($T_{amb}=25^{\circ}\text{C}$, $\text{GND}=0\text{V}$, $C_L=50\text{pF}$, unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
propagation delay	t _{pd}	CP to Qn; see Figure 8	V _{CC} =2.0V	-	55	185	ns
			V _{CC} =4.5V	-	20	37	ns
			V _{CC} =5.0V; C _L = 15pF	-	17	-	ns
			V _{CC} =6.0V	-	16	31	ns
		CP to TC; see Figure 8	V _{CC} =2.0V	-	69	215	ns
			V _{CC} =4.5V	-	25	43	ns
			V _{CC} =5.0V; C _L = 15pF	-	21	-	ns
			V _{CC} =6.0V	-	20	37	ns
		CET to TC; see Figure 9	V _{CC} =2.0V	-	36	120	ns
			V _{CC} =4.5V	-	13	24	ns
			V _{CC} =5.0V; C _L = 15pF	-	11	-	ns
			V _{CC} =6.0V	-	10	20	ns
transition time	t _t	see Figure 8 and Figure 9	V _{CC} =2.0V	-	19	75	ns
			V _{CC} =4.5V	-	7	15	ns
			V _{CC} =6.0V	-	6	13	ns
pulse width	t _w	CP HIGH or LOW; see Figure 8	V _{CC} =2.0V	80	17	-	ns
			V _{CC} =4.5V	16	6	-	ns
			V _{CC} =6.0V	14	5	-	ns
set-up time	t _{su}	MR, Dn to CP; see Figure 10, 11	V _{CC} =2.0V	80	22	-	ns
			V _{CC} =4.5V	16	8	-	ns
			V _{CC} =6.0V	14	6	-	ns
		PE to CP; see Figure 10	V _{CC} =2.0V	80	17	-	ns
			V _{CC} =4.5V	16	6	-	ns
			V _{CC} =6.0V	14	5	-	ns
		CEP, CET to CP; see Figure 12	V _{CC} =2.0V	175	58	-	ns
			V _{CC} =4.5V	35	21	-	ns
			V _{CC} =6.0V	30	17	-	ns
hold time	t _h	Dn, PE, CEP, CET, MR to CP; see Figure 10, 11,	V _{CC} =2.0V	0	-14	-	ns
			V _{CC} =4.5V	0	-5	-	ns
			V _{CC} =6.0V	0	-4	-	ns
maximum frequency	f _{max}	CP; see Figure 8	V _{CC} =2.0V	5	15	-	MHz
			V _{CC} =4.5V	27	46	-	MHz
			V _{CC} =5.0V; C _L = 15pF	-	51	-	MHz
			V _{CC} =6.0V	32	55	-	MHz
power dissipation capacitanc e	C _{PD}	f _i = 1MHz; V _{CC} =5.0V; V _I =GND to V _{CC}		-	33	-	pF

Note:

[1] t_{pd} is the same as t_{PLH} and t_{PHL} .

[2] t_t is the same as t_{THL} and t_{TLH} .

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o)$ where:

f_i =input frequency in MHz; f_o =output frequency in MHz;

C_L =output load capacitance in pF; V_{CC} =supply voltage in V;

N =number of inputs switching; $\sum (C_L \times V_{CC}^2 \times f_o)$ =sum of outputs.

AC Characteristics 2

($T_{amb} = -20^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $GND = 0V$, $C_L = 50pF$, unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
propagation delay	t_{pd}	CP to Qn; see Figure 8	$V_{CC}=2.0V$	-	-	230 ns
			$V_{CC}=4.5V$	-	-	46 ns
			$V_{CC}=6.0V$	-	-	39 ns
		CP to TC; see Figure 8	$V_{CC}=2.0V$	-	-	270 ns
			$V_{CC}=4.5V$	-	-	54 ns
			$V_{CC}=6.0V$	-	-	46 ns
		CET to TC; see Figure 9	$V_{CC}=2.0V$	-	-	150 ns
			$V_{CC}=4.5V$	-	-	30 ns
			$V_{CC}=6.0V$	-	-	26 ns
transition time	t_t	see Figure 8 and Figure 9	$V_{CC}=2.0V$	-	-	95 ns
			$V_{CC}=4.5V$	-	-	19 ns
			$V_{CC}=6.0V$	-	-	16 ns
pulse width	t_w	CP HIGH or LOW; see Figure 8	$V_{CC}=2.0V$	100	-	- ns
			$V_{CC}=4.5V$	20	-	- ns
			$V_{CC}=6.0V$	17	-	- ns
set-up time	t_{su}	$\overline{MR}$, Dn to CP; see Figure 10, 11	$V_{CC}=2.0V$	100	-	- ns
			$V_{CC}=4.5V$	20	-	- ns
			$V_{CC}=6.0V$	17	-	- ns
		$\overline{PE}$ to CP; see Figure 10	$V_{CC}=2.0V$	100	-	- ns
			$V_{CC}=4.5V$	20	-	- ns
			$V_{CC}=6.0V$	17	-	- ns
		CEP, CET to CP; see Figure 12	$V_{CC}=2.0V$	220	-	- ns
			$V_{CC}=4.5V$	44	-	- ns
			$V_{CC}=6.0V$	37	-	- ns
hold time	t_h	Dn, $\overline{PE}$, CEP, CET $\overline{MR}$ to CP; see Figure 10, 11, 12	$V_{CC}=2.0V$	0	-	- ns
			$V_{CC}=4.5V$	0	-	- ns
			$V_{CC}=6.0V$	0	-	- ns
maximum frequency	f_{max}	CP; see Figure 8	$V_{CC}=2.0V$	4	-	- MHz
			$V_{CC}=4.5V$	22	-	- MHz
			$V_{CC}=6.0V$	26	-	- MHz

Note:

[1] t_{pd} is the same as t_{PLH} and t_{PHL} .

[2] t_t is the same as t_{THL} and t_{TLH} .

Testing Circuit

AC Testing Circuit

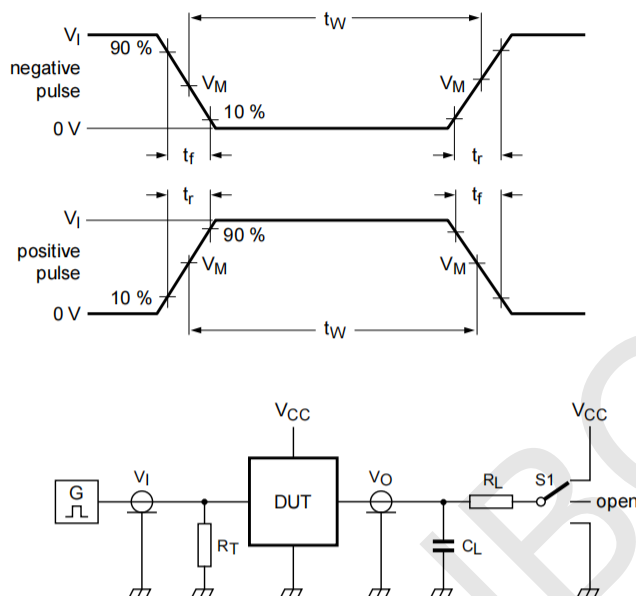


Figure 7. Test circuit for measuring switching times

Definitions for test circuit:

C_L =Load capacitance including jig and probe capacitance.

R_T =Termination resistance should be equal to the output impedance Z_o of the pulse generator. R_L =Load resistance.

S1=Test selection switch

AC Testing Waveforms

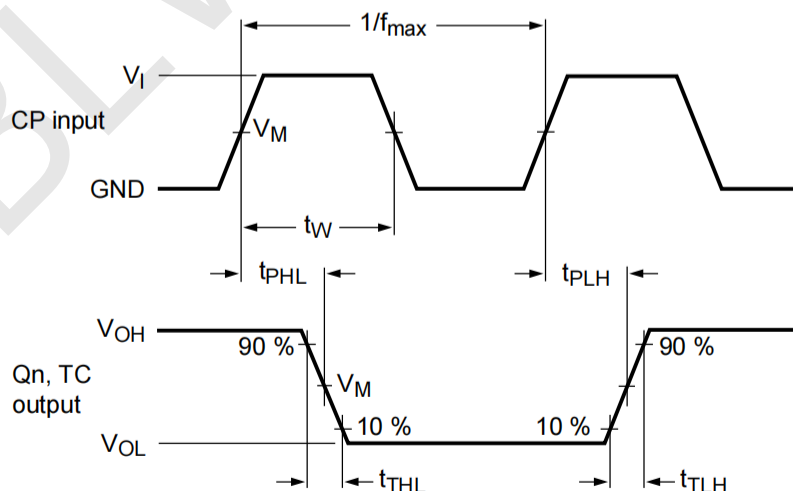


Figure 8. The clock (CP) to outputs (Qn, TC) propagation delays, pulse width, output transition times and maximum frequency

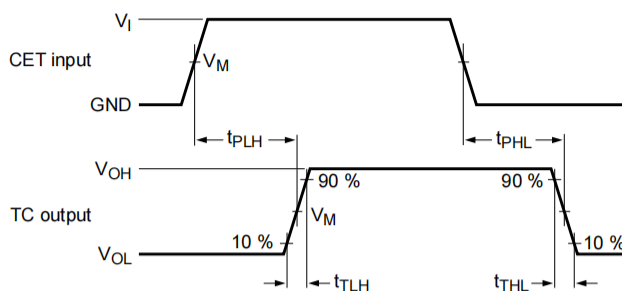


Figure 9. The count enable carry input (CET) to terminal count output (TC) propagation delays and output transition times

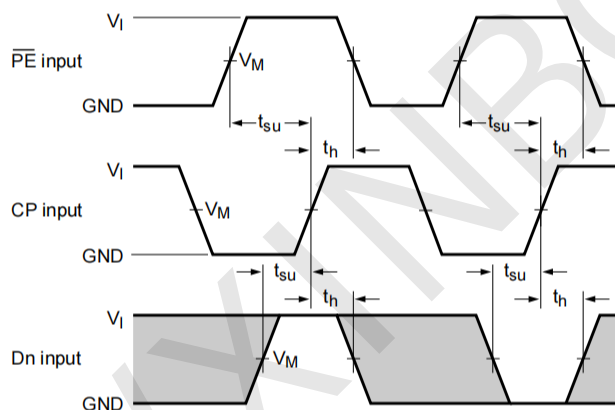


Figure 10. The data input (Dn) and parallel enable input ($\overline{PE}$) set-up and hold times

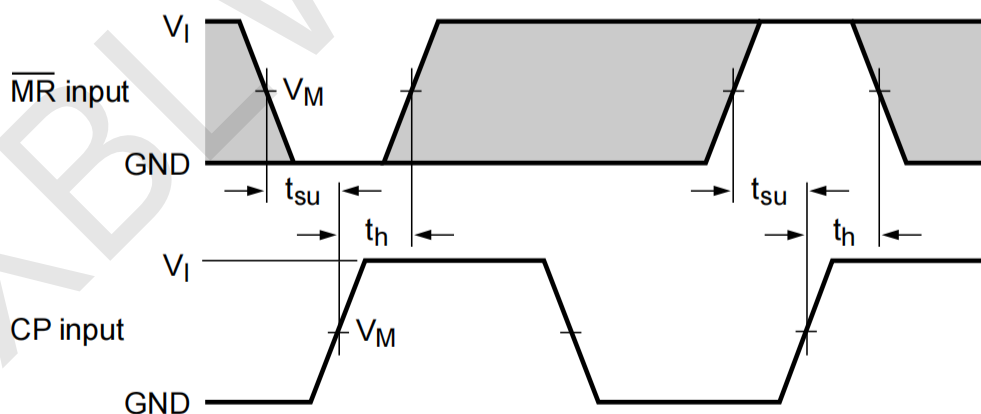


Figure 11. The master reset ($\overline{MR}$) set-up and hold times

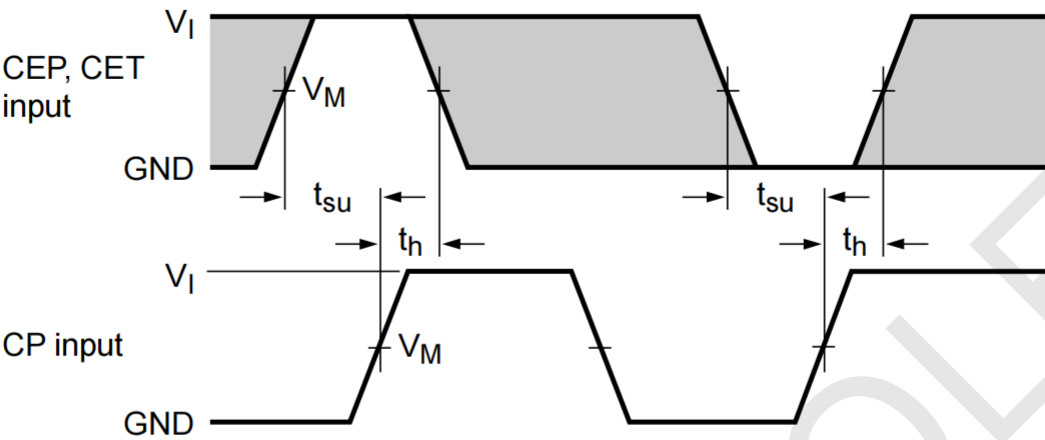


Figure 12. The count enable input (CEP) and count enable carry input (CET) set-up and hold times

Measurement Points

Type	Input		Output
	V_I	V_M	V_M
SN74LS163	GND to V_{CC}	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$

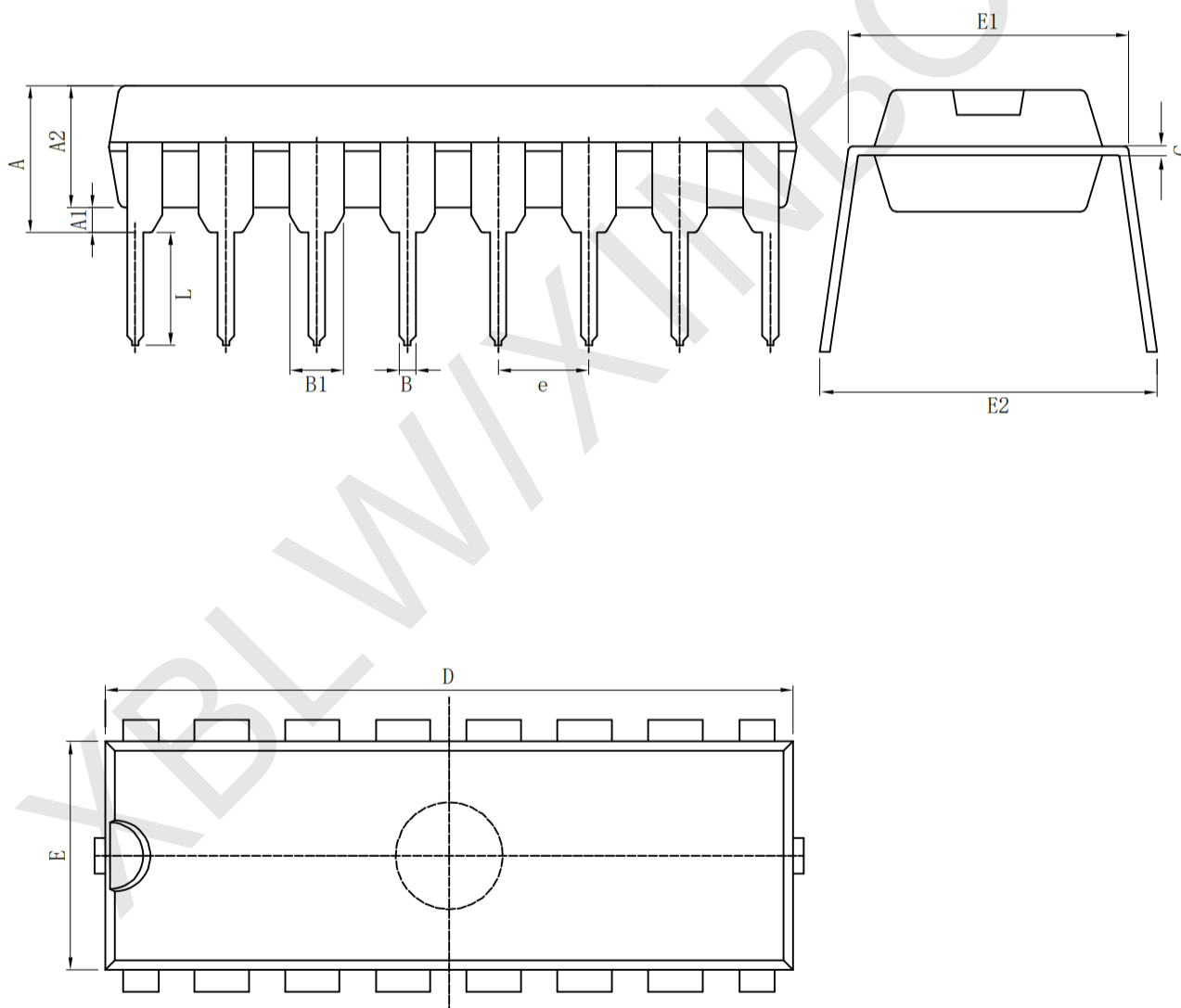
Test Data

Type	Input		Load		S1 position
	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}
SN74LS163	V_{CC}	6ns	15pF, 50pF	1k Ω	open

Package Information

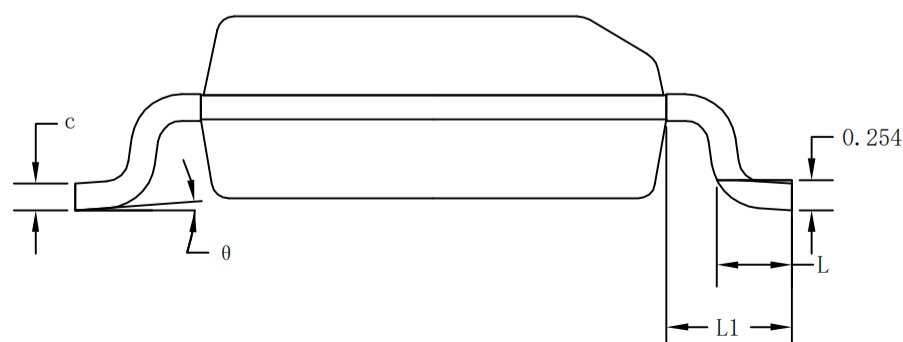
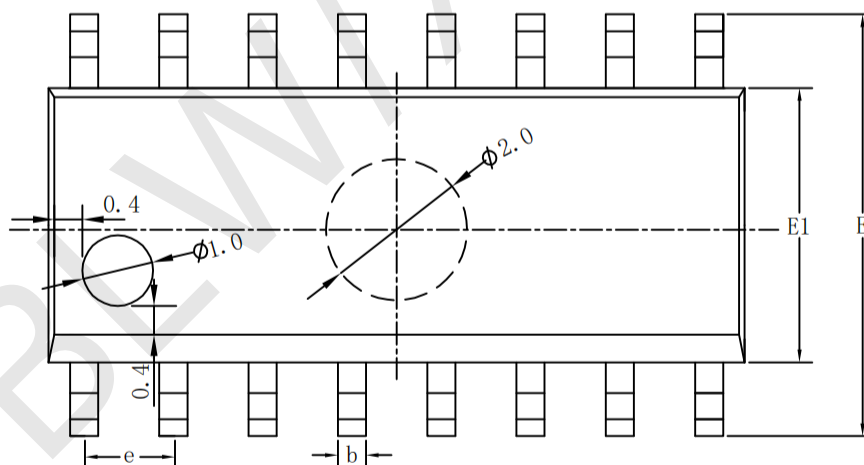
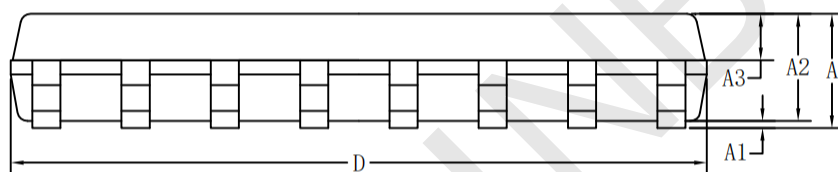
· DIP-16

Size Symbol	Dimensions In Millimeters		Size Symbol	Dimensions In Inches	
	Min(mm)	Max(mm)		Min(in)	Max(in)
A	3.710	4.310	A	0.146	0.170
A1	0.510		A1	0.020	
A2	3.200	3.600	A2	0.126	0.142
B	0.380	0.570	B	0.015	0.022
B1	1.524 (BSC)		B1	0.060 (BSC)	
C	0.204	0.360	C	0.008	0.014
D	18.80	19.20	D	0.740	0.756
E	6.200	6.600	E	0.244	0.260
E1	7.320	7.920	E1	0.288	0.312
e	2.540 (BSC)		e	0.100 (BSC)	
L	3.000	3.600	L	0.118	0.142
E2	8.400	9.000	E2	0.331	0.354



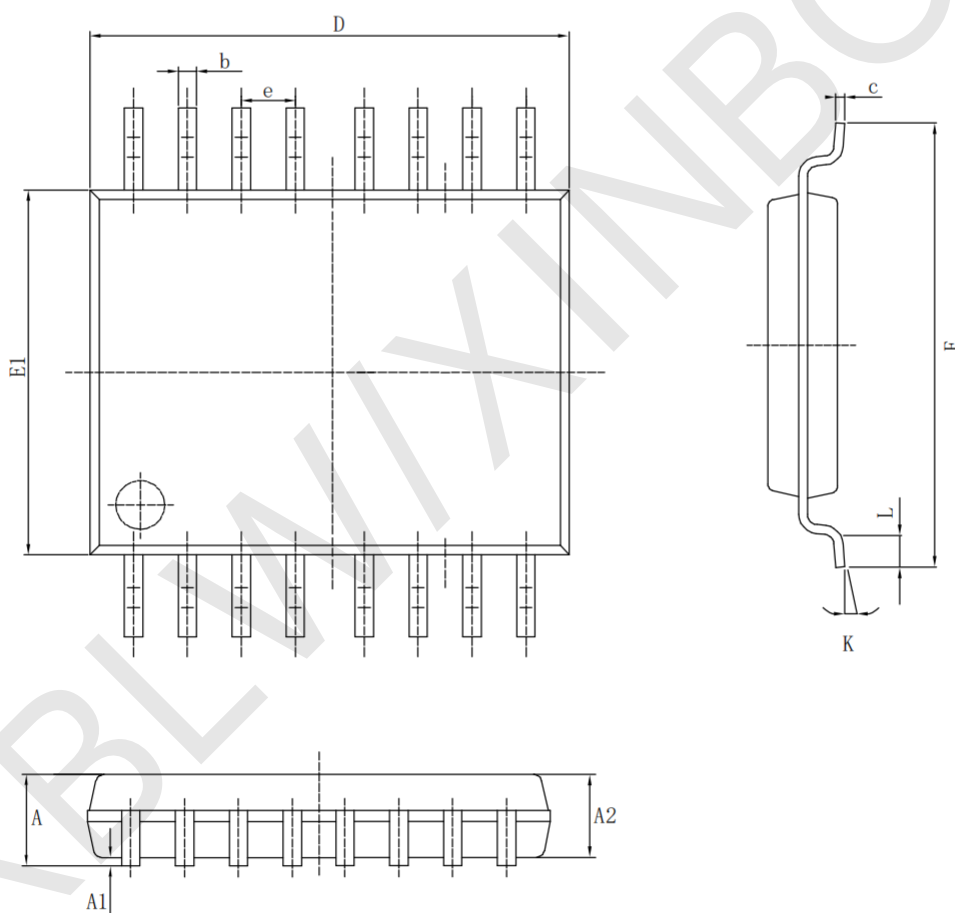
• SOP-16

Size Symbol	Dimensions In Millimeters			Size Symbol	Dimensions In Inches		
	Min (mm)	Nom (mm)	Max (mm)		Min (in)	Nom (in)	Max (in)
A	1.500	1.600	1.700	A	0.059	0.063	0.067
A1	0.100	0.150	0.250	A1	0.004	0.006	0.010
A2	1.400	1.450	1.500	A2	0.055	0.057	0.059
A3	0.600	0.650	0.700	A3	0.024	0.026	0.028
b	0.300	0.400	0.500	b	0.012	0.016	0.020
c	0.150	0.200	0.250	c	0.006	0.008	0.010
D	9.800	9.900	10.00	D	0.386	0.390	0.394
E	5.800	6.000	6.200	E	0.228	0.236	0.244
E1	3.850	3.900	3.950	E1	0.152	0.154	0.156
e	1.27 (BSC)			e	0.050 (BSC)		
L	0.500	0.600	0.700	L	0.020	0.024	0.028
L1	1.05 (BSC)			L1	0.041 (BSC)		
θ	0°	4°	8°	θ	0°	4°	8°



• TSSOP-16

Size Symbol	Dimensions In Millimeters		Size Symbol	Dimensions In Inches	
	Min(mm)	Max(mm)		Min(in)	Max(in)
A		1.200	A		0.047
A1	0.050	0.150	A1	0.002	0.006
A2	0.800	1.050	A2	0.031	0.041
b	0.190	0.300	b	0.007	0.012
c	0.090	0.200	c	0.004	0.0089
D	4.900	5.100	D	0.193	0.201
E	6.200	6.600	E	0.244	0.260
E1	4.300	4.480	E1	0.169	0.176
e	0.65 (BSC)		e	0.0256 (BSC)	
K	0°	8°	K	0°	8°
L	0.450	0.750	L	0.018	0.030



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