NTB5860NL, NTP5860NL, NVB5860NL

N-Channel Power MOSFET

60 V, 220 A, 3.0 mΩ

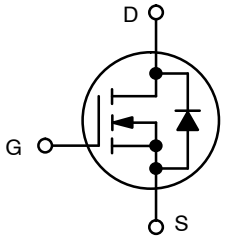
ON Semiconductor®

http://onsemi.com

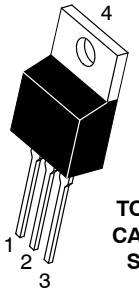
$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	I_D MAX
60 V	3.0 mΩ @ 10 V	220 A
	3.6 mΩ @ 4.5 V	

Features

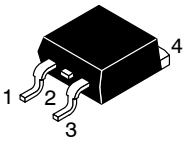
- Low $R_{DS(on)}$
- High Current Capability
- 100% Avalanche Tested
- These Devices are Pb−Free, Halogen Free and are RoHS Compliant
- NVB Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable



N−CHANNEL MOSFET



TO−220AB
CASE 221A
STYLE 5



D²PAK
CASE 418B
STYLE 2

MAXIMUM RATINGS (T_J = 25°C Unless otherwise specified)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	60	V
Gate−to−Source Voltage − Continuous			V_{GS}	±20	V
Continuous Drain Current, $R_{\theta JC}$	Steady State	T_A = 25°C	I_D	220	A
		T_A = 100°C		156	
Power Dissipation, $R_{\theta JC}$	Steady State	T_A = 25°C	P_D	283	W
Pulsed Drain Current	t_p = 10 μs		I_{DM}	660	A
Current Limited by Package			I_{DMmax}	130	A
Operating and Storage Temperature Range			T_J, T_{stg}	−55 to +175	°C
Source Current (Body Diode)			I_S	130	A
Single Pulse Drain−to−Source Avalanche Energy (L = 0.3 mH)			E_{AS}	735	mJ
Lead Temperature for Soldering Purposes (1/8″ from Case for 10 Seconds)			T_L	260	°C

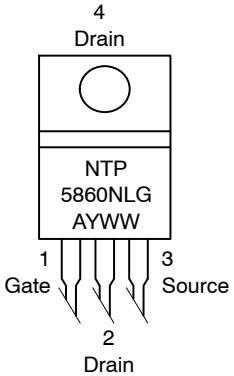
THERMAL RESISTANCE RATINGS

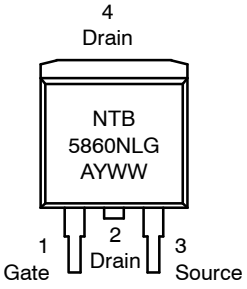
Parameter	Symbol	Max	Unit
Junction−to−Case (Drain) Steady State	$R_{\theta JC}$	0.53	°C/W
Junction−to−Ambient − Steady State (Note 1)	$R_{\theta JA}$	28	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Surface mounted on FR4 board using 1 sq in pad size, (Cu Area 1.127 sq in [2 oz] including traces).

MARKING DIAGRAMS & PIN ASSIGNMENTS





G = Pb−Free Device
A = Assembly Location
Y = Year
WW = Work Week

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless otherwise specified)

Characteristics	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{DS} = 0 V, I_D = 250 μA		60			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	I_D = 250 μA			6.1		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 60 V	T_J = 25°C			1.0	μA
		V_{GS} = 0 V, V_{DS} = 60 V	T_J = 125°C			100	
Gate−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V				±100	nA
ON CHARACTERISTICS (Note 2)							
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 250 μA		1.0		3.0	V
Threshold Temperature Coefficient	$V_{GS(th)}/T_J$				−7.7		mV/°C
Drain−to−Source On−Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 20 A			2.4	3.0	mΩ
		V_{GS} = 4.5 V, I_D = 20 A			2.8	3.6	
Forward Transconductance	g_{FS}	V_{DS} = 15 V, I_D = 30 A			47		S
CHARGES, CAPACITANCES & GATE RESISTANCE							
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz			13216		pF
Output Capacitance	C_{oss}				1127		
Transfer Capacitance	C_{rss}				752		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DS} = 48 V, I_D = 40 A			220		nC
Threshold Gate Charge	$Q_{G(TH)}$				13		
Gate−to−Source Charge	Q_{GS}				37		
Gate−to−Drain Charge	Q_{GD}				54		
SWITCHING CHARACTERISTICS, V_{GS} = 10 V (Note 3)							
Turn−On Delay Time	$t_{d(on)}$	V_{GS} = 10 V, V_{DD} = 48 V, I_D = 100 A, R_G = 2.5 Ω			25		ns
Rise Time	t_r				58		
Turn−Off Delay Time	$t_{d(off)}$				98		
Fall Time	t_f				144		
DRAIN−SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 40 A	T_J = 25°C		0.76	1.1	V_{dc}
			T_J = 125°C		0.60		
Reverse Recovery Time	t_{rr}	V_{GS} = 0 V, I_S = 100 A, dI_S/dt = 20 A/μs			50		ns
Charge Time	t_a				25		
Discharge Time	t_b				25		
Reverse Recovery Stored Charge	Q_{RR}				71		nC

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
3. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

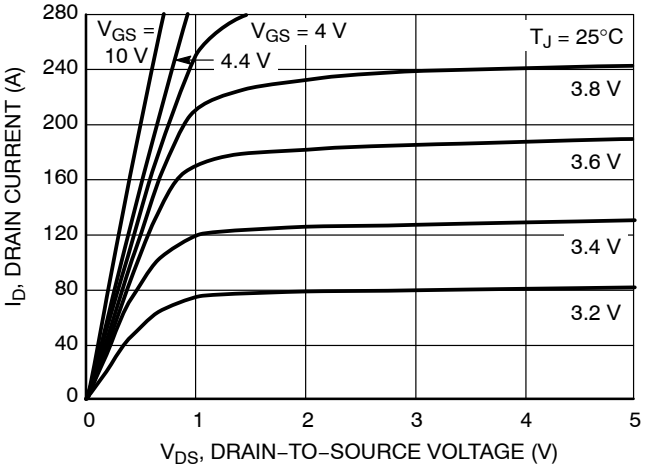


Figure 1. On−Region Characteristics

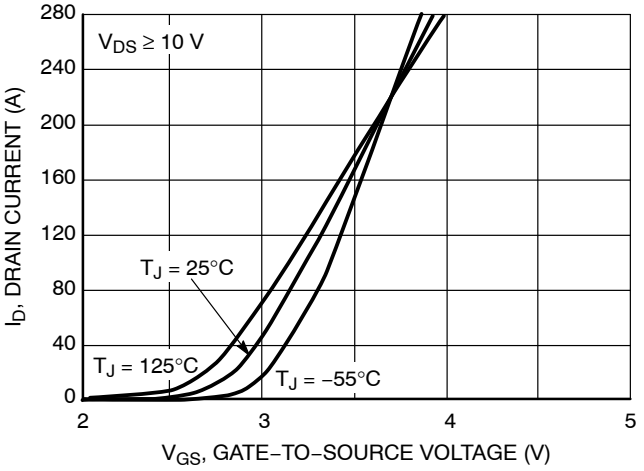


Figure 2. Transfer Characteristics

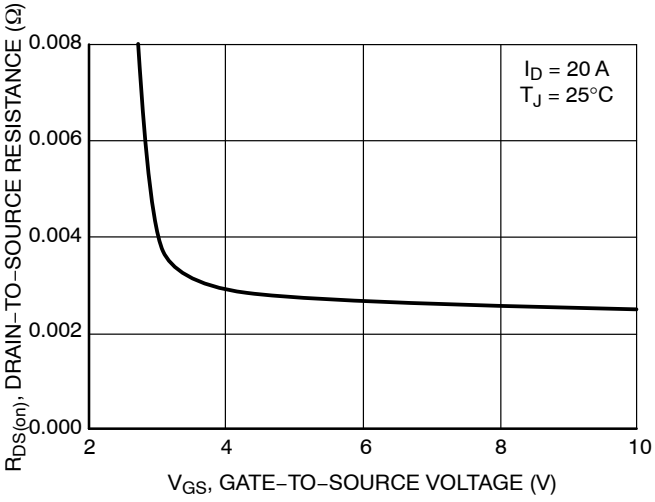


Figure 3. On−Resistance vs. Gate Voltage

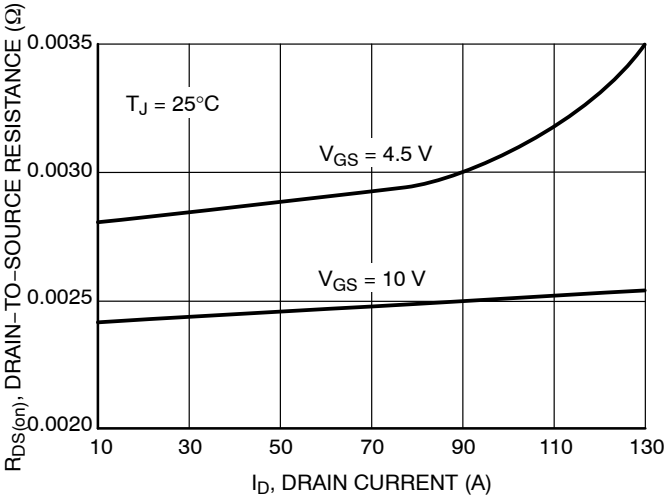


Figure 4. On−Resistance vs. Drain Current

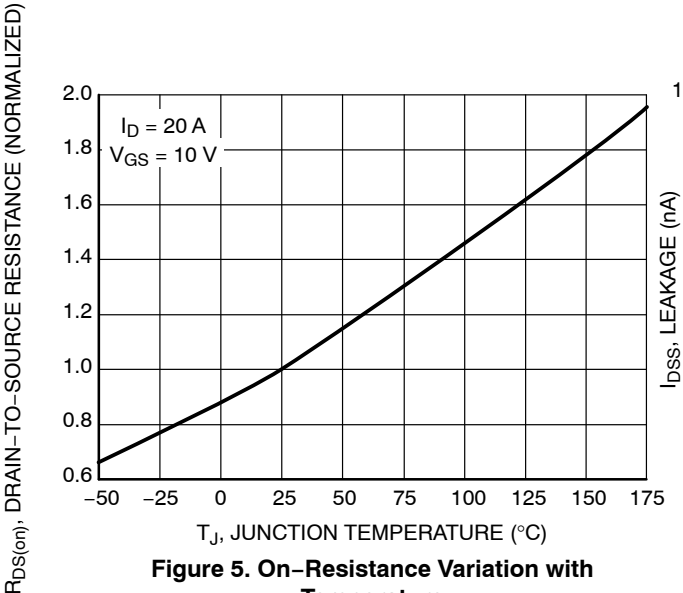


Figure 5. On−Resistance Variation with Temperature

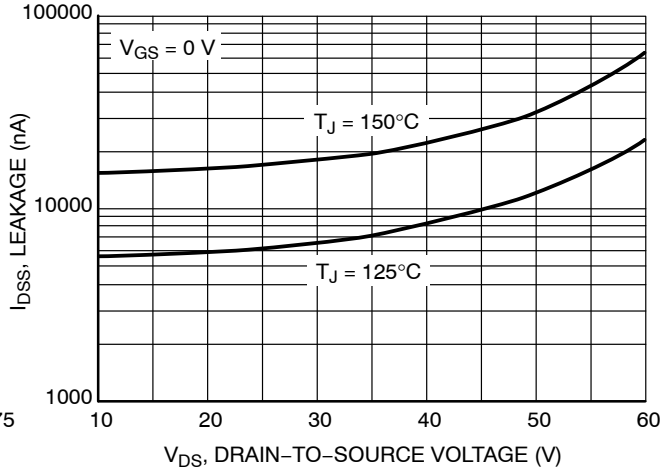


Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

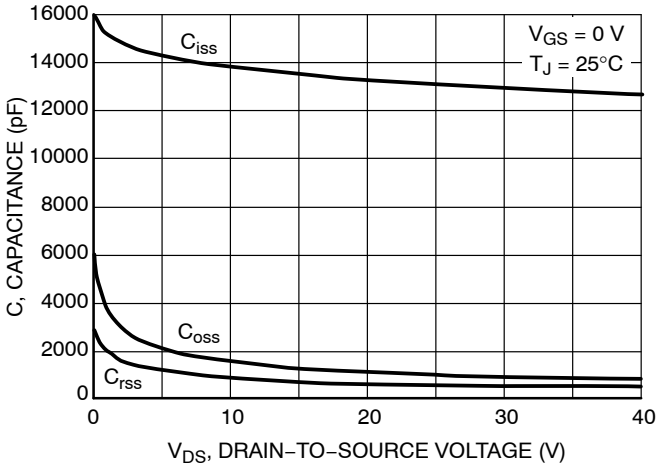


Figure 7. Capacitance Variation

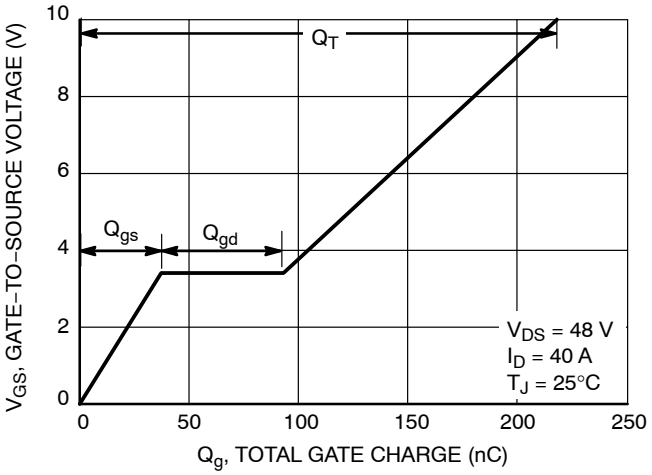


Figure 8. Gate−to−Source vs. Total Charge

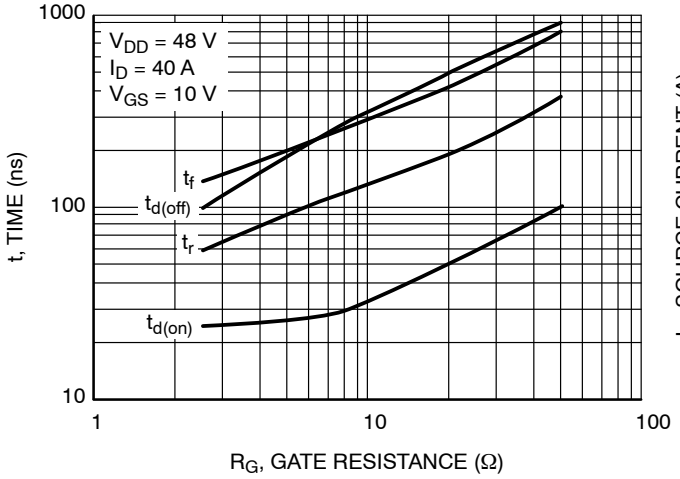


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

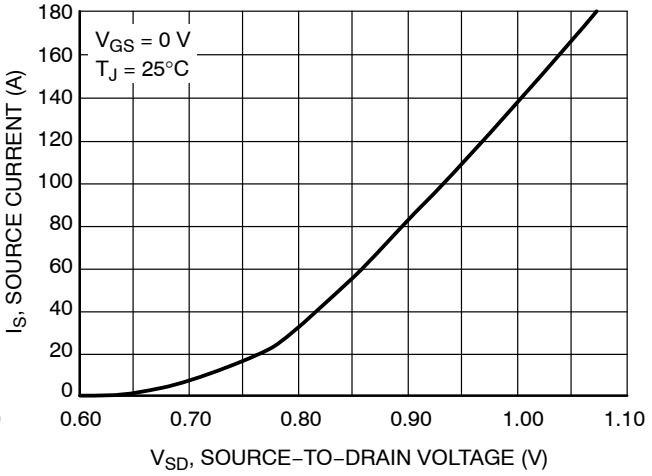


Figure 10. Diode Forward Voltage vs. Current

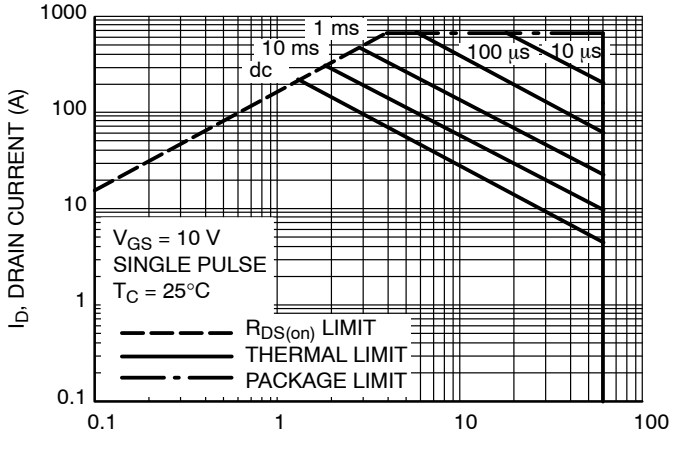


Figure 11. Maximum Rated Forward Biased Safe Operating Area

TYPICAL CHARACTERISTICS

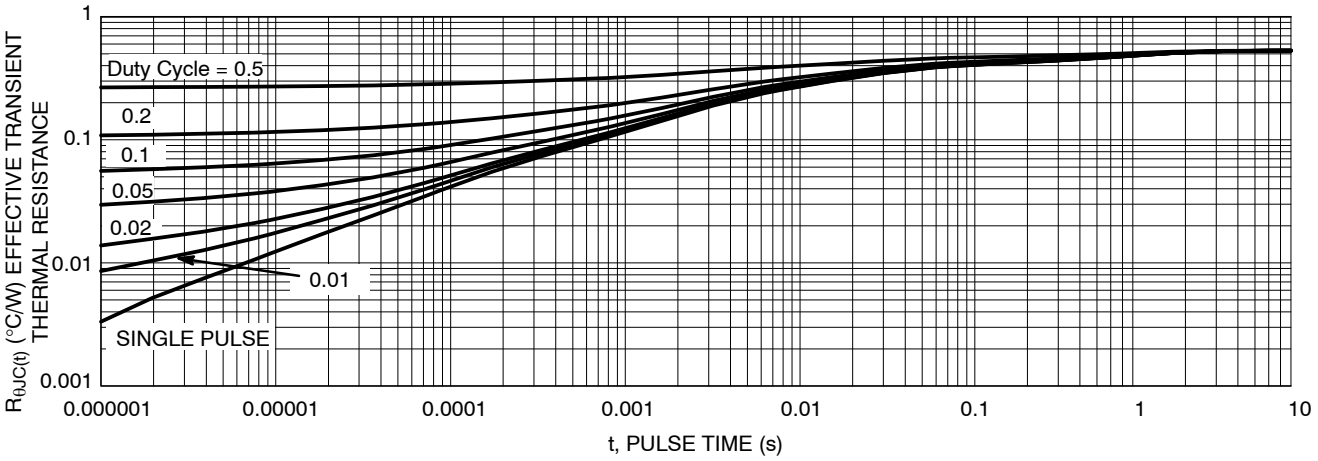


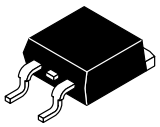
Figure 12. Thermal Response

ORDERING INFORMATION

Device	Package	Shipping†
NTP5860NLG	TO−220AB (Pb−Free)	50 Units / Rail
NTB5860NLT4G	D^2PAK (Pb−Free)	800 / Tape & Reel
NVB5860NLT4G*	D^2PAK (Pb−Free)	800 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

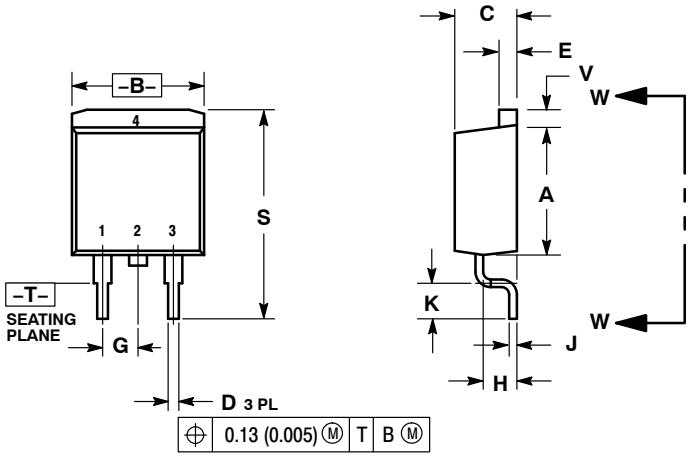
*NVB Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable.



D²PAK 3
CASE 418B–04
ISSUE L

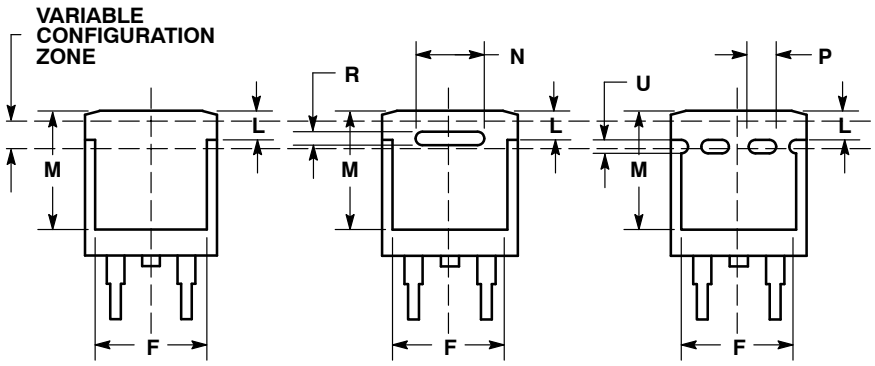
DATE 17 FEB 2015

SCALE 1:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 418B–01 THRU 418B–03 OBSOLETE, NEW STANDARD 418B–04.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.340	0.380	8.64	9.65
B	0.380	0.405	9.65	10.29
C	0.160	0.190	4.06	4.83
D	0.020	0.035	0.51	0.89
E	0.045	0.055	1.14	1.40
F	0.310	0.350	7.87	8.89
G	0.100 BSC		2.54 BSC	
H	0.080	0.110	2.03	2.79
J	0.018	0.025	0.46	0.64
K	0.090	0.110	2.29	2.79
L	0.052	0.072	1.32	1.83
M	0.280	0.320	7.11	8.13
N	0.197 REF		5.00 REF	
P	0.079 REF		2.00 REF	
R	0.039 REF		0.99 REF	
S	0.575	0.625	14.60	15.88
V	0.045	0.055	1.14	1.40



VIEW W–W 1 | VIEW W–W 2 | VIEW W–W 3

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 4:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 5:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

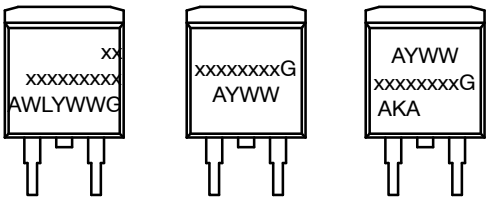
STYLE 6:
PIN 1. NO CONNECT
2. CATHODE
3. ANODE
4. CATHODE

MARKING INFORMATION AND FOOTPRINT ON PAGE 2

D²PAK 3
CASE 418B−04
ISSUE L

DATE 17 FEB 2015

GENERIC
MARKING DIAGRAM*

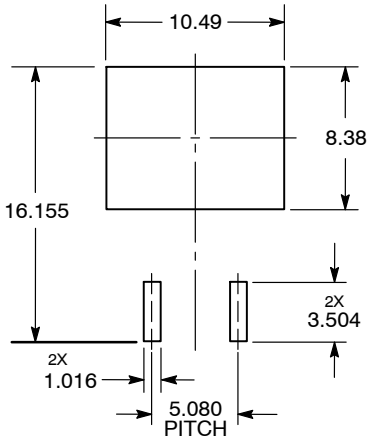


IC **Standard** **Rectifier**

xx	= Specific Device Code
A	= Assembly Location
WL	= Wafer Lot
Y	= Year
WW	= Work Week
G	= Pb−Free Package
AKA	= Polarity Indicator

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	**D²PAK 3**		**PAGE 2 OF 2**

ADDITIONAL INFORMATION

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