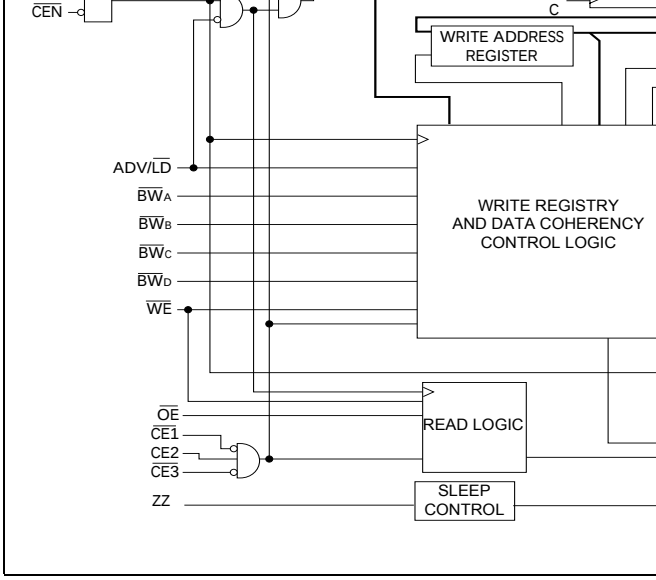
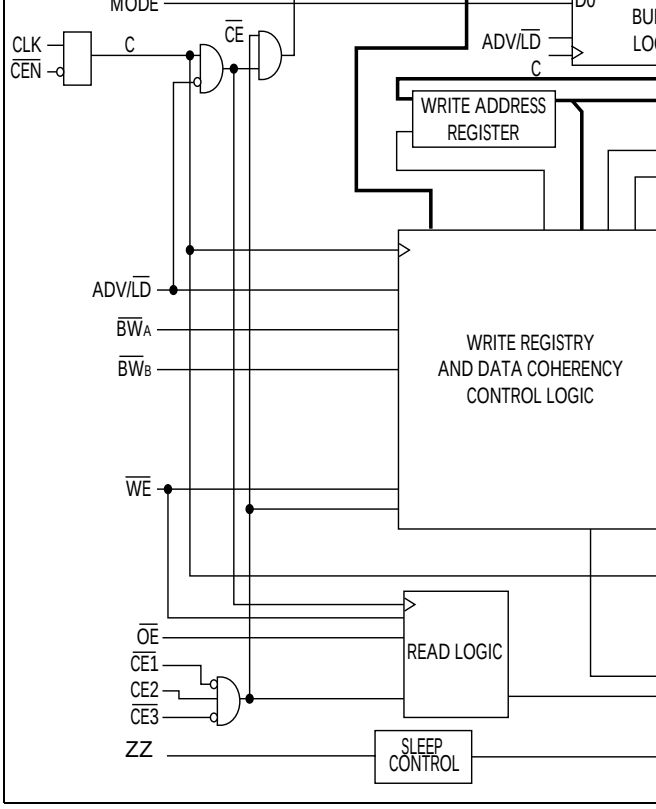
- No Bus Latency™ (NoBL™) architecture eliminates dead cycles between write and read cycles
- Can support up to 133-MHz bus operations with zero wait states
  - Data is transferred on every clock
- Pin compatible and functionally equivalent to ZBT™ devices
- Internally self-timed output buffer control to eliminate the nee to use $\overline{OE}$
- Registered inputs for flow-through operation
- Byte Write capability
- 3.3V/2.5V I/O power supply (V_{DDQ})
- Fast clock-to-output times
  - 6.5 ns (for 133-MHz device)
- Clock Enable ($\overline{CEN}$) pin to enable clock and suspend operatio
- Synchronous self-timed writes
- Asynchronous Output Enable
- Available in JEDEC-standard and lead-free 100-Pin TQFP, lead-free and non lead-free 119-Ball BGA package and 165-Ball FBGA package
- Three chip enables for simple depth expansion.
- Automatic Power-down feature available using ZZ mode or C deselect
- IEEE 1149.1 JTAG-Compatible Boundary Scan
- Burst Capability—linear or interleaved burst order
- Low standby power

Selection Guide

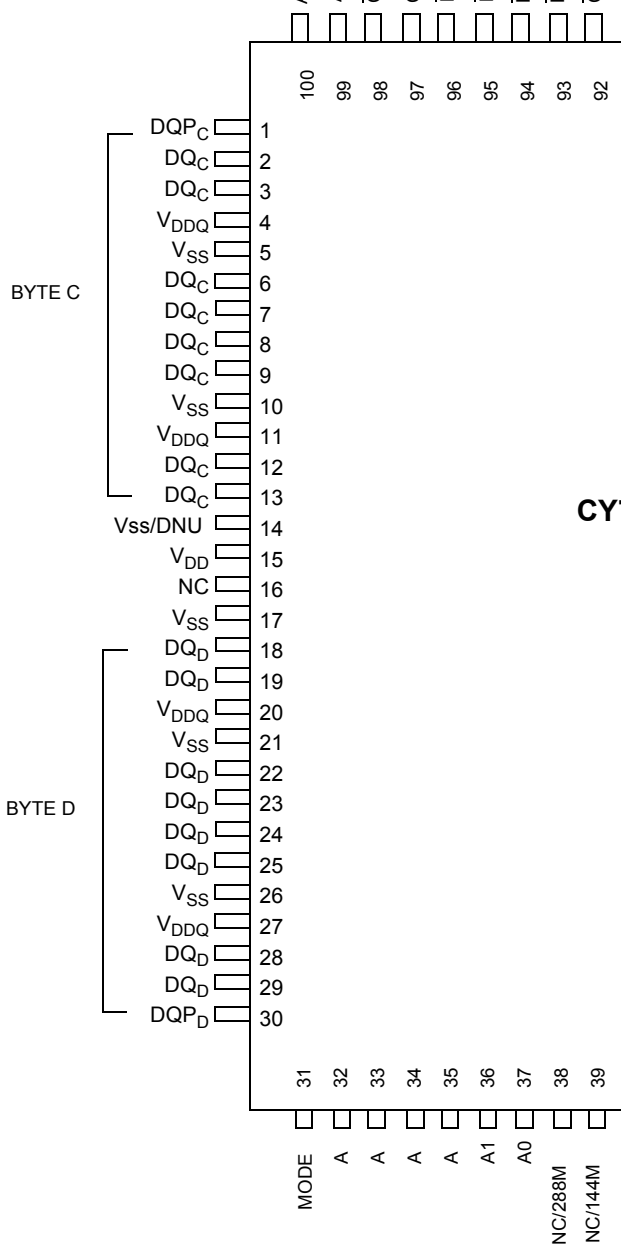
Description	
Maximum Access Time	
Maximum Operating Current	
Maximum CMOS Standby Current	

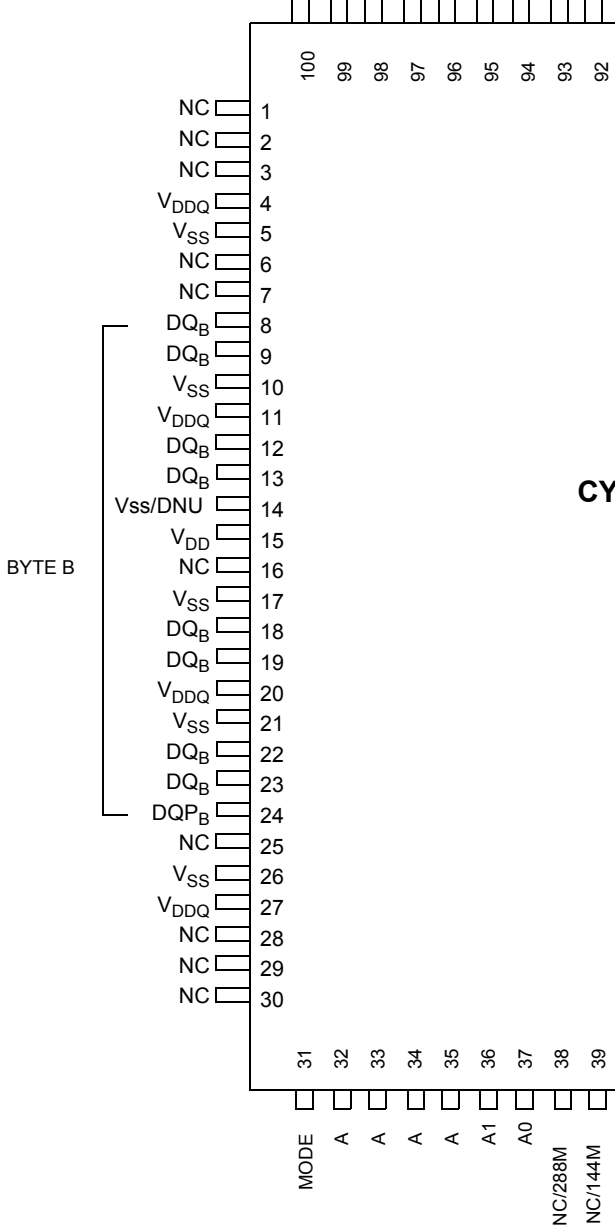
Note
1. For best-practices recommendations, please refer to the Cypress applicati





Document Number: 38-05539 Rev. *F





A	V_{DDQ}	A	A
B	NC/576M	CE_2	A
C	NC/1G	A	A
D	DQ_C	DQP_C	V_{SS}
E	DQ_C	DQ_C	V_{SS}
F	V_{DDQ}	DQ_C	V_{SS}
G	DQ_C	DQ_C	$\overline{BW}_C$
H	DQ_C	DQ_C	V_{SS}
J	V_{DDQ}	V_{DD}	NC
K	DQ_D	DQ_D	V_{SS}
L	DQ_D	DQ_D	$\overline{BW}_D$
M	V_{DDQ}	DQ_D	V_{SS}
N	DQ_D	DQ_D	V_{SS}
P	DQ_D	DQP_D	V_{SS}
R	NC/144M	A	MODE
T	NC	NC/72M	A
U	V_{DDQ}	TMS	TDI

CY7C1357

	1	2	3
A	V_{DDQ}	A	A
B	NC/576M	CE_2	A
C	NC/1G	A	A
D	DQ_B	NC	V_{SS}
E	NC	DQ_B	V_{SS}
F	V_{DDQ}	NC	V_{SS}
G	NC	DQ_B	$\overline{BW}_B$
H	DQ_B	NC	V_{SS}
J	V_{DDQ}	V_{DD}	NC
K	NC	DQ_B	V_{SS}
L	DQ_B	NC	V_{SS}
M	V_{DDQ}	DQ_B	V_{SS}
N	DQ_B	NC	V_{SS}
P	NC	DQP_B	V_{SS}
R	NC/144M	A	MODE
T	NC/72M	A	A
U	V_{DDQ}	TMS	TDI

A	NC/576M	A	CE_1	BW_C	BW_B
B	NC/1G	A	CE2	$\overline{BW}_D$	$\overline{BW}_A$
C	DQP_C	NC	V_{DDQ}	V_{SS}	V_{SS}
D	DQ_C	DQ_C	V_{DDQ}	V_{DD}	V_{SS}
E	DQ_C	DQ_C	V_{DDQ}	V_{DD}	V_{SS}
F	DQ_C	DQ_C	V_{DDQ}	V_{DD}	V_{SS}
G	DQ_C	DQ_C	V_{DDQ}	V_{DD}	V_{SS}
H	NC	NC	NC	V_{DD}	V_{SS}
J	DQ_D	DQ_D	V_{DDQ}	V_{DD}	V_{SS}
K	DQ_D	DQ_D	V_{DDQ}	V_{DD}	V_{SS}
L	DQ_D	DQ_D	V_{DDQ}	V_{DD}	V_{SS}
M	DQ_D	DQ_D	V_{DDQ}	V_{DD}	V_{SS}
N	DQP_D	NC	V_{DDQ}	V_{SS}	NC
P	NC/144M	NC/72M	A	A	TDI
R	MODE	NC/36M	A	A	TMS

CY7C1357C

	1	**2**	**3**	**4**	**5**
A	NC/576M	A	$\overline{CE}_1$	$\overline{BW}_B$	NC
B	NC/1G	A	CE2	NC	$\overline{BW}_A$
C	NC	NC	V_{DDQ}	V_{SS}	V_{SS}
D	NC	DQ_B	V_{DDQ}	V_{DD}	V_{SS}
E	NC	DQ_B	V_{DDQ}	V_{DD}	V_{SS}
F	NC	DQ_B	V_{DDQ}	V_{DD}	V_{SS}
G	NC	DQ_B	V_{DDQ}	V_{DD}	V_{SS}
H	NC	NC	NC	V_{DD}	V_{SS}
J	DQ_B	NC	V_{DDQ}	V_{DD}	V_{SS}
K	DQ_B	NC	V_{DDQ}	V_{DD}	V_{SS}
L	DQ_B	NC	V_{DDQ}	V_{DD}	V_{SS}
M	DQ_B	NC	V_{DDQ}	V_{DD}	V_{SS}
N	DQP_B	NC	V_{DDQ}	V_{SS}	NC
P	NC/144M	NC/72M	A	A	TDI
R	MODE	NC/36M	A	A	TMS

$\overline{BW_A}$, $\overline{BW_B}$ $\overline{BW_C}$, $\overline{BW_D}$	Input-Synchronous	**Byte Write Inputs, activ** on the rising edge of CLK
$\overline{WE}$	Input-Synchronous	**Write Enable Input, acti** This signal must be asse
ADV/$\overline{LD}$	Input-Synchronous	**Advance/Load Input**. Us When HIGH (and CEN is a new address can be loa should be driven LOW in
CLK	Input-Clock	**Clock Input**. Used to ca $\overline{CEN}$. CLK is only recogn
$\overline{CE_1}$	Input-Synchronous	**Chip Enable 1 Input, act** with CE_2, and $\overline{CE_3}$ to sel
CE_2	Input-Synchronous	**Chip Enable 2 Input, act** with $\overline{CE_1}$ and $\overline{CE_3}$ to sele
$\overline{CE_3}$	Input-Synchronous	**Chip Enable 3 Input, act** with $\overline{CE_1}$ and CE_2 to sele
$\overline{OE}$	Input-Asynchronous	**Output Enable, asynchr** block inside the device to allowed to behave as ou input data pins. $\overline{OE}$ is ma clock when emerging fro
$\overline{CEN}$	Input-Synchronous	**Clock Enable Input, act** the SRAM. When deasse does not deselect the dev
ZZ	Input-Asynchronous	**ZZ "Sleep" Input**. This a condition with data integr floating. ZZ pin has an in
DQ_s	I/O-Synchronous	**Bidirectional Data I/O li** triggered by the rising ed memory location specifie Read cycle. The direction pins behave as outputs. W outputs are automatically first clock when emerging regardless of the state of
DQP_X	I/O-Synchronous	**Bidirectional Data Parity** Write sequences, DQP_X
MODE	Input Strap Pin	**Mode Input. Selects the** sequence. When tied to
V_{DD}	Power Supply	**Power supply inputs to**
V_{DDQ}	I/O Power Supply	**Power supply for the I/**
V_{SS}	Ground	**Ground for the device**.
TDO	JTAG serial output Synchronous	**Serial data-out to the JT** feature is not being utilize TQFP packages.

TMS	JTAG serial input Synchronous	**Serial data-In to the JTA** is not being utilized, this available on TQFP packa
TCK	JTAG Clock	**Clock input to the JTAG** be connected to V_{SS}. Th
NC	–	**No Connects**. Not intern Mbit, 576 Mbit and 1G ar die.
V_{SS}/DNU	Ground/DNU	This pin can be connecte

Functional Overview

The CY7C1355C/CY7C1357C is a synchronous flow-throug burst SRAM designed specifically to eliminate wait states durin Write-Read transitions. All synchronous inputs pass throug input registers controlled by the rising edge of the clock. Th clock signal is qualified with the Clock Enable input signal (CEN If CEN is HIGH, the clock signal is not recognized and all intern states are maintained. All synchronous operations are qualifie with CEN. Maximum access delay from the clock rise (t_{CDV}) 6.5 ns (133-MHz device).

Accesses can be initiated by asserting all three Chip Enable ($\overline{CE}_1$, CE_2, $\overline{CE}_3$) active at the rising edge of the clock. If Cloc Enable ($\overline{CEN}$) is active LOW and ADV/$\overline{LD}$ is asserted LOW, th address presented to the device will be latched. The access ca either be a Read or Write operation, depending on the status the Write Enable ($\overline{WE}$). BW_X can be used to conduct Byte Wri operations.

Write operations are qualified by the Write Enable ($\overline{WE}$). A writes are simplified with on-chip synchronous self-timed Wri circuitry.

Three synchronous Chip Enables ($\overline{CE}_1$, CE_2, $\overline{CE}_3$) and a asynchronous Output Enable ($\overline{OE}$) simplify depth expansion. A operations (Reads, Writes, and Deselects) are pipeline ADV/$\overline{LD}$ should be driven LOW once the device has bee deselected in order to load a new address for the next operatio

Single Read Accesses

A read access is initiated when the following conditions a satisfied at clock rise: (1) $\overline{CEN}$ is asserted LOW, (2) $\overline{CE}_1$, CE and $\overline{CE}_3$ are ALL asserted active, (3) the Write Enable inp signal $\overline{WE}$ is deasserted HIGH, and 4) ADV/$\overline{LD}$ is asserted LOW The address presented to the address inputs is latched into th address register and presented to the memory array and contr logic. The control logic determines that a read access is progress and allows the requested data to propagate to th output buffers. The data is available within 7.5 ns (133-MH device) provided $\overline{OE}$ is active LOW. After the first clock of th read access, the output buffers are controlled by $\overline{OE}$ and th internal control logic. $\overline{OE}$ must be driven LOW in order for th device to drive out the requested data. On the subsequent cloc another operation (Read/Write/Deselect) can be initiated. Whe

tri-state the output drivers. As a safety precaution, DQs a
DQP_X are automatically tri-stated during the data portion of
write cycle, regardless of the state of $\overline{OE}$.

Burst Write Accesses

The CY7C1355C/CY7C1357C has an on-chip burst counter th
allows the user the ability to supply a single address and condu
up to four Write operations without reasserting the addres
inputs. ADV/$\overline{LD}$ must be driven LOW in order to load the initi
address, as described in the Single Write Access section abov
When ADV/$\overline{LD}$ is driven HIGH on the subsequent clock rise, th
Chip Enables ($\overline{CE_1}$, CE_2, and $\overline{CE_3}$) and $\overline{WE}$ inputs are ignore
and the burst counter is incremented. The correct $\overline{BW_X}$ inpu
must be driven in each cycle of the burst write, in order to wri
the correct bytes of data.

Sleep Mode

The ZZ input pin is an asynchronous input. Asserting ZZ place
the SRAM in a power conservation “sleep” mode. Two clo
cycles are required to enter into or exit from this “sleep” mod
While in this mode, data integrity is guaranteed. Accesse
pending when entering the “sleep” mode are not considered val
nor is the completion of the operation guaranteed. The devic
must be deselected prior to entering the “sleep” mode. $\overline{CE_1}$, CE
and $\overline{CE_3}$, must remain inactive for the duration of t_{ZZREC} after th
ZZ input returns LOW.

. .

ZZ Mode Electrical Characteristics

Parameter	Description
I_{DDZZ}	Sleep mode standby current
t_{ZZS}	Device operation to ZZ
t_{ZZREC}	ZZ recovery time
t_{ZZI}	ZZ active to sleep current
t_{RZZI}	ZZ Inactive to exit sleep current

Deselect Cycle	None	X	X
Deselect Cycle	None	X	L
Continue Deselect Cycle	None	X	X
READ Cycle (Begin Burst)	External	L	H
READ Cycle (Continue Burst)	Next	X	X
NOP/DUMMY READ (Begin Burst)	External	L	H
DUMMY READ (Continue Burst)	Next	X	X
WRITE Cycle (Begin Burst)	External	L	H
WRITE Cycle (Continue Burst)	Next	X	X
NOP/WRITE ABORT (Begin Burst)	None	L	H
WRITE ABORT (Continue Burst)	Next	X	X
IGNORE CLOCK EDGE (Stall)	Current	X	X
SLEEP MODE	None	X	X

Notes
2. X = “Don't Care.” H = Logic HIGH, L = Logic LOW. $\overline{BW}$x = L signifies at lea Selects are asserted, see Truth Table for details.
3. Write is defined by $\overline{BW}_X$, and $\overline{WE}$. See Truth Table for Read/Write.
4. When a Write cycle is detected, all I/Os are tri-stated, even during Byte Wr
5. The DQs and DQP_X pins are controlled by the current cycle and the $\overline{OE}$ si
6. $\overline{CEN}$ = H, inserts wait states.
7. Device will power-up deselected and the I/Os in a tri-state condition, regar
8. $\overline{OE}$ is asynchronous and is not sampled with the clock rise. It is masked in OE is inactive or when the device is deselected, and DQs and DQP_X = dat

Partial Truth Table for Read/Write[2, 3, 9]

Function (CY7C1355C)	$\overline{W}$
Read	H
Write No bytes written	L
Write Byte A – (DQ_A and DQP_A)	L
Write Byte B – (DQ_B and DQP_B)	L
Write Byte C – (DQ_C and DQP_C)	L
Write Byte D – (DQ_D and DQP_D)	L
Write All Bytes	L

Truth Table for Read/Write[2, 3,9]

Function (CY7C1357C)
Read
Write - No bytes written
Write Byte A – (DQ_A and DQP_A)
Write Byte B – (DQ_B and DQP_B)
Write All Bytes

Note
9. Table only lists a partial listing of the byte write combinations. Any combinati

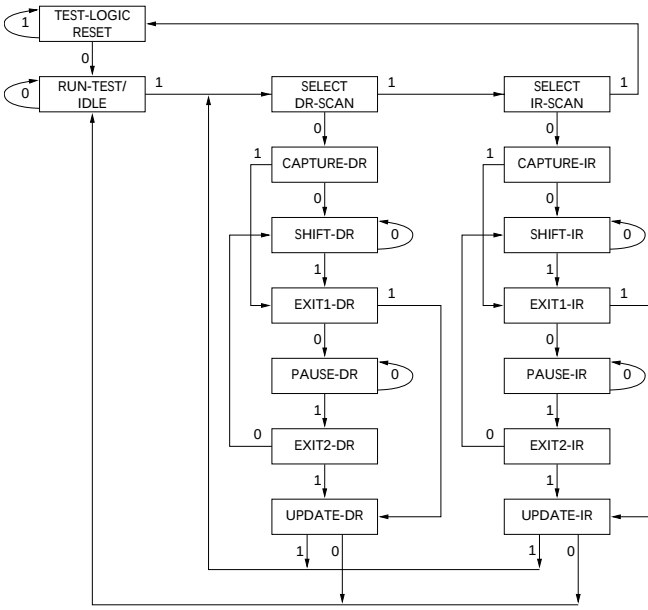
functions from the IEEE specification are excluded because the inclusion places an added delay in the critical speed path of th SRAM. Note the TAP controller functions in a manner that doe not conflict with the operation of other devices using 1149.1 ful compliant TAPs. The TAP operates using JEDEC-standard 3.3 or 2.5V I/O logic levels.

The CY7C1355C/CY7C1357C contains a TAP controlle instruction register, boundary scan register, bypass register, ar ID register.

Disabling the JTAG Feature

It is possible to operate the SRAM without using the JTA feature. To disable the TAP controller, TCK must be tie LOW(V_{SS}) to prevent clocking of the device. TDI and TMS a internally pulled up and may be unconnected. They may alte nately be connected to V_{DD} through a pull-up resistor. TD should be left unconnected. Upon power-up, the device w come up in a reset state which will not interfere with the operatio of the device.

TAP Controller State Diagram



The 0/1 next to each state represents the value of TMS at th rising edge of the TCK.

comes up in a High-Z state.

TAP Registers

Registers are connected between the TDI and TDO balls ar
allow data to be scanned into and out of the SRAM test circuitr
Only one register can be selected at a time through the

instruction register. Data is serially loaded into the TDI ball on th
rising edge of TCK. Data is output on the TDO ball on the fallin
edge of TCK.

Instruction Register

Three-bit instructions can be serially loaded into the instructio
register. This register is loaded when it is placed between the TI
and TDO balls as shown in the Tap Controller Block Diagran
Upon power-up, the instruction register is loaded with th
IDCODE instruction. It is also loaded with the IDCOD
instruction if the controller is placed in a reset state as describe
in the previous section.

When the TAP controller is in the Capture-IR state, the two lea
significant bits are loaded with a binary “01” pattern to allow f
fault isolation of the board-level serial test data path.

Bypass Register

To save time when serially shifting data through registers, it
sometimes advantageous to skip certain chips. The bypas
register is a single-bit register that can be placed between th
TDI and TDO balls. This allows data to be shifted through th
SRAM with minimal delay. The bypass register is set LOW (Vs
when the BYPASS instruction is executed.

Boundary Scan Register

The boundary scan register is connected to all the input ar
bidirectional balls on the SRAM.

The boundary scan register is loaded with the contents of th
RAM I/O ring when the TAP controller is in the Capture-DR sta
and is then placed between the TDI and TDO balls when th
controller is moved to the Shift-DR state. The EXTES
SAMPLE/PRELOAD and SAMPLE Z instructions can be used
capture the contents of the I/O ring.

The Boundary Scan Order tables show the order in which the bi
are connected. Each bit corresponds to one of the bumps on th
SRAM package. The MSB of the register is connected to TD
and the LSB is connected to TDO.

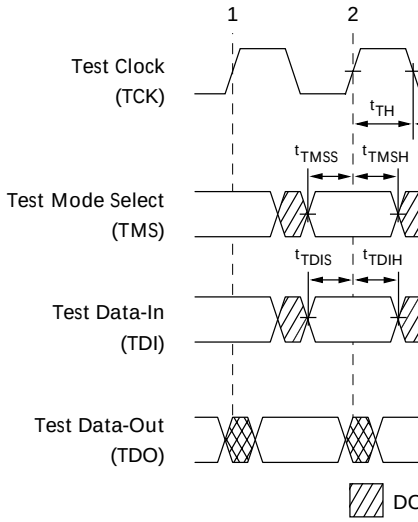
Identification (ID) Register

The ID register is loaded with a vendor-specific, 32-bit coc
during the Capture-DR state when the IDCODE command
loaded in the instruction register. The IDCODE is hardwired in
the SRAM and can be shifted out when the TAP controller is
the Shift-DR state. The ID register has a vendor code and oth
information described in the Identification Register Definitior
table.

BYPASS

When the BYPASS instruction is loaded in the instruction regist
and the TAP is placed in a Shift-DR state, the bypass register
placed between the TDI and TDO pins. The advantage of th

TAP Timing



TAP AC Switching Characteristics Over the Op

Parameter	Description
Clock	
t_{TCYC}	TCK Clock Cycle Time
t_{TF}	TCK Clock Frequency
t_{TH}	TCK Clock HIGH Time
t_{TL}	TCK Clock LOW Time
Output Times	
t_{TDOV}	TCK Clock LOW to TDO Valid
t_{TDOX}	TCK Clock LOW to TDO Invalid
Set-up Times	
t_{TMSS}	TMS Set-Up to TCK Clock Rise
t_{TDIS}	TDI Set-Up to TCK Clock Rise
t_{CS}	Capture Set-Up to TCK Rise
Hold Times	
t_{TMSH}	TMS Hold after TCK Clock Rise
t_{TDIH}	TDI Hold after Clock Rise
t_{CH}	Capture Hold after Clock Rise

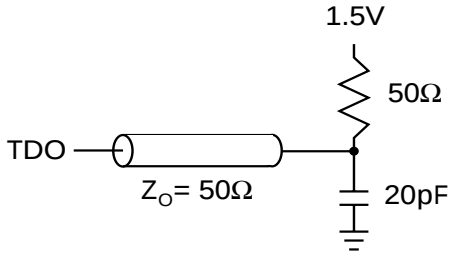
Notes

10. t_{CS} and t_{CH} refer to the set-up and hold time requirements of latching data
11. Test conditions are specified using the load in TAP AC Test Conditions. t_R/

Output reference levels 1.5V

Test load termination supply voltage 1.5V

3.3V TAP AC Output Load Equivalent



TAP DC Electrical Characteristics And Operatin

noted)[12]

Parameter	Description	C
V_{OH1}	Output HIGH Voltage	I_{OH} = –4.0 mA, V I_{OH} = –1.0 mA, V
V_{OH2}	Output HIGH Voltage	I_{OH} = –100 µA
V_{OL1}	Output LOW Voltage	I_{OL} = 8.0 mA
		I_{OL} = 8.0 mA
V_{OL2}	Output LOW Voltage	I_{OL} = 100 µA
V_{IH}	Input HIGH Voltage	
V_{IL}	Input LOW Voltage	
I_X	Input Load Current	GND ≤ V_{IN} ≤ V_{DD}

Identification Register Definitions

Instruction Field	CY7C1355C (256Kx36)	
Revision Number (31:29)	010	
Device Depth (28:24)	01010	
Device Width (23:18)	001001	
Cypress Device ID (17:12)	100110	
Cypress JEDEC ID Code (11:1)	00000110100	0
ID Register Presence Indicator (0)	1	

Note

12. All voltages referenced to V_{SS} (GND).

ID	
Boundary Scan Order (119-ball BGA package)	
Boundary Scan Order (165-ball FBGA package)	

Identification Codes

Instruction	Code	
EXTEST	000	Captures I/O ring conten Forces all SRAM outputs
IDCODE	001	Loads the ID register wit TDO. This operation doe
SAMPLE Z	010	Captures I/O ring conten Forces all SRAM output
RESERVED	011	Do Not Use: This instruc
SAMPLE/PRELOAD	100	Captures I/O ring conten Does not affect SRAM o function and is therefore
RESERVED	101	Do Not Use: This instruc
RESERVED	110	Do Not Use: This instruc
BYPASS	111	Places the bypass regist operations.

2	H4	$\overline{WE}$	38	T5	A
3	M4	$\overline{CEN}$	39	T3	A
4	F4	$\overline{OE}$	40	R2	A
5	B4	ADV/$\overline{LD}$	41	R3	MODE
6	G4	A	42	P2	DQP_D
7	C3	A	43	P1	DQ_D
8	B3	A	44	L2	DQ_D
9	D6	DQP_B	45	K1	DQ_D
10	H7	DQ_B	46	N2	DQ_D
11	G6	DQ_B	47	N1	DQ_D
12	E6	DQ_B	48	M2	DQ_D
13	D7	DQ_B	49	L1	DQ_D
14	E7	DQ_B	50	K2	DQ_D
15	F6	DQ_B	51	Internal	Internal
16	G7	DQ_B	52	H1	DQ_C
17	H6	DQ_B	53	G2	DQ_C
18	T7	ZZ	54	E2	DQ_C
19	K7	DQ_A	55	D1	DQ_C
20	L6	DQ_A	56	H2	DQ_C
21	N6	DQ_A	57	G1	DQ_C
22	P7	DQ_A	58	F2	DQ_C
23	N7	DQ_A	59	E1	DQ_C
24	M6	DQ_A	60	D2	DQP_C
25	L7	DQ_A	61	C2	A
26	K6	DQ_A	62	A2	A
27	P6	DQP_A	63	E4	$\overline{CE}_1$
28	T4	A	64	B2	CE_2
29	A3	A	65	L3	$\overline{BW}_D$
30	C5	A	66	G3	$\overline{BW}_C$
31	B5	A	67	G5	$\overline{BW}B$
32	A5	A	68	L5	$\overline{BW}_A$
33	C6	A	69	B6	$\overline{CE}_3$
34	A6	A			
35	P4	A0			
36	N4	A1			

2	B7	$\overline{WE}$	38	P4	A
3	A7	$\overline{CEN}$	39	R3	A
4	B8	$\overline{OE}$	40	P3	A
5	A8	ADV/$\overline{LD}$	41	R1	MODE
6	A9	A	42	N1	DQP_D
7	B10	A	43	L2	DQ_D
8	A10	A	44	K2	DQ_D
9	C11	DQP_B	45	J2	DQ_D
10	E10	DQ_B	46	M2	DQ_D
11	F10	DQ_B	47	M1	DQ_D
12	G10	DQ_B	48	L1	DQ_D
13	D10	DQ_B	49	K1	DQ_D
14	D11	DQ_B	50	J1	DQ_D
15	E11	DQ_B	51	Internal	Internal
16	F11	DQ_B	52	G2	DQ_C
17	G11	DQ_B	53	F2	DQ_C
18	H11	ZZ	54	E2	DQ_C
19	J10	DQ_A	55	D2	DQ_C
20	K10	DQ_A	56	G1	DQ_C
21	L10	DQ_A	57	F1	DQ_C
22	M10	DQ_A	58	E1	DQ_C
23	J11	DQ_A	59	D1	DQ_C
24	K11	DQ_A	60	C1	DQP_C
25	L11	DQ_A	61	B2	A
26	M11	DQ_A	62	A2	A
27	N11	DQP_A	63	A3	CE_1
28	R11	A	64	B3	CE_2
29	R10	A	65	B4	BW_D
30	P10	A	66	A4	$\overline{BW}_C$
31	R9	A	67	A5	$\overline{BW}_B$
32	P9	A	68	B5	$\overline{BW}_A$
33	R8	A	69	A6	$\overline{CE}_3$
34	P8	A			
35	R6	A0			
36	P6	A1			

Ambient Temperature with
Power Applied ..... –55°C to +125°C

Supply Voltage on V_{DD} Relative to GND .....–0.5V to +4.6V

Supply Voltage on V_{DDQ} Relative to GND..... –0.5V to +V_{DD}

DC Voltage Applied to Outputs
in Tri-State .....–0.5V to V_{DDQ} + 0.5V

Electrical Characteristics Over the Operating Rang

Parameter	Description	Tes
V_{DD}	Power Supply Voltage	
V_{DDQ}	I/O Supply Voltage	for 3.3V I/O
		for 2.5V I/O
V_{OH}	Output HIGH Voltage	for 3.3V I/O, I_{OH} = –4.0
		for 2.5V I/O, I_{OH} = –1.0
V_{OL}	Output LOW Voltage	for 3.3V I/O, I_{OL}= 8.0 m
		for 2.5V I/O, I_{OL}= 1.0 m
V_{IH}	Input HIGH Voltage[13]	for 3.3V I/O
		for 2.5V I/O
V_{IL}	Input LOW Voltage[13]	for 3.3V I/O
		for 2.5V I/O
I_X	Input Leakage Current except ZZ and MODE	GND ≤ V_I ≤ V_{DDQ}
	Input Current of MODE	Input = V_{SS}
		Input = V_{DD}
	Input Current of ZZ	Input = V_{SS}
		Input = V_{DD}
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{DDQ}, Outp
I_{DD}	V_{DD} Operating Supply Current	V_{DD} = Max., I_{OUT} = 0 m f = f_{MAX} = 1/t_{CYC}
I_{SB1}	Automatic CE Power-down Current—TTL Inputs	V_{DD} = Max, Device De V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL} f = f_{MAX}, inputs switchi
I_{SB2}	Automatic CE Power-down Current—CMOS Inputs	V_{DD} = Max, Device De V_{IN} ≤ 0.3V or V_{IN} ≥ V_{DI} f = 0, inputs static
I_{SB3}	Automatic CE Power-down Current—CMOS Inputs	V_{DD} = Max, Device Des V_{IN} ≤ 0.3V or V_{IN} ≥ V_{DI} f = f_{MAX}, inputs switchi
I_{SB4}	Automatic CE Power-down Current—TTL Inputs	V_{DD} = Max, Device De V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f static

Notes
13. Overshoot: V_{IH}(AC) < V_{DD} +1.5V (Pulse width less than t_{CYC}/2), undersho
14. $T_{Power-up}$: Assumes a linear ramp from 0V to V_{DD}(min.) within 200 ms. Du

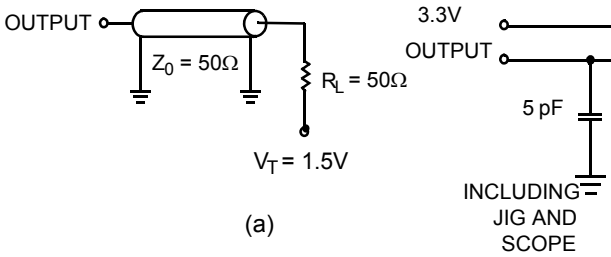
$C_{I/O}$	Input/Output Capacitance	V_{DDQ}

Thermal Resistance[15]

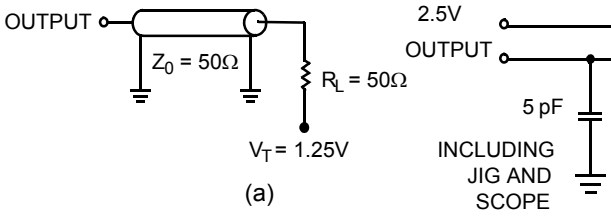
Parameter	Description	Test Co
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Test condition standard test procedures fo thermal impe EIA/JESD51.
Θ_{JC}	Thermal Resistance (Junction to Case)	

AC Test Loads and Waveforms

3.3V I/O Test Load



2.5V I/O Test Load

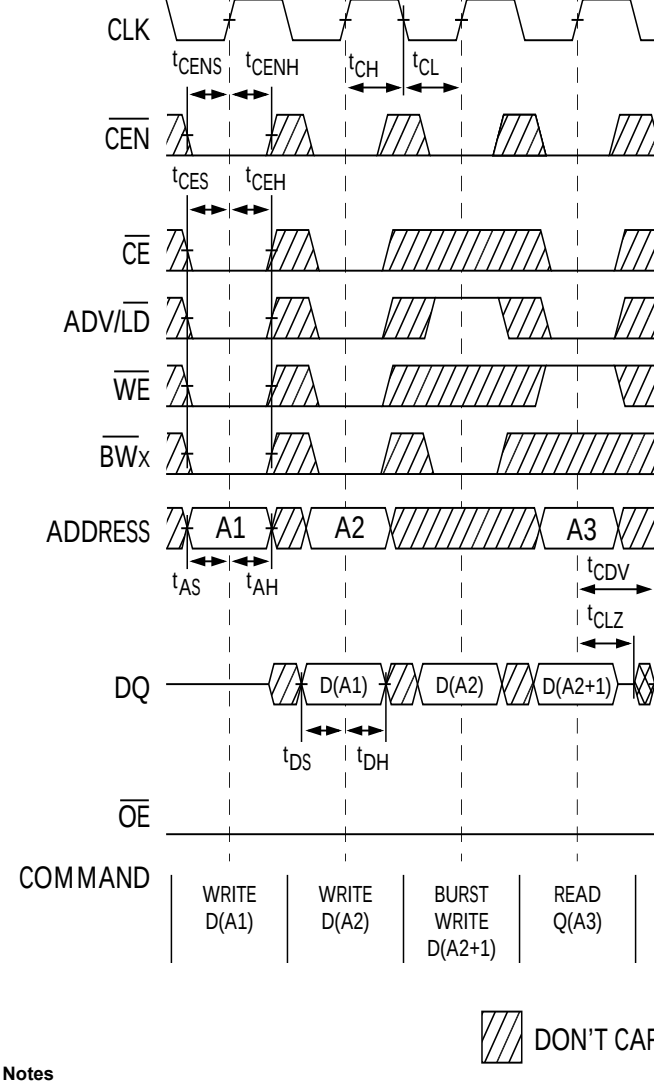


Note
15. Tested initially and after any design or process change that may affect th

Clock	
t_{CYC}	Clock Cycle Time
t_{CH}	Clock HIGH
t_{CL}	Clock LOW
Output Times	
t_{CDV}	Data Output Valid after CLK Rise
t_{DOH}	Data Output Hold after CLK Rise
t_{CLZ}	Clock to Low-Z[19, 20, 21]
t_{CHZ}	Clock to High-Z[19, 20, 21]
t_{OEV}	$\overline{OE}$ LOW to Output Valid
t_{OELZ}	$\overline{OE}$ LOW to Output Low-Z[19, 20, 21]
t_{OEHZ}	$\overline{OE}$ HIGH to Output High-Z[19, 20, 21]
Set-up Times	
t_{AS}	Address Set-up before CLK Rise
t_{ALS}	ADV/$\overline{LD}$ Set-up before CLK Rise
t_{WES}	$\overline{WE}$, $\overline{BW}_X$ Set-up before CLK Rise
t_{CENS}	$\overline{CEN}$ Set-up before CLK Rise
t_{DS}	Data Input Set-up before CLK Rise
t_{CES}	Chip Enable Set-Up before CLK Rise
Hold Times	
t_{AH}	Address Hold after CLK Rise
t_{ALH}	ADV/$\overline{LD}$ Hold after CLK Rise
t_{WEH}	$\overline{WE}$, $\overline{BW}_X$ Hold after CLK Rise
t_{CENH}	$\overline{CEN}$ Hold after CLK Rise
t_{DH}	Data Input Hold after CLK Rise
t_{CEH}	Chip Enable Hold after CLK Rise

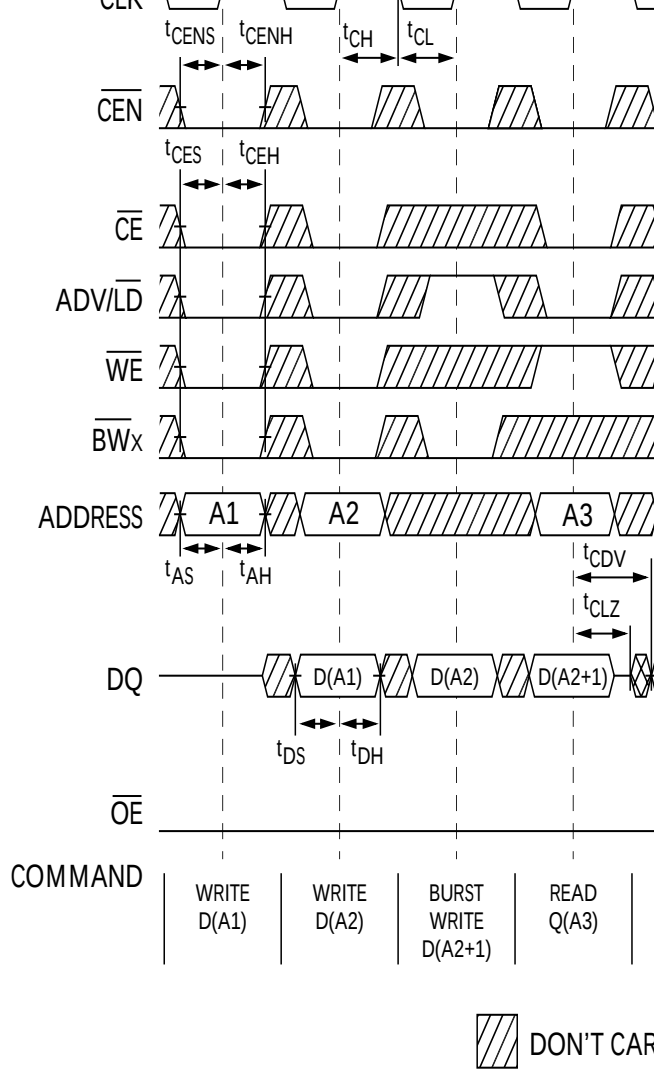
Notes

16. Timing reference level is 1.5V when V_{DDQ} = 3.3V and is 1.25V when V_{DDQ}
17. Test conditions shown in (a) of AC Test Loads unless otherwise noted.
18. This part has a voltage regulator internally; t_{POWER} is the time that the power can be initiated.
19. t_{CHZ}, t_{CLZ}, t_{OELZ}, and t_{OEHZ} are specified with AC test conditions shown voltage.
20. At any given voltage and temperature, t_{OEHZ} is less than t_{OELZ} and t_{CHZ} is data bus. These specifications do not imply a bus contention condition, but to achieve High-Z prior to Low-Z under the same system conditions.
21. This parameter is sampled and not 100% tested.

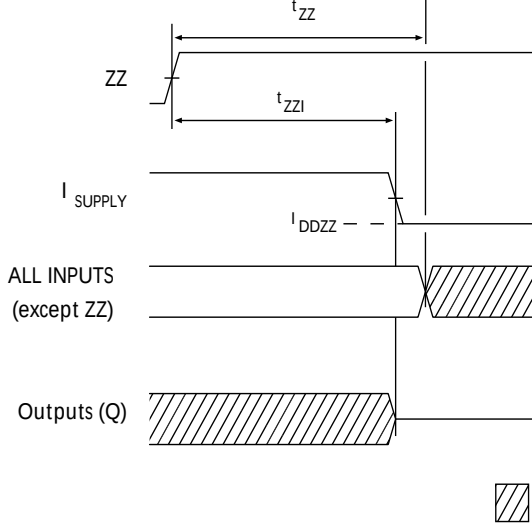


Notes

22. For this waveform ZZ is tied LOW.
23. When $\overline{CE}$ is LOW, $\overline{CE}_1$ is LOW, CE_2 is HIGH and $\overline{CE}_3$ is LOW. When $\overline{CE}$ is
24. Order of the Burst sequence is determined by the status of the MODE (0 =



Note
25. The IGNORE CLOCK EDGE or STALL cycle (Clock 3) illustrates $\overline{CEN}$ bein



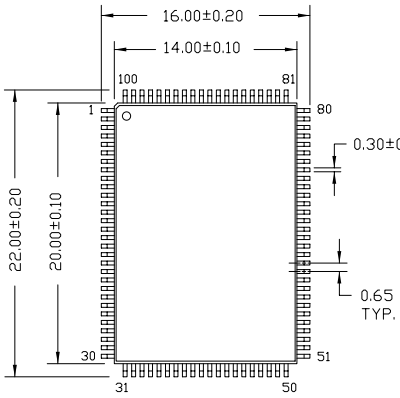
Notes
26. Device must be deselected when entering ZZ mode. See truth table for all
27. DQs are in high-Z when exiting ZZ sleep mode.

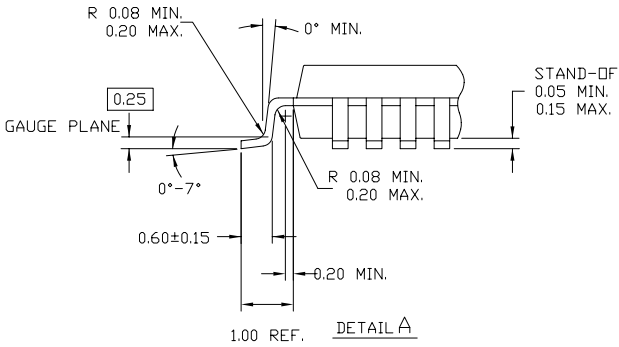
office closest to you, visit us at http://www.cypress.com/go/da

Speed (MHz)	Ordering Code	Package Diagram	
133	CY7C1355C-133AXC	51-85050	100-Pin Thin Q
	CY7C1357C-133AXC		
	CY7C1355C-133BGC	51-85115	119-ball Ball Gr
	CY7C1355C-133BGXC		119-ball Ball Gr
	CY7C1357C-133AXI	51-85050	100-Pin Thin Q
100	CY7C1357C-100AXC	51-85050	100-Pin Thin Q
	CY7C1355C-100BGC	51-85115	119-ball Ball Gr
	CY7C1357C-100BZC	51-85180	165-ball Fine-P

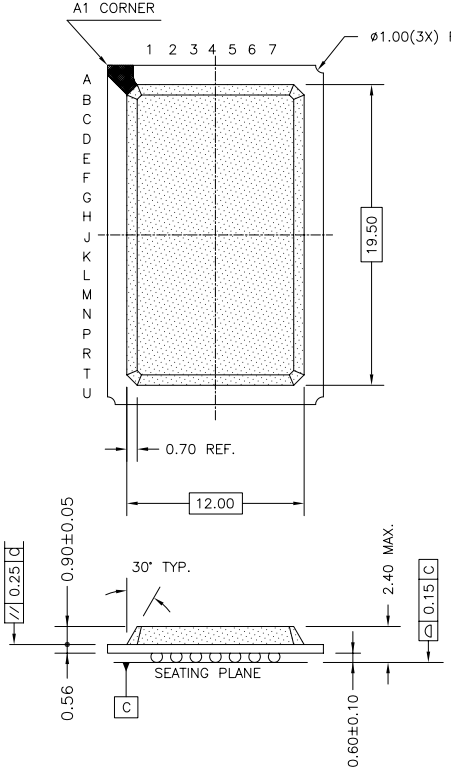
Package Diagrams

100 Pin Thin Plastic Quad

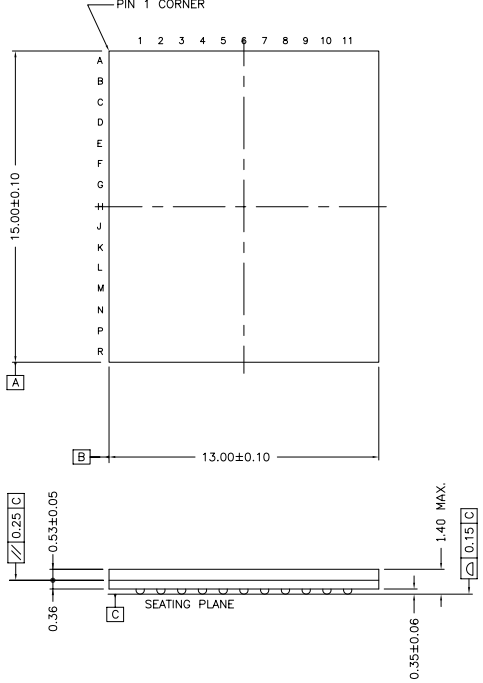




Document Number: 38-05539 Rev. *F



Document Number: 38-05539 Rev. *F



Document Number: 38-05539 Rev. *F

**	242032	See ECN	RKF	New data sh
*A	332059	See ECN	PCI	Changed Bo Removed d Removed 1 Changed I_D Changed I_S Address exp per JEDEC Modified V_C Corrected I_S or $V_{IN} \leq V_{IL}$) Changed Θ_J 6.13 °C/W respectively Changed Θ_J °C/W respectively Changed Θ_J °C/W respe Added lead- Packages Updated Or Changed fro
*B	351895	See ECN	PCI	Changed I_S Updated Or
*C	377095	See ECN	PCI	Modified tes
*D	408298	See ECN	RXU	Changed ad “3901 North Modified “In Electrical C Changed th Replaced P Information Updated Or
*E	501793	See ECN	VKN	Added the M Changed t_T Switching C Updated the
*F	2896585	03/20/2010	NJY	Removed o diagram, da section.

Products

Automotive	cypress.com/go/automotive
Clocks & Buffers	cypress.com/go/clocks
Interface	cypress.com/go/interface
Lighting & Power Control	cypress.com/go/powerpsoc
	cypress.com/go/plc
Memory	cypress.com/go/memory
Optical & Image Sensing	cypress.com/go/image
PSoC	cypress.com/go/psoc
Touch Sensing	cypress.com/go/touch
USB Controllers	cypress.com/go/USB
Wireless/RF	cypress.com/go/wireless

Document Number: 38-05539 Rev. *F