

IRFI4410ZPBF-VB Datasheet

N-Channel 100 V (D-S) 175 °C MOSFET

PRODUCT SUMMARY	
V_{DS} (V)	100
$R_{DS(on)}$ (Ω) at $V_{GS} = 10$ V	0.0038
I_D (A)	120
Configuration	Single

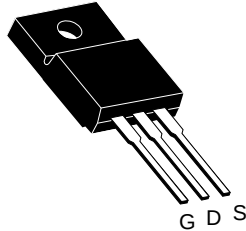
FEATURES

- TrenchFET® Power MOSFET
- Package with Low Thermal Resistance
- 100 % R_g and UIS Tested

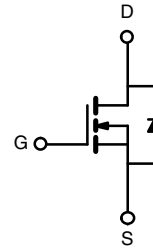


RoHS
COMPLIANT
HALOGEN
FREE

TO-220 FULLPAK



Top View



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted)				
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current	$T_C = 25\text{ }^\circ\text{C}^a$	I_D	120	A
	$T_C = 125\text{ }^\circ\text{C}$		102	
Continuous Source Current (Diode Conduction) ^a		I_S	120	
Pulsed Drain Current ^b		I_{DM}	480	
Single Pulse Avalanche Current	$L = 0.1\text{ mH}$	I_{AS}	73	
Single Pulse Avalanche Energy		E_{AS}	266	mJ
Maximum Power Dissipation ^b	$T_C = 25\text{ }^\circ\text{C}$	P_D	84	W
	$T_C = 125\text{ }^\circ\text{C}$		35	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to + 175	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS				
PARAMETER		SYMBOL	LIMIT	UNIT
Junction-to-Ambient	PCB Mount ^c	R_{thJA}	40	$^\circ\text{C/W}$
Junction-to-Case (Drain)		R_{thJC}	0.6	

Notes

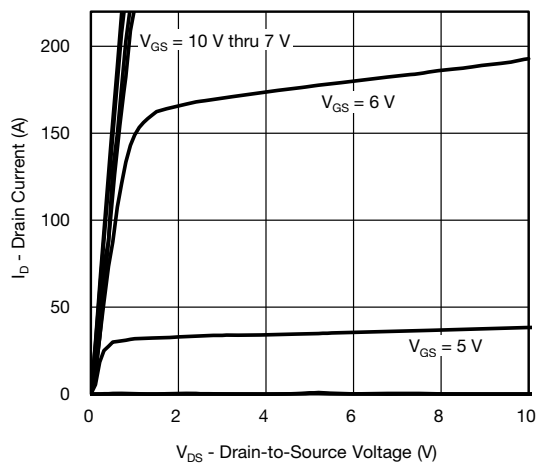
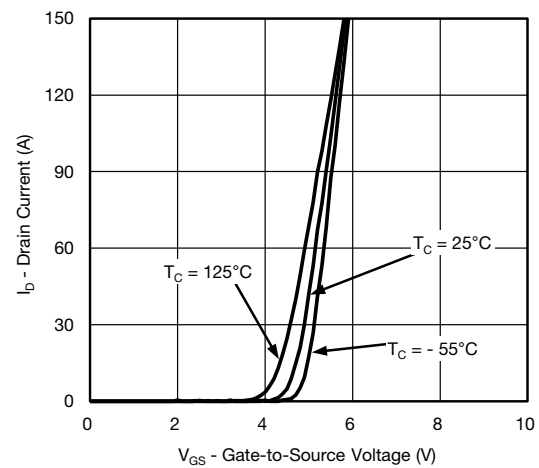
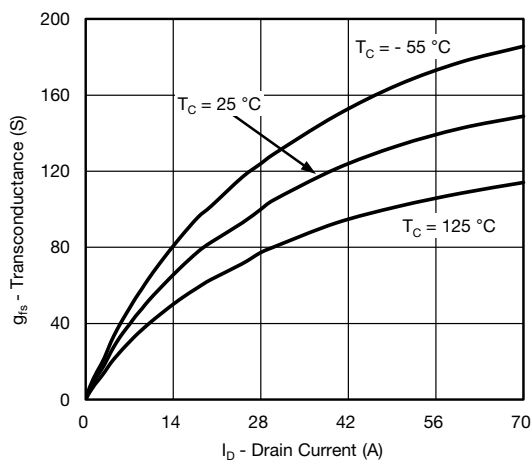
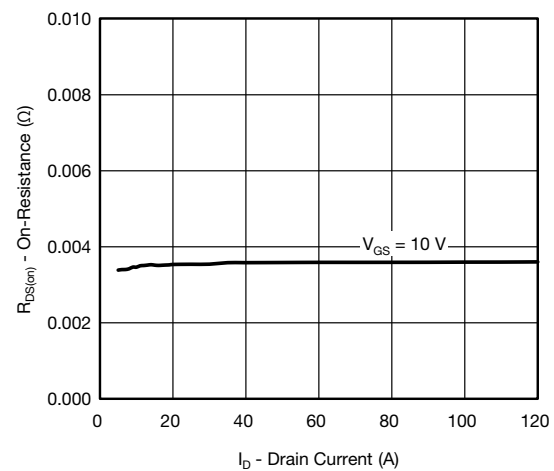
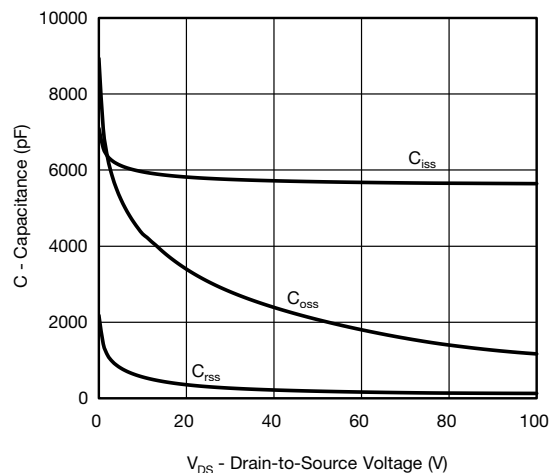
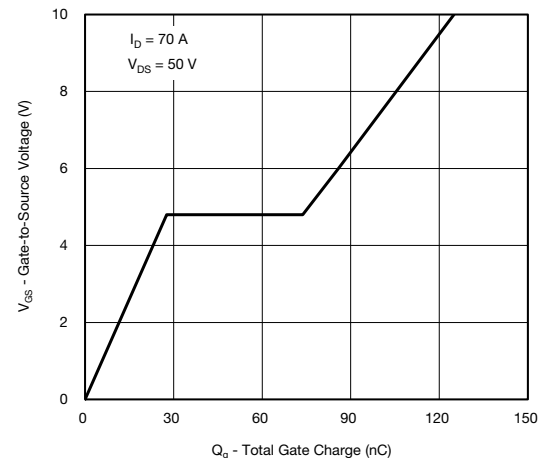
- Package limited.
- Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
- When mounted on 1" square PCB (FR-4 material).
- Parametric verification ongoing.

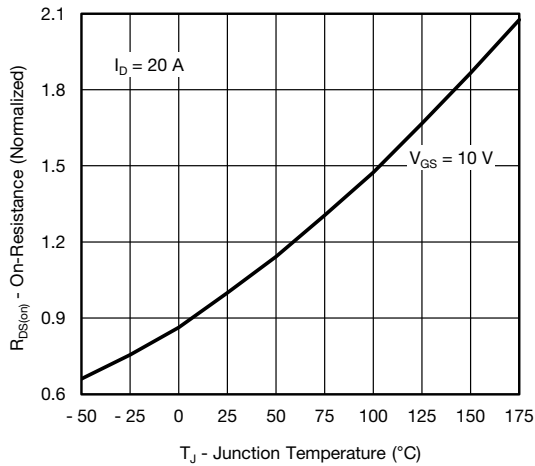
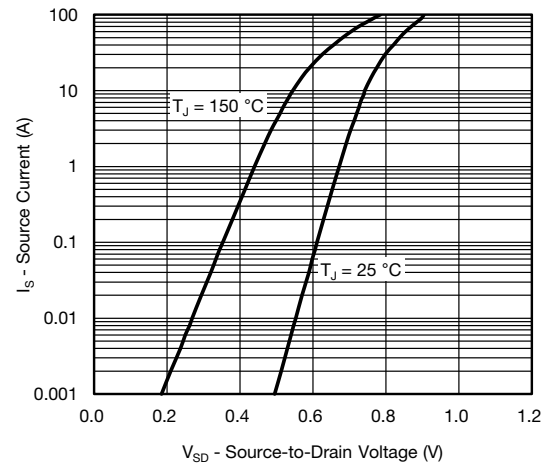
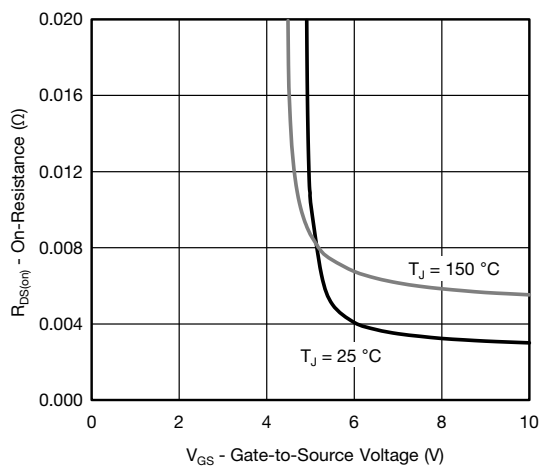
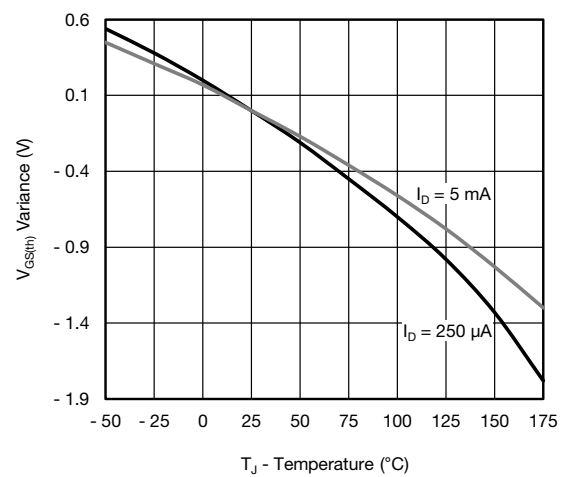
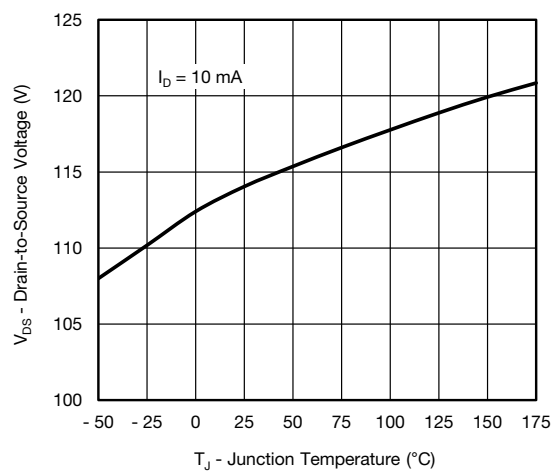
SPECIFICATIONS (T _C = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0, I _D = 250 μA		100	-	-	V
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		2.5	3.0	3.5	
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V	V _{DS} = 100 V	-	-	1	μA
		V _{GS} = 0 V	V _{DS} = 100 V, T _J = 125 °C	-	-	50	
		V _{GS} = 0 V	V _{DS} = 100 V, T _J = 175 °C	-	-	500	
On-State Drain Current ^a	I _{D(on)}	V _{GS} = 10 V	V _{DS} ≥ 5 V	120	-	-	A
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 10 V	I _D = 20 A	-	0.0038	-	Ω
		V _{GS} = 10 V	I _D = 20 A, T _J = 125 °C	-	0.0064	-	
		V _{GS} = 10 V	I _D = 20 A, T _J = 175 °C	-	0.0080	-	
Forward Transconductance ^b	g _{fs}	V _{DS} = 15 V, I _D = 20 A		-	82	-	S
Dynamic ^b							
Input Capacitance	C _{iss}	V _{GS} = 0 V	V _{DS} = 25 V, f = 1 MHz	-	5780	7230	pF
Output Capacitance	C _{oss}			-	3070	3840	
Reverse Transfer Capacitance	C _{rss}			-	305	385	
Total Gate Charge ^c	Q _g	V _{GS} = 10 V	V _{DS} = 50 V, I _D = 70 A	-	125	190	nC
Gate-Source Charge ^c	Q _{gs}			-	28	-	
Gate-Drain Charge ^c	Q _{gd}			-	46	-	
Gate Resistance	R _g	f = 1 MHz		1.6	3.3	5	Ω
Turn-On Delay Time ^c	t _{d(on)}	V _{DD} = 50 V, R _L = 0.7 Ω I _D ≅ 70 A, V _{GEN} = 10 V, R _g = 1 Ω		-	16	25	ns
Rise Time ^c	t _r			-	110	165	
Turn-Off Delay Time ^c	t _{d(off)}			-	40	60	
Fall Time ^c	t _f			-	12	20	
Source-Drain Diode Ratings and Characteristics ^b							
Pulsed Current ^a	I _{SM}			-	-	480	A
Forward Voltage	V _{SD}	I _F = 100 A, V _{GS} = 0		-	0.9	1.5	V

Notes

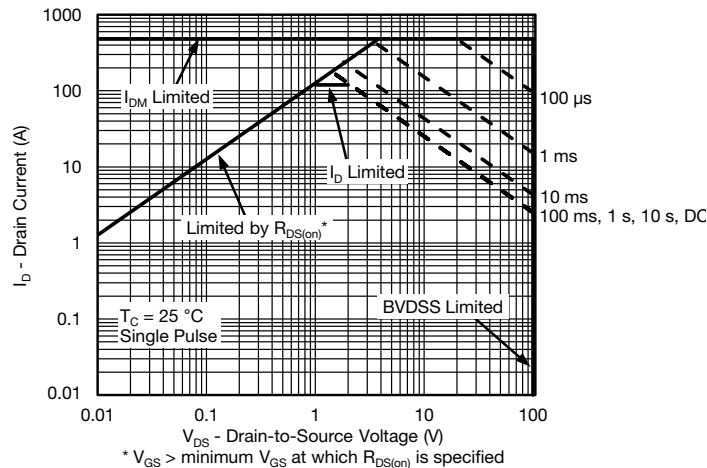
- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
 b. Guaranteed by design, not subject to production testing.
 c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

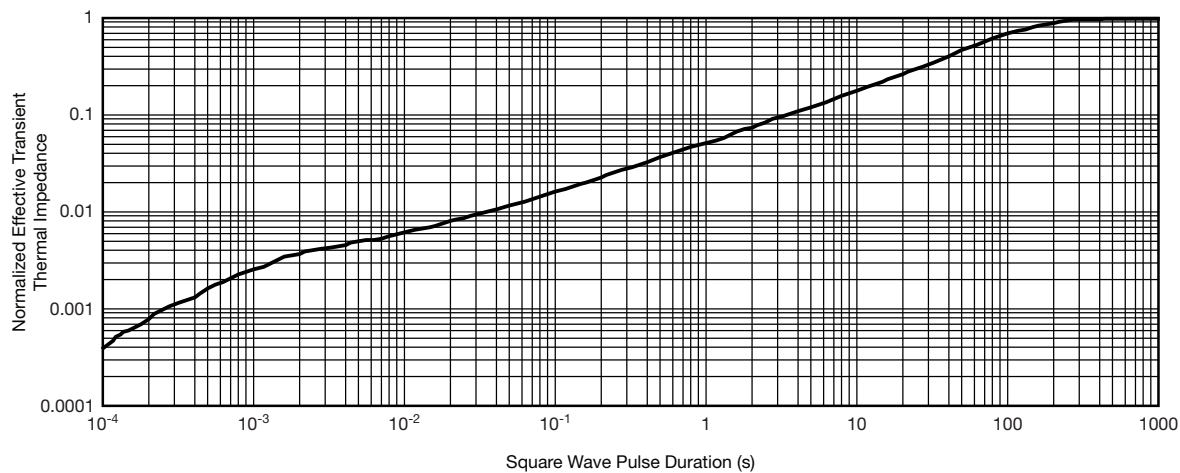
TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

Output Characteristics

Transfer Characteristics

Transconductance

On-Resistance vs. Drain Current

Capacitance

Gate Charge

TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

On-Resistance vs. Junction Temperature

Source Drain Diode Forward Voltage

On-Resistance vs. Gate-to-Source Voltage

Threshold Voltage

Drain Source Breakdown vs. Junction Temperature

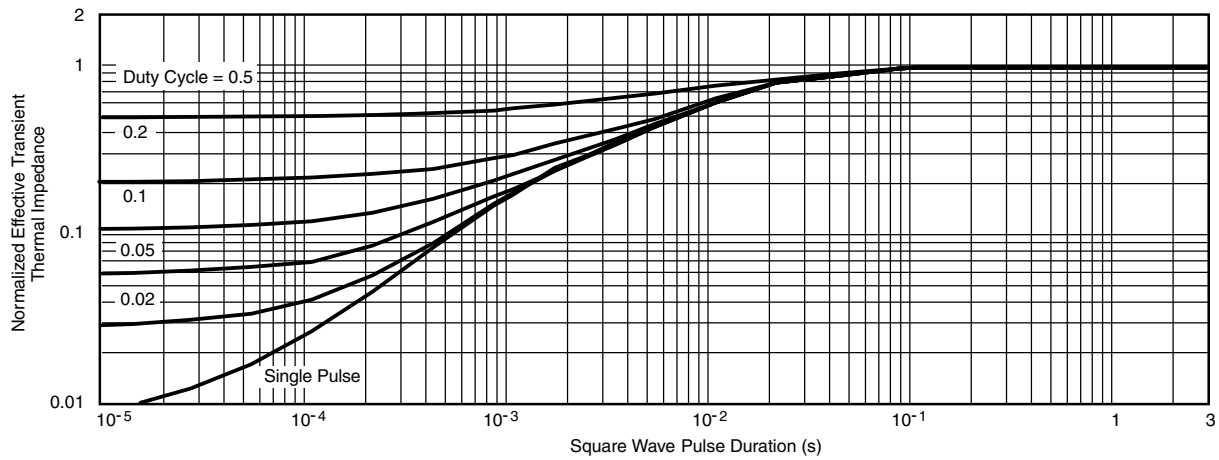
THERMAL RATINGS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)



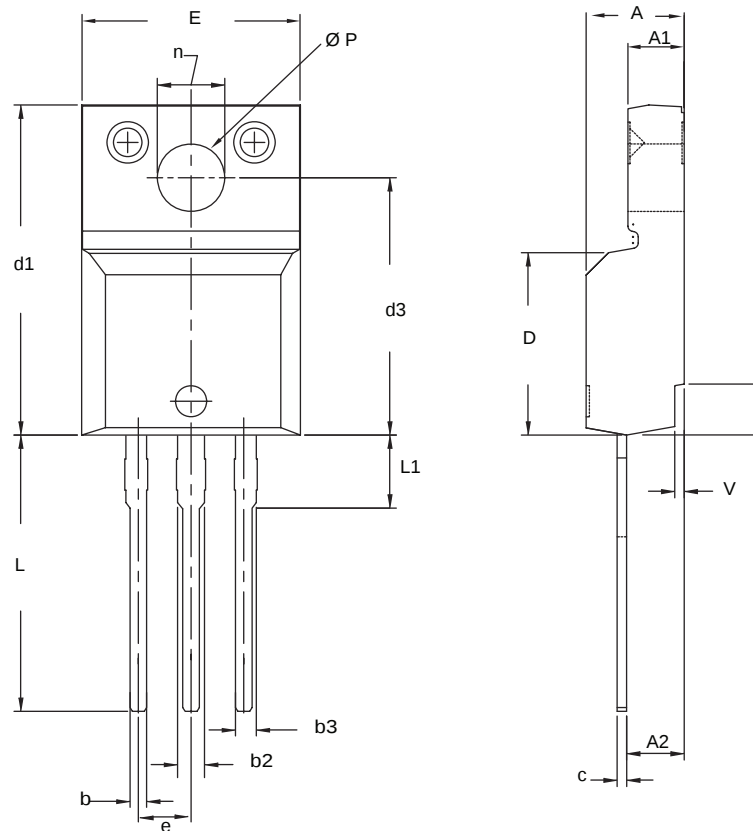
Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient

THERMAL RATINGS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

Normalized Thermal Transient Impedance, Junction-to-Case
Note

- The characteristics shown in the two graphs
 - Normalized Transient Thermal Impedance Junction to Ambient ($25\text{ }^{\circ}\text{C}$)
 - Normalized Transient Thermal Impedance Junction to Case ($25\text{ }^{\circ}\text{C}$)
- are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

TO-220 FULLPAK (HIGH VOLTAGE)

DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.570	4.830	0.180	0.190
A1	2.570	2.830	0.101	0.111
A2	2.510	2.850	0.099	0.112
b	0.622	0.890	0.024	0.035
b2	1.229	1.400	0.048	0.055
b3	1.229	1.400	0.048	0.055
c	0.440	0.629	0.017	0.025
D	8.650	9.800	0.341	0.386
d1	15.88	16.120	0.622	0.635
d3	12.300	12.920	0.484	0.509
E	10.360	10.630	0.408	0.419
e	2.54 BSC		0.100 BSC	
L	13.200	13.730	0.520	0.541
L1	3.100	3.500	0.122	0.138
n	6.050	6.150	0.238	0.242
Ø P	3.050	3.450	0.120	0.136
u	2.400	2.500	0.094	0.098
v	0.400	0.500	0.016	0.020

ECN: X09-0126-Rev. B, 26-Oct-09
 DWG: 5972

Notes

1. To be used only for process drawing.
2. These dimensions apply to all TO-220, FULLPAK leadframe versions 3 leads.
3. All critical dimensions should C meet $C_{pk} > 1.33$.
4. All dimensions include burrs and plating thickness.
5. No chipping or package damage.

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