

FDMS4D5N08LC

MOSFET, N-Channel Shielded Gate, POWER trench[®]

80 V, 116 A, 4.2 m Ω

General Description

This N-Channel MV MOSFET is produced using ON Semiconductor's advanced POWER trench[®] process that incorporates Shielded Gate technology. This process has been optimized to minimise on-state resistance and yet maintain superior switching performance with best in class soft body diode.

Features

- Shielded Gate MOSFET Technology
- Max $r_{DS(on)}$ = 4.2 m Ω at V_{GS} = 10 V, I_D = 37 A
- Max $r_{DS(on)}$ = 6.1 m Ω at V_{GS} = 4.5 V, I_D = 29 A
- 50% Lower Q_{rr} than Other MOSFET Suppliers
- Lowers Switching Noise/EMI
- MSL1 Robust Package Design
- 100% UIL Tested
- RoHS Compliant

Typical Applications

- Primary DC-DC MOSFET
- Synchronous Rectifier in DC-DC and AC-DC
- Motor Drive
- Solar

MOSFET MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{DS}	Drain to Source Voltage	80	V
V_{GS}	Gate to Source Voltage	± 20	V
I_D	Drain Current – Continuous T_C = 25°C (Note 5)	116	A
	– Continuous T_C = 100°C (Note 5)	73	
	– Continuous T_A = 25°C (Note 1a)	17	
	– Pulsed (Note 4)	633	
E_{AS}	Single Pulse Avalanche Energy (Note 3)	384	mJ
P_D	Power dissipation T_C = 25°C	113.6	W
	Power dissipation T_A = 25°C (Note 1a)	2.5	
T_J , T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	°C

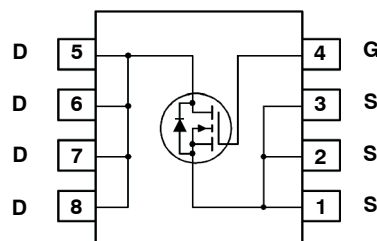
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.



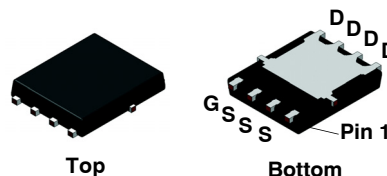
ON Semiconductor[®]

www.onsemi.com

ELECTRICAL CONNECTION

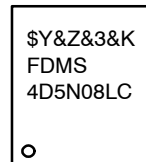


N-Channel MOSFET



Power 56
(PQFN8 5x6)
CASE 483AE

MARKING DIAGRAM



\$Y = ON Semiconductor Logo
&Z = Assembly Plant Code
&3 = Numeric Date Code
&K = Lot Code
FDMS4D5N08LC = Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

FDMS4D5N08LC

THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.1	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	50	

PACKAGE MARKING AND ORDERING INFORMATION

Device Marking	Device	Package	Shipping [†]
FDMS4D5N08LC	FDMS4D5N08LC	PQFN8 5×6 (Pb-Free/Halogen Free)	3000 Units/ Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\ \mu\text{A}$, $V_{GS} = 0\ \text{V}$	80			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, referenced to 25°C		66		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 64\ \text{V}$, $V_{GS} = 0\ \text{V}$			1	μA
I_{GSS}	Gate-to-Source Leakage Current	$V_{GS} = \pm 20\ \text{V}$, $V_{DS} = 0\ \text{V}$			± 100	nA

ON CHARACTERISTICS

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 210\ \mu\text{A}$	1.0	1.4	2.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 210\ \mu\text{A}$, referenced to 25°C		-5.1		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\ \text{V}$, $I_D = 37\ \text{A}$		3.2	4.2	m Ω
		$V_{GS} = 4.5\ \text{V}$, $I_D = 29\ \text{A}$		4.5	6.1	
		$V_{GS} = 10\ \text{V}$, $I_D = 37\ \text{A}$, $T_J = 125^\circ\text{C}$		5.7	7.5	
g_{FS}	Forward Transconductance	$V_{DS} = 5\ \text{V}$, $I_D = 37\ \text{A}$		135		S

DYNAMIC CHARACTERISTICS

C_{iss}	Input Capacitance	$V_{DS} = 40\ \text{V}$, $V_{GS} = 0\ \text{V}$, $f = 1\ \text{MHz}$		3640	5100	pF
C_{oss}	Output Capacitance			834	1170	
C_{rss}	Reverse Transfer Capacitance			39	65	
R_g	Gate Resistance		0.1	0.6	1.1	Ω

SWITCHING CHARACTERISTICS

$t_{d(on)}$	Turn – On Delay Time	$V_{DD} = 40\ \text{V}$, $I_D = 37\ \text{A}$, $V_{GS} = 10\ \text{V}$, $R_{GEN} = 6\ \Omega$		13	23	ns
t_r	Rise Time			19	34	
$t_{D(off)}$	Turn – Off Delay Time			59	94	
t_f	Fall Time			17	30	
Q_g	Total Gate Charge	$V_{GS} = 0\ \text{V}$ to $10\ \text{V}$	$V_{DD} = 40\ \text{V}$, $I_D = 37\ \text{A}$	51	71	nC
Q_g	Total Gate Charge	$V_{GS} = 0\ \text{V}$ to $4.5\ \text{V}$		24	34	
Q_{gs}	Gate to Source Charge			8		
Q_{gd}	Gate to Drain “Miller” Charge			6		
Q_{oss}	Output Charge	$V_{DD} = 40\ \text{V}$, $V_{GS} = 0\ \text{V}$		51		nC
Q_{sync}	Total Gate Charge Sync.	$V_{DS} = 0\ \text{V}$, $I_D = 37\ \text{A}$		46		

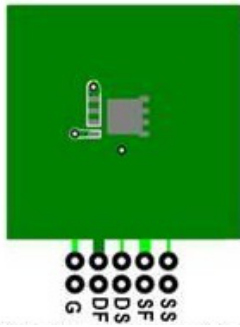
ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
DRAIN-SOURCE DIODE CHARACTERISTICS						
V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 2.1\text{ A}$ (Note 2)		0.7	1.2	V
		$V_{GS} = 0\text{ V}, I_S = 37\text{ A}$ (Note 2)		0.8	1.3	
t_{rr}	Reverse Recovery Time	$I_F = 18\text{ A}, di/dt = 300\text{ A}/\mu\text{s}$		22	36	ns
Q_{rr}	Reverse Recovery Charge			38	61	nC
t_{rr}	Reverse Recovery Time	$I_F = 18\text{ A}, di/dt = 1000\text{ A}/\mu\text{s}$		17	27	ns
Q_{rr}	Reverse Recovery Charge			82	132	nC

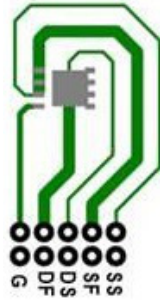
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

- $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 × 1.5 in. board of FR-4 material. $R_{\theta CA}$ is determined by the user's board design.



a) $50^\circ\text{C}/\text{W}$ when mounted on a 1 in² pad of 2 oz copper.



b) $125^\circ\text{C}/\text{W}$ when mounted on a minimum pad of 2 oz copper.

- Pulse Test: Pulse Width < 300 μs , Duty cycle < 2.0%.
- E_{AS} of 384 mJ is based on starting $T_J = 25^\circ\text{C}$; N-ch: $L = 3\text{ mH}$, $I_{AS} = 16\text{ A}$, $V_{DD} = 72\text{ V}$, $V_{GS} = 10\text{ V}$. 100% tested at $L = 0.1\text{ mH}$, $I_{AS} = 41\text{ A}$, $V_{GS} = 10\text{ V}$.
- Pulsed I_D please refer to Figure 11 SOA graph for more details.
- Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

TYPICAL CHARACTERISTICS $T_J = 25^\circ\text{C}$ unless otherwise noted

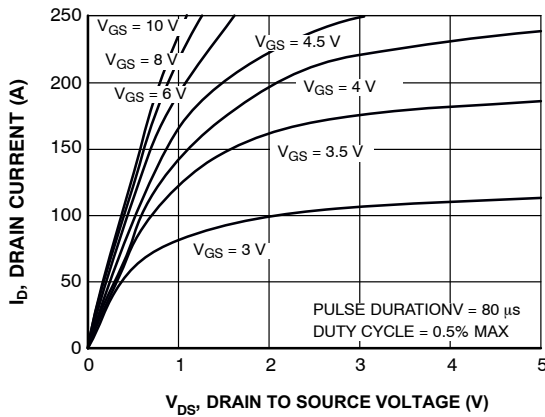


Figure 1. On Region Characteristics

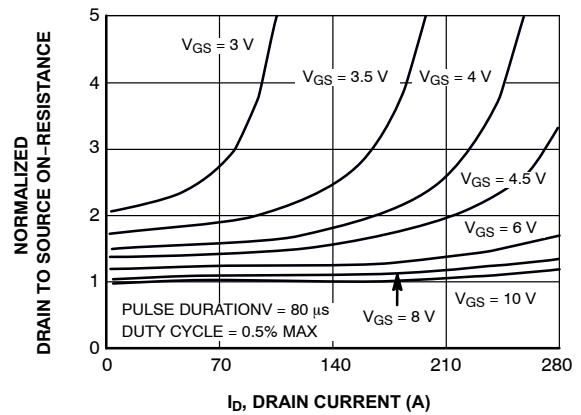


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

TYPICAL CHARACTERISTICS $T_J = 25^\circ\text{C}$ unless otherwise noted (continued)

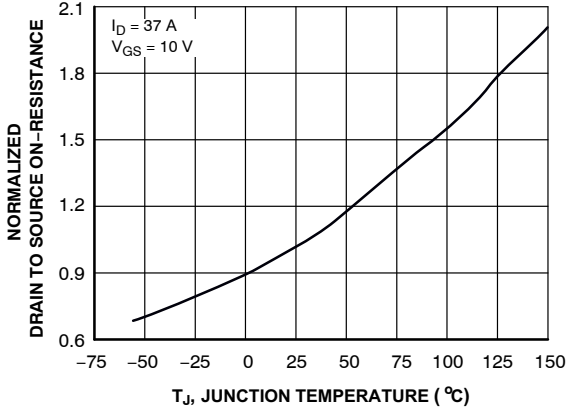


Figure 3. Normalized On Resistance vs. Junction Temperature

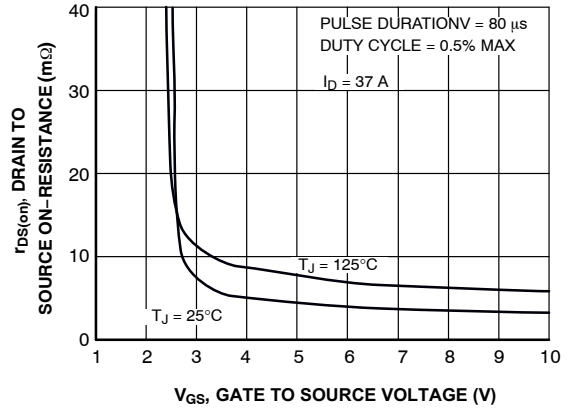


Figure 4. On-Resistance vs. Gate to Source Voltage

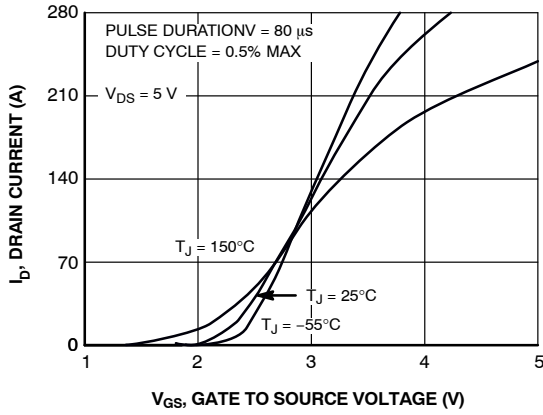


Figure 5. Transfer Characteristics

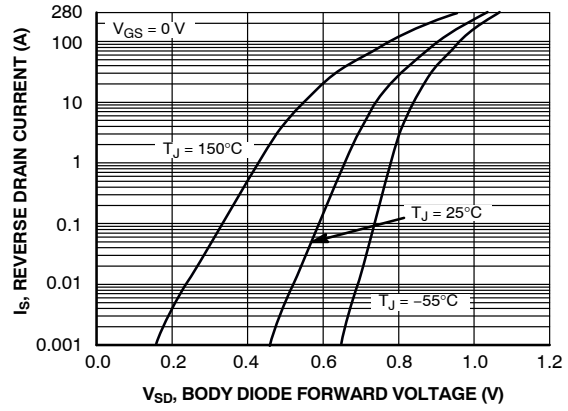


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

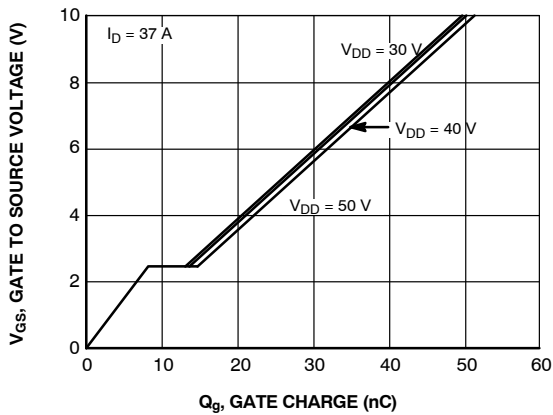


Figure 7. Gate Charge Characteristics

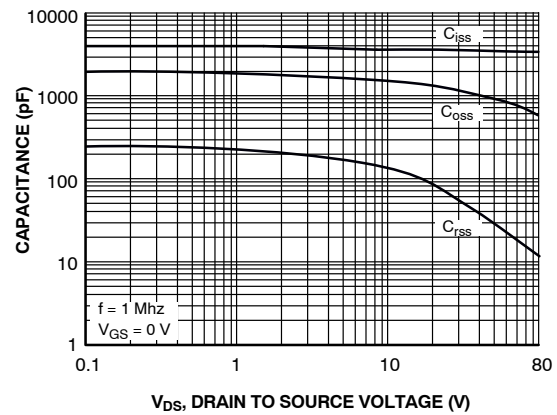


Figure 8. Capacitance vs. Drain to Source Voltage

TYPICAL CHARACTERISTICS $T_J = 25^\circ\text{C}$ unless otherwise noted (continued)

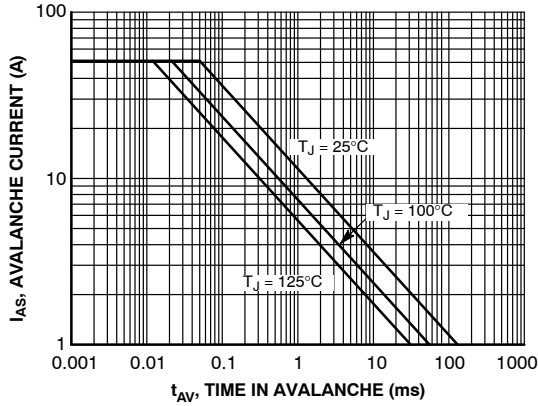


Figure 9. Unclamped Inductive Switching Capability

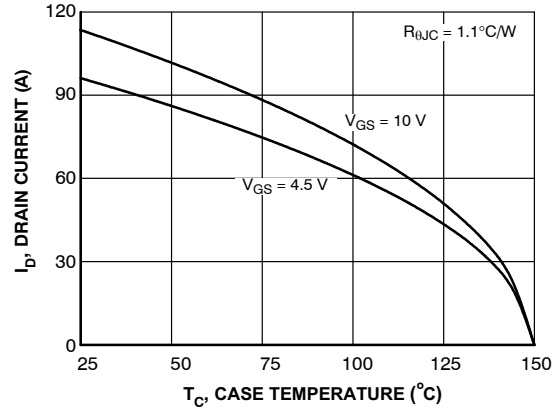


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

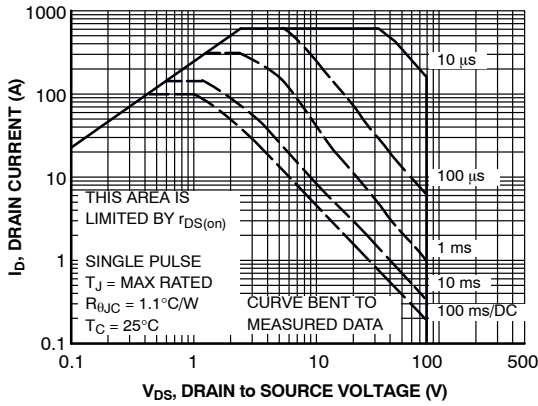


Figure 11. Unclamped Inductive Switching Capability

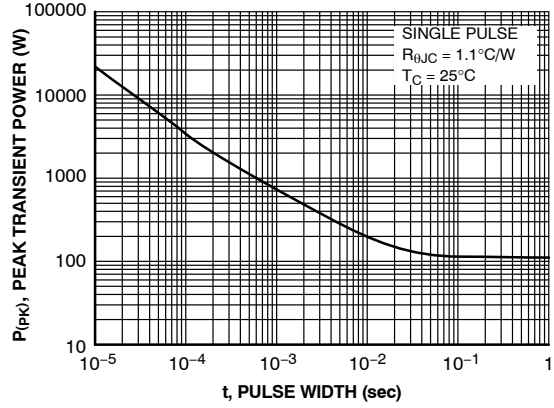


Figure 12. Maximum Continuous Drain Current vs. Case Temperature

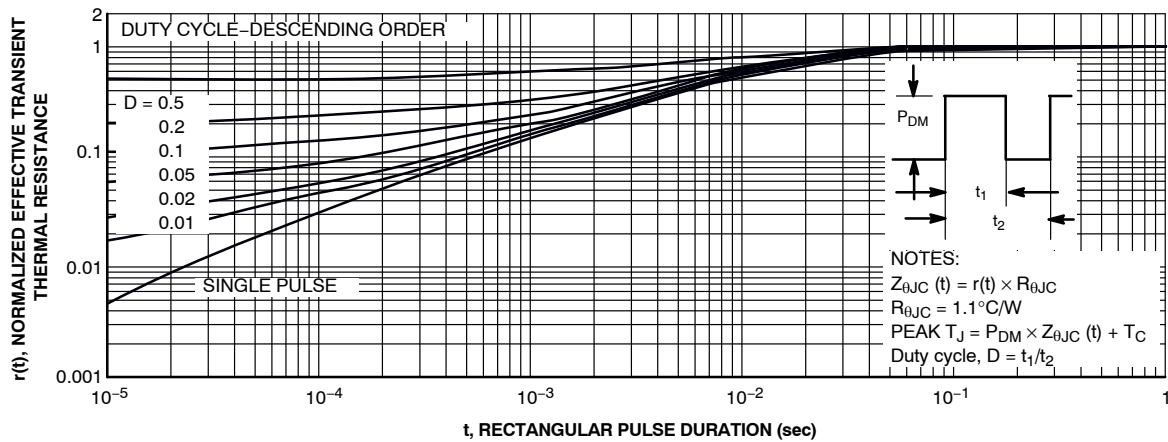
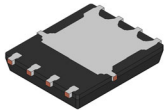
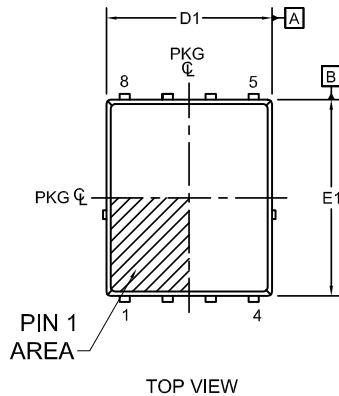


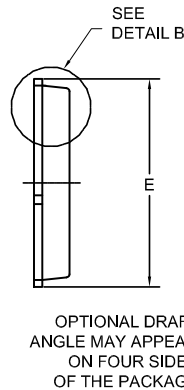
Figure 13. Junction-to-Case Transient Thermal Response Curve


PQFN8 5X6, 1.27P
CASE 483AE
ISSUE C

DATE 21 JAN 2022

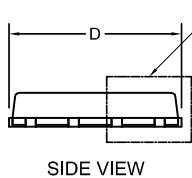


TOP VIEW

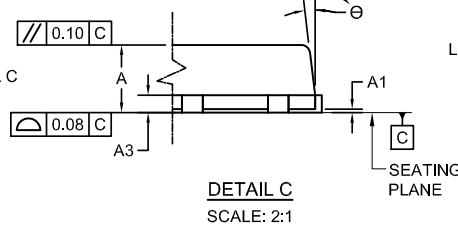
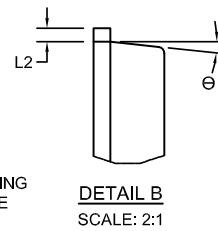
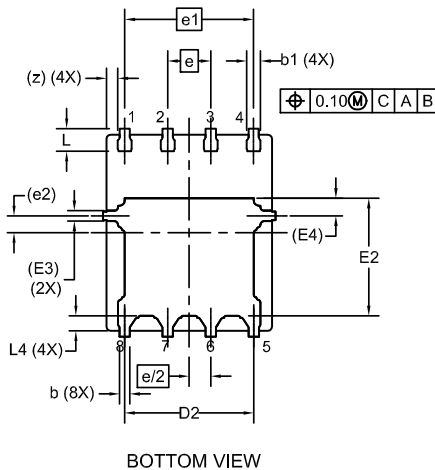

OPTIONAL DRAFT
ANGLE MAY APPEAR
ON FOUR SIDES
OF THE PACKAGE

NOTES:

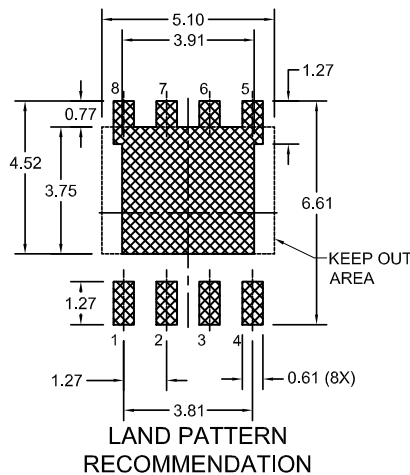
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
6. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.



SIDE VIEW


DETAIL C
SCALE: 2:1

DETAIL B
SCALE: 2:1


BOTTOM VIEW


LAND PATTERN
RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERM/D.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	-	0.05
b	0.21	0.31	0.41
b1	0.31	0.41	0.51
A3	0.15	0.25	0.35
D	4.90	5.00	5.20
D1	4.80	4.90	5.00
D2	3.61	3.82	3.96
E	5.90	6.15	6.25
E1	5.70	5.80	5.90
E2	3.38	3.48	3.78
E3	0.30 REF		
E4	0.52 REF		
e	1.27 BSC		
e/2	0.635 BSC		
e1	3.81 BSC		
e2	0.50 REF		
L	0.51	0.66	0.76
L2	0.05	0.18	0.30
L4	0.34	0.44	0.54
z	0.34 REF		
Θ	0°	-	12°

DOCUMENT NUMBER: 98AON13655G

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DESCRIPTION: PQFN8 5X6, 1.27P

PAGE 1 OF 1

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