

P-channel Enhancement Mode Power MOSFET

Features

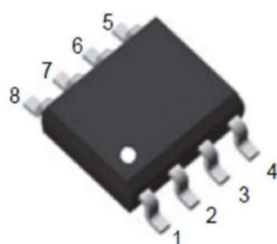
- $V_{DS} = -20V$, $I_D = -13A$
 $R_{DS(ON)} < 17\text{ m}\Omega$ @ $V_{GS} = -4.5V$
 $R_{DS(ON)} < 20\text{ m}\Omega$ @ $V_{GS} = -2.5V$

General Features

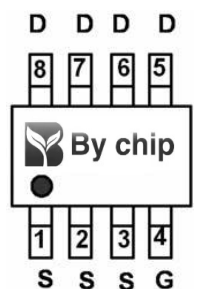
- Advanced Trench Technology
- Provide Excellent $R_{DS(ON)}$ and Low Gate Charge
- Lead Free and Green Available

100% UIS TESTED!

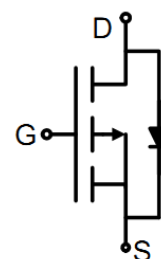
100% ΔV_{ds} TESTED!



SOP-8



pin assignment



Schematic diagram

■ Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Maximum	Unit
Drain-source Voltage		V_{DS}	-20	V
Gate-source Voltage		V_{GS}	± 10	V
Drain Current	$T_A = 25^\circ\text{C}$ @ Steady State	I_D	-13	A
	$T_A = 70^\circ\text{C}$ @ Steady State		-10.4	
Pulsed Drain Current ^A		I_{DM}	-55	A
Total Power Dissipation @ $T_A = 25^\circ\text{C}$		P_D	3.0	W
Thermal Resistance Junction-to-Ambient @ Steady State ^B		$R_{\theta JA}$	42	$^\circ\text{C}/\text{W}$
Junction and Storage Temperature Range		T_J, T_{STG}	-55 ~ +150	$^\circ\text{C}$

■ Electrical Characteristics (T_J=25℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D =-250μA	-20			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-20V, V _{GS} =0V, T _C =25℃			-1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} = ±10V, V _{DS} =0V			±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D =-250μA	-0.4		-2.0	V
Static Drain-Source On-Resistance	R _{DS(ON)}	V _{GS} = -4.5V, I _D =-10A			17	mΩ
		V _{GS} = -2.5V, I _D =-6.5A			20	
		V _{GS} = -1.8V, I _D =-4.0A			26	
Diode Forward Voltage	V _{SD}	I _S =-13A, V _{GS} =0V			-1.2	V
Maximum Body-Diode Continuous Current	I _S				-13	A
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =-10V, V _{GS} =0V, f=1MHZ		2992		pF
Output Capacitance	C _{oss}			330		
Reverse Transfer Capacitance	C _{rss}			272		
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =-10V, V _{DS} =-15V, I _D =-9.1A		72.8		nC
Gate Source Charge	Q _{gs}			6.6		
Gate Drain Charge	Q _{gd}			10.1		
Reverse Recovery Charge	Q _{rr}	I _F =-6A, di/dt=100A/us		34		
Reverse Recovery Time	t _{rr}			67		
Turn-on Delay Time	t _{D(on)}	V _{GS} =-10V, V _{DS} =-15V, I _D =-6A, R _{GEN} =2.5Ω		7		ns
Turn-on Rise Time	t _r			33		
Turn-off Delay Time	t _{D(off)}			130		
Turn-off Fall Time	t _f			132		

A. Pulse Test: Pulse Width≤300us, Duty cycle ≤2%.

B. R_{θJA} is the sum of the junction-to-lead and lead-to-ambient thermal resistance, where the lead thermal reference is defined as the solder mounting surface of the drain pins. R_{θJL} is guaranteed by design, while R_{θJA} is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.

■ Typical Performance Characteristics

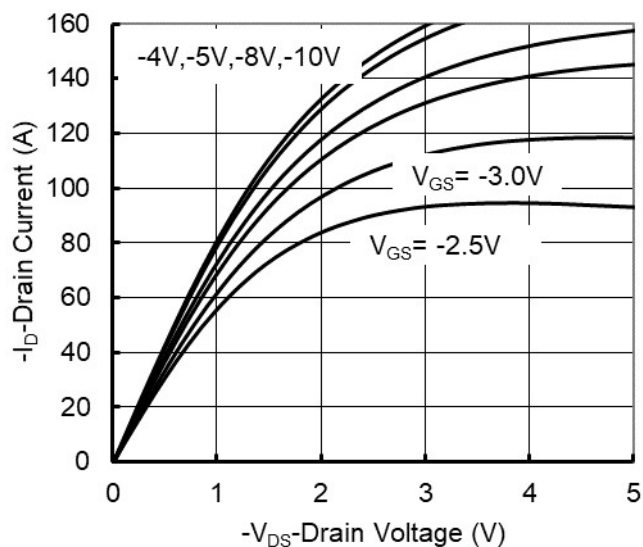


Figure 1. Output Characteristics

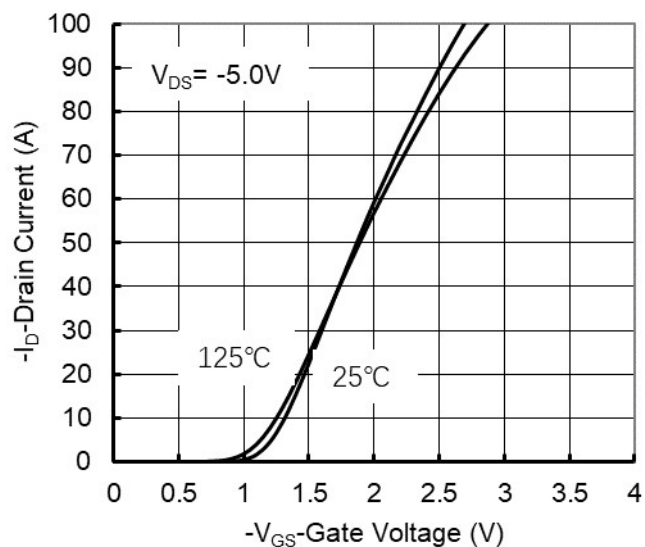


Figure 2. Transfer Characteristics

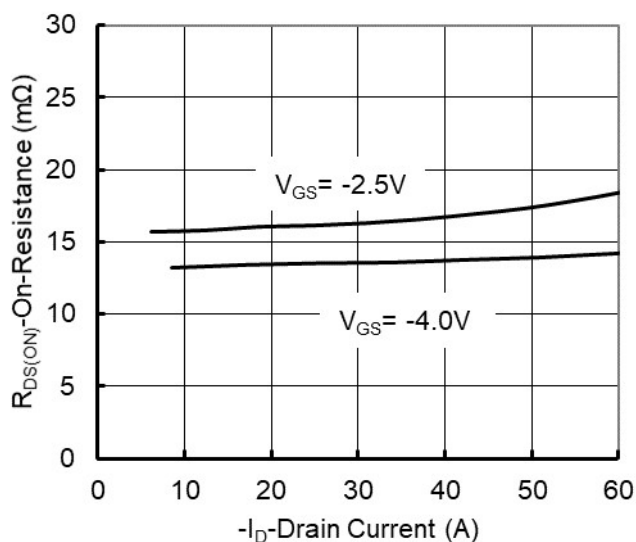


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

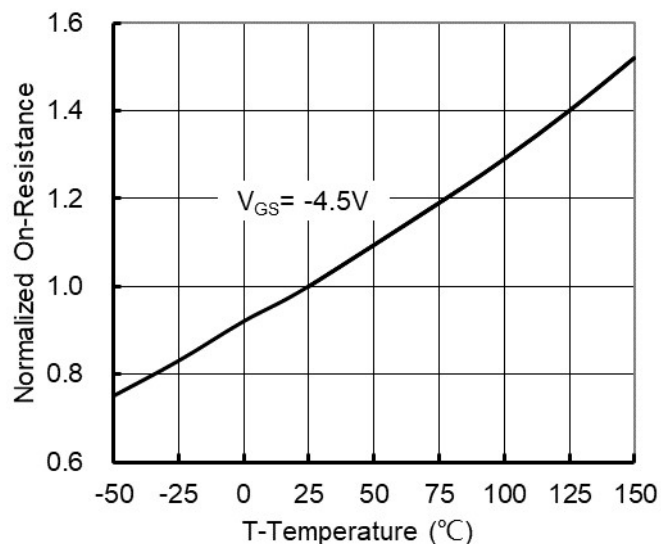


Figure 4. On-Resistance vs. Junction Temperature

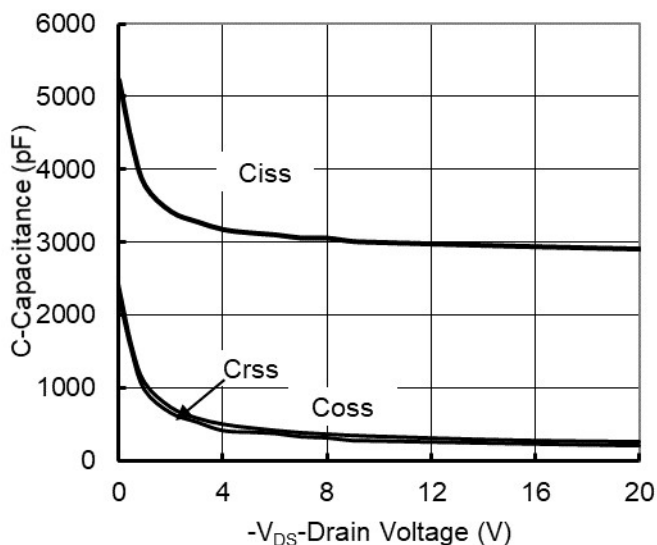


Figure 5. Capacitance Characteristics

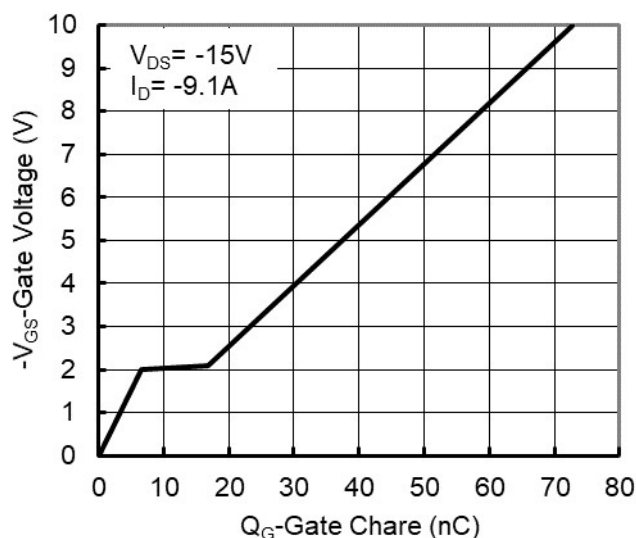


Figure 6. Gate Charge

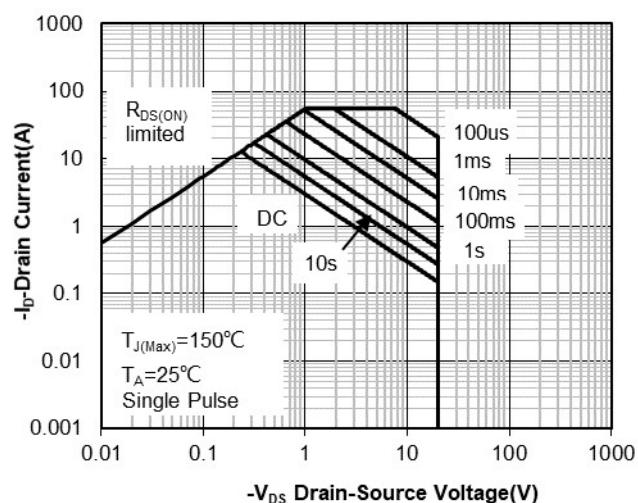


Figure 7. Safe Operation Area

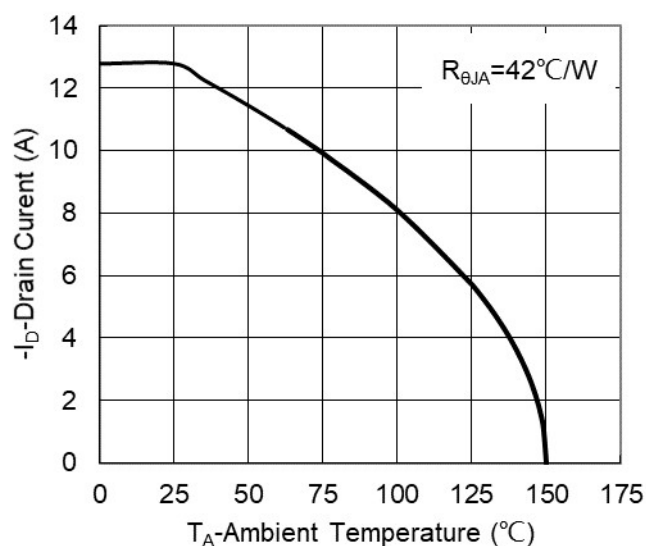


Figure 8. Maximum Continuous Drain Current vs Ambient Temperature

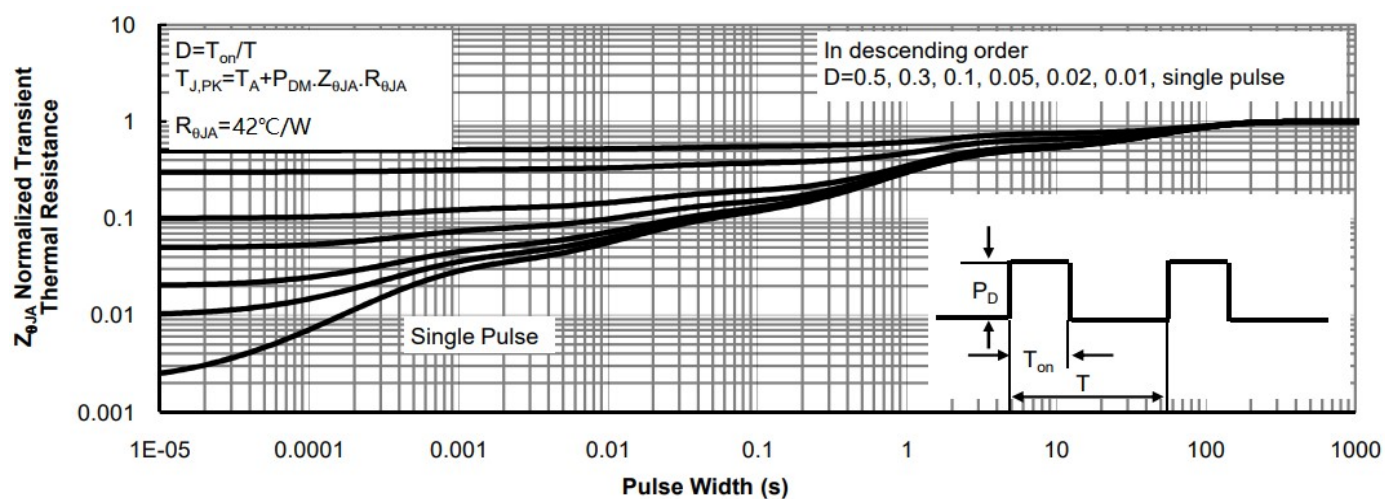
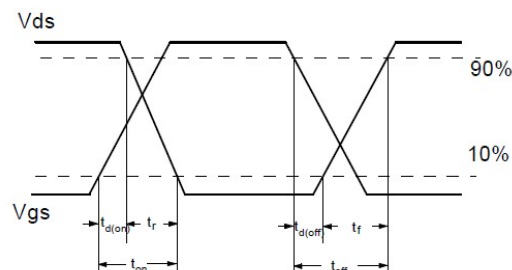
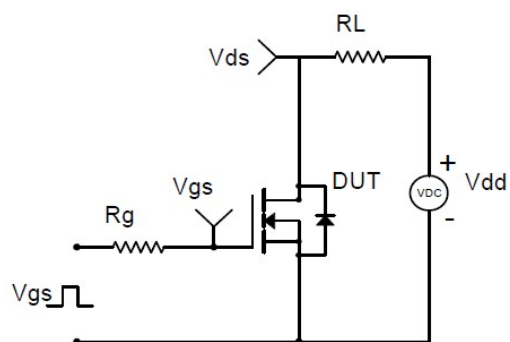
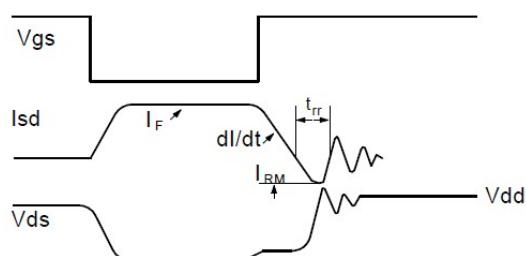
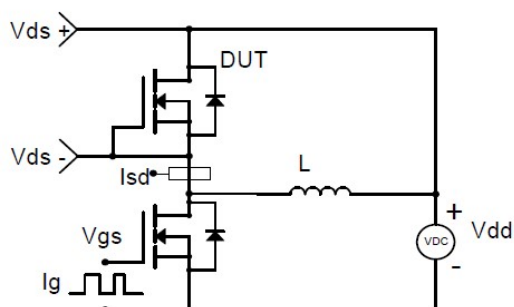


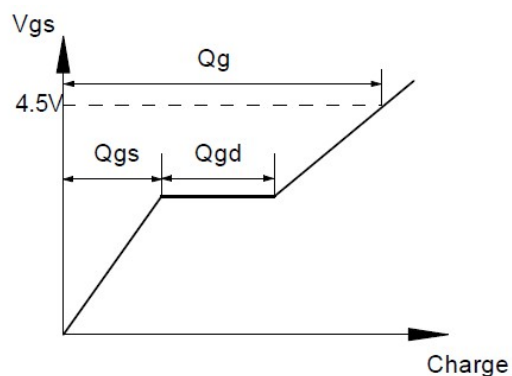
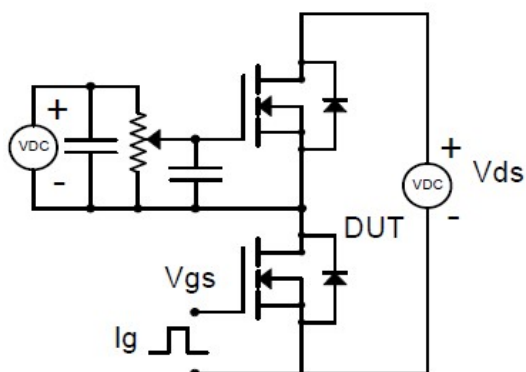
Figure 9. Normalized Maximum Transient Thermal Impedance



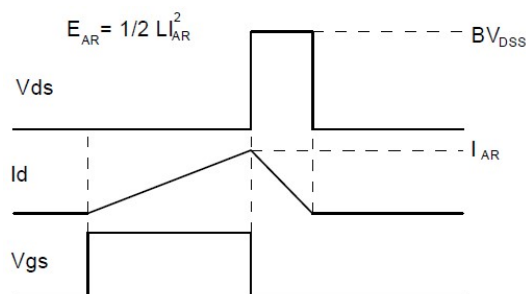
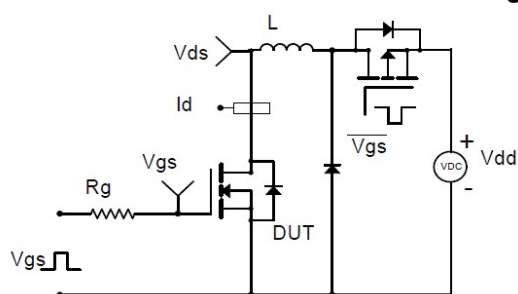
Resistive Switching Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



Gate Charge Test Circuit & Waveform



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms