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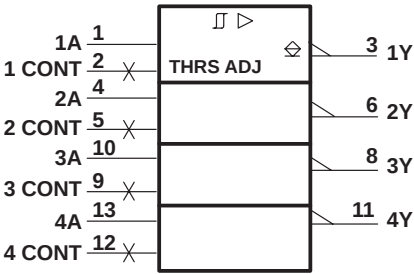
1

MC1489, MC1489A, SN55189, SN55189A, SN75189, SN75189A

QUADRUPLE LINE RECEIVERS

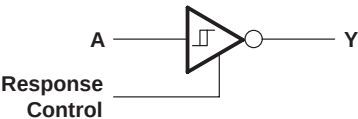
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logic symbol†

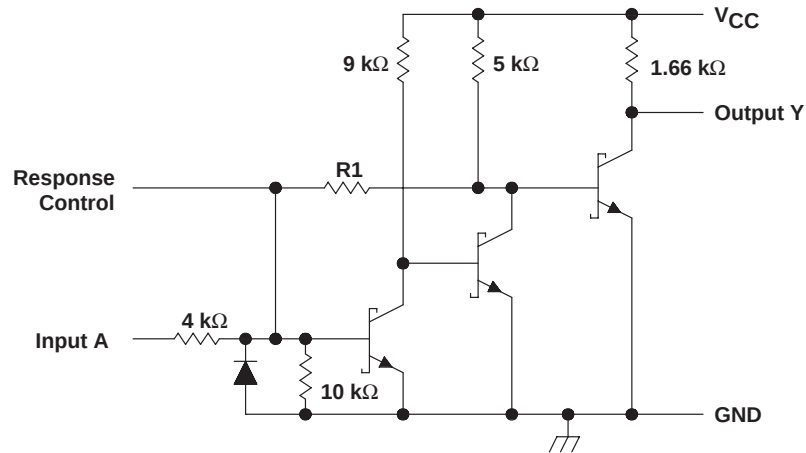


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, N, NS, and W packages.

logic diagram (positive logic)



schematic (each receiver)



	MC1489 SN55189 SN75189	MC1489A SN55189A SN75189A
R1	8.4 kΩ	1.84 kΩ

Resistor values shown are nominal.

MC1489, MC1489A, SN55189, SN55189A, SN75189, SN75189A QUADRUPLE LINE RECEIVERS

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absolute maximum ratings over operating free-air temperature (unless otherwise noted)[†]

Supply voltage, V_{CC} (see Note 1)	10 V
Input voltage, V_I	± 30 V
Output voltage, V_O	20 mA
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A : SN55189, SN55189A	-55°C to 125°C
MC1489, MC1489A, SN75189, SN75189A	0°C to 70°C
Storage temperature range, T_{stg}	-65°C to 150°C
Case temperature for 60 seconds, FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J or W package	300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, N, or NS package	260°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to the network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^{\circ}\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^{\circ}\text{C}$	$T_A = 70^{\circ}\text{C}$ POWER RATING	$T_A = 125^{\circ}\text{C}$ POWER RATING
D	950 mW	7.6 mW/ $^{\circ}\text{C}$	608 mW	N/A
FK	1375 mW	11.0 mW/ $^{\circ}\text{C}$	880 mW	275 mW
J [‡]	1375 mW	11.0 mW/ $^{\circ}\text{C}$	880 mW	275 mW
N	1150 mW	9.2 mW/ $^{\circ}\text{C}$	736 mW	N/A
NS	625 mW	4.0 mW/ $^{\circ}\text{C}$	445 mW	N/A
W	1000 mW	8.0 mW/ $^{\circ}\text{C}$	640 mW	200 mW

[‡] In the J package, SN55189 and SN55189A chips are either silver glass or alloy mounted.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.5	5	5.5	V
Input voltage, V_I	-25		25	V
High-level output current, I_{OH}			-0.5	mA
Low-level output current, I_{OL}			10	mA
Operating free-air temperature, T_A	0		70	$^{\circ}\text{C}$



MC1489, MC1489A, SN55189, SN55189A, SN75189, SN75189A QUADRUPLE LINE RECEIVERS

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electrical characteristics over operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 1\%$ (unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS†		SN55189 SN55189A			MC1489, MC1489A SN75189 SN75189A			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IT+} Positive-going input threshold voltage	1	'89	$T_A = 25^\circ\text{C}$	1	1.3	1.5	1	1.3	1.5	V
			$T_A = 0^\circ\text{C to } 70^\circ\text{C}$				0.9		1.6	
			$T_A = -55^\circ\text{C to } 125^\circ\text{C}$	0.6		1.9				
		'89A	$T_A = 25^\circ\text{C}$	1.75	1.9	2.25	1.75	1.9	2.25	
			$T_A = 0^\circ\text{C to } 70^\circ\text{C}$				1.55		2.25	
			$T_A = -55^\circ\text{C to } 125^\circ\text{C}$	1.30		2.65				
V_{IT-} Negative-going input threshold voltage	1	'89, '89A	$T_A = 25^\circ\text{C}$	0.75	1.0	1.25	0.75	1.0	1.25	V
			$T_A = 0^\circ\text{C to } 70^\circ\text{C}$				0.65		1.25	
			$T_A = -55^\circ\text{C to } 125^\circ\text{C}$	0.35		1.6				
V_{OH} High-level output voltage	1	$V_I = 0.75\text{ V}$, $I_{OH} = -0.5\text{ mA}$		2.6	4	5	2.6	4	5	V
		Input open, $I_{OH} = -0.5\text{ mA}$		2.6	4	5	2.6	4	5	
V_{OL} Low-level output voltage	1	$V_I = 3\text{ V}$, $I_{OL} = 10\text{ mA}$			0.2	0.45		0.2	0.45	V
I_{IH} High-level input current	2	$V_I = 25\text{ V}$		3.6		8.3	3.6		8.3	mA
		$V_I = 3\text{ V}$		0.43			0.43			
I_{IL} Low-level input current	2	$V_I = -25\text{ V}$		-3.6		-8.3	-3.6		-8.3	mA
		$V_I = -3\text{ V}$		-0.43			-0.43			
I_{OS} Short-circuit output current	3				-3			-3		mA
I_{CC} Supply current	2	$V_I = 5\text{ V}$, Outputs open			20	26		20	26	mA

† All characteristics are measured with the response-control terminal open.

‡ All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

switching characteristics, $V_{CC} = 5\text{ V}$, $C_L = 15\text{ pF}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low- to high-level output	4	$R_L = 3.9\text{ k}\Omega$		25	85	ns
t_{PHL} Propagation delay time, high- to low-level output		$R_L = 390\text{ }\Omega$		25	50	
t_{TLH} Transition time, low- to high-level output		$R_L = 3.9\text{ k}\Omega$		120	175	ns
t_{THL} Transition time, high- to low-level output		$R_L = 390\text{ }\Omega$		10	20	



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

PARAMETER MEASUREMENT INFORMATION†

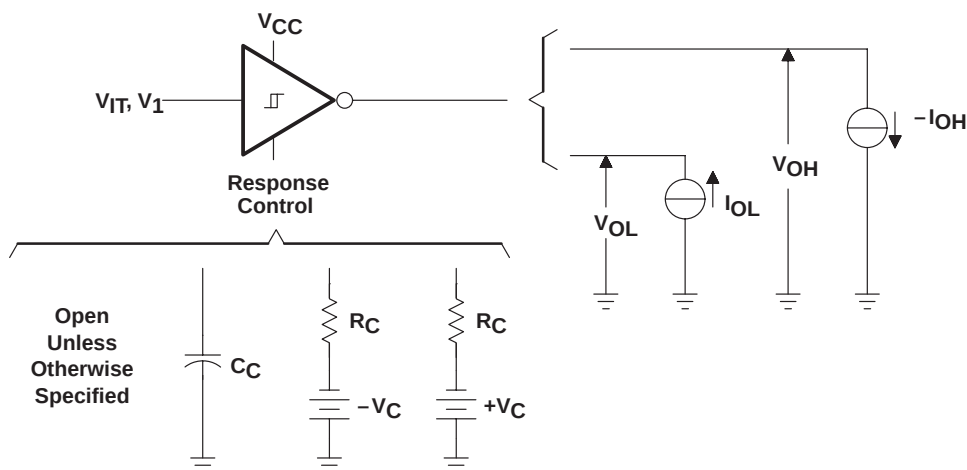
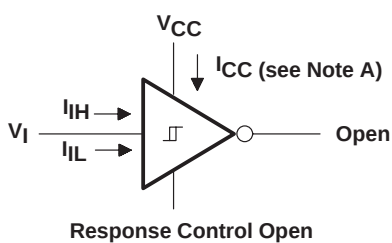


Figure 1. V_{IT+} , V_{IT-} , V_{OH} , V_{OL}



NOTE A: I_{CC} is tested for all four receivers simultaneously.

Figure 2. I_{iH} , I_{iL} , I_{CC}

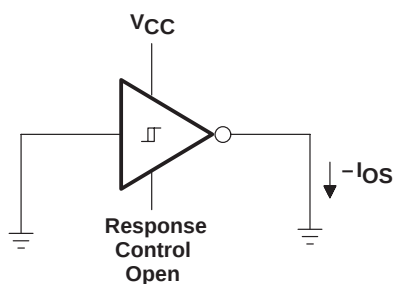


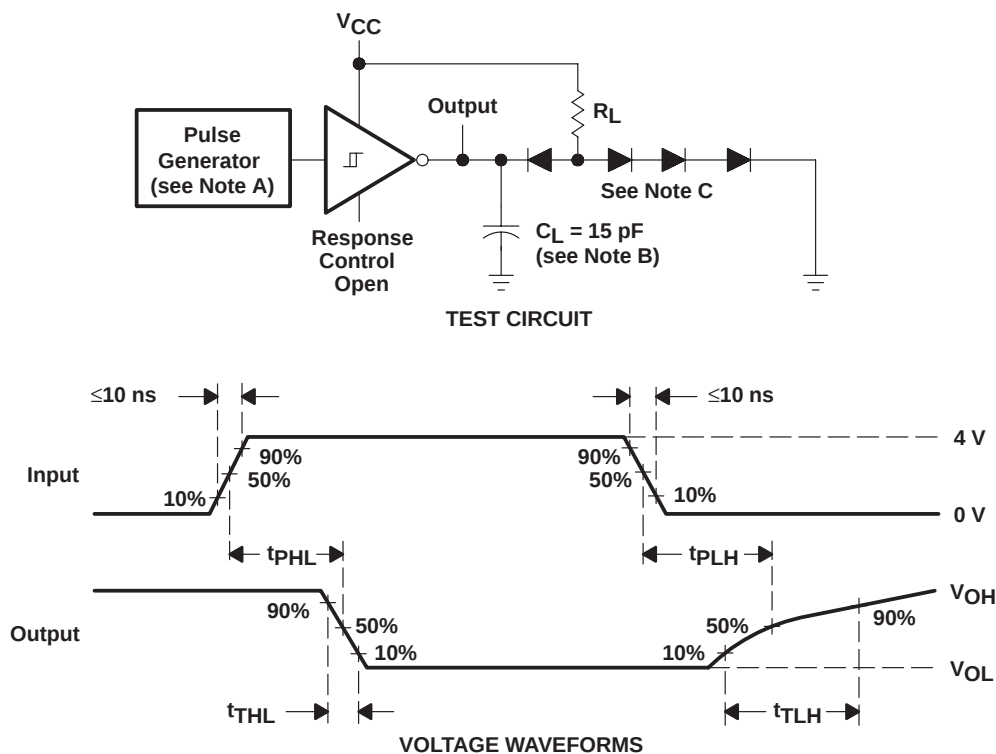
Figure 3. I_{OS}

† Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

MC1489, MC1489A, SN55189, SN55189A, SN75189, SN75189A QUADRUPLE LINE RECEIVERS

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PARAMETER MEASUREMENT INFORMATION



- NOTES: A. The pulse generator has the following characteristics: $Z_O = 50 \Omega$, $t_W = 500 \text{ ns}$.
B. C_L includes probe and jig capacitances.
C. All diodes are 1N3064 or equivalent.

Figure 4. Test Circuit and Voltage Waveforms

MC1489, MC1489A, SN55189, SN55189A, SN75189, SN75189A QUADRUPLE LINE RECEIVERS

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TYPICAL CHARACTERISTICS

SN65189, SN75189
OUTPUT VOLTAGE
vs
INPUT VOLTAGE

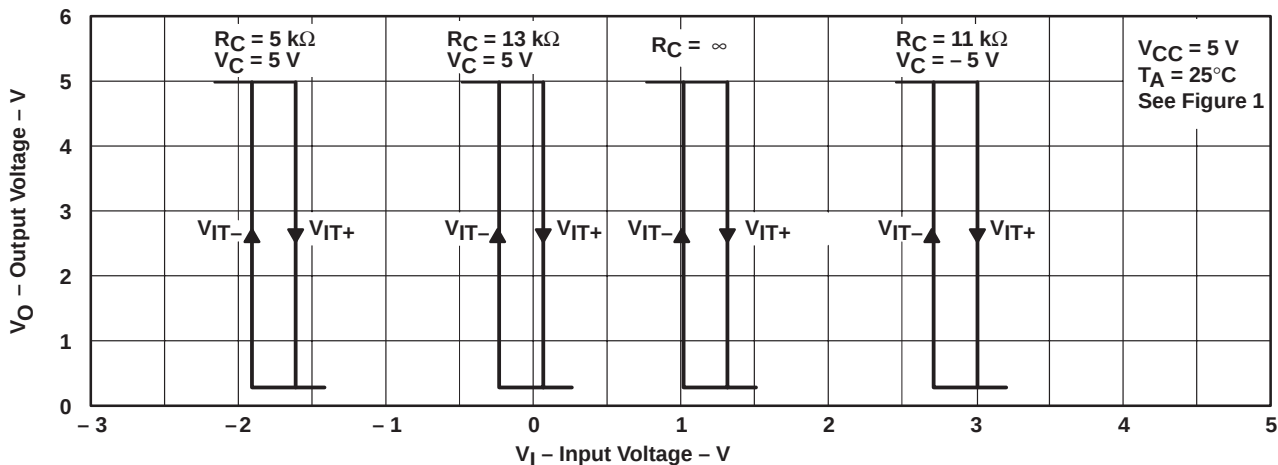


Figure 5

SN65189A, SN75189A
OUTPUT VOLTAGE
vs
INPUT VOLTAGE

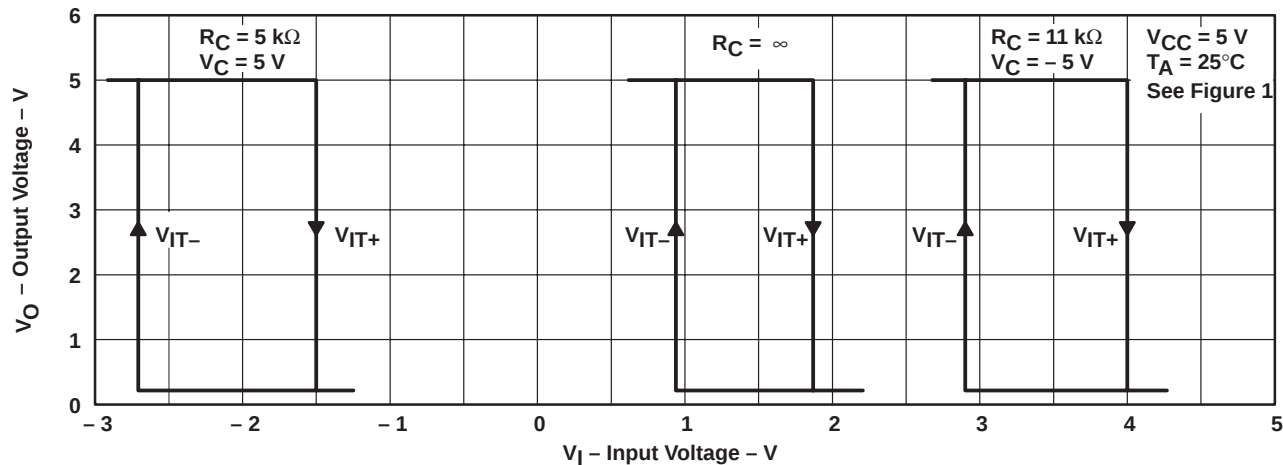


Figure 6

MC1489, MC1489A, SN55189, SN55189A, SN75189, SN75189A
QUADRUPLE LINE RECEIVERS

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TYPICAL CHARACTERISTICS†

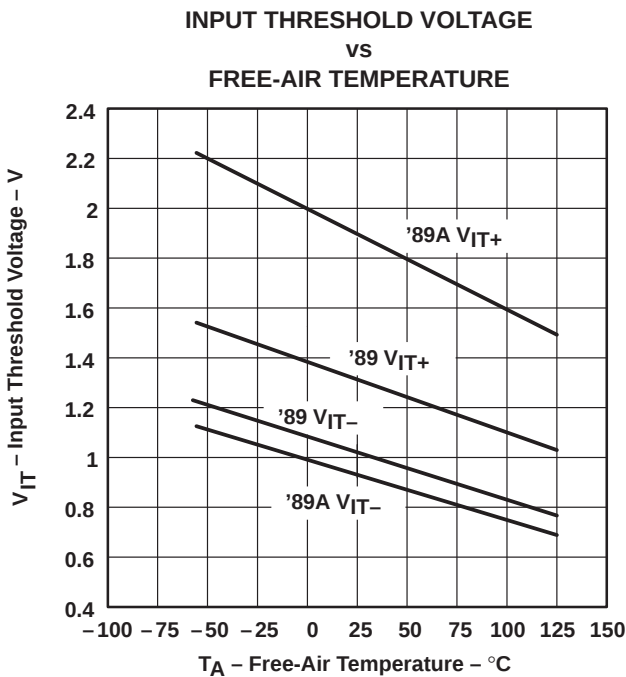


Figure 7

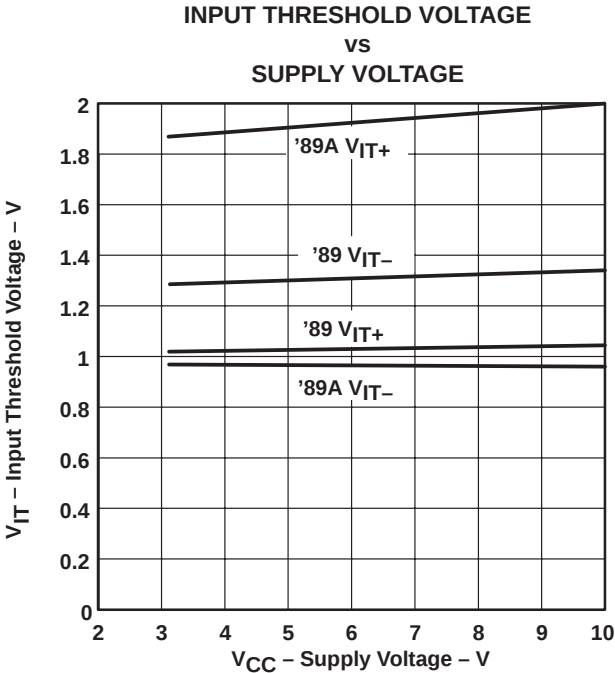
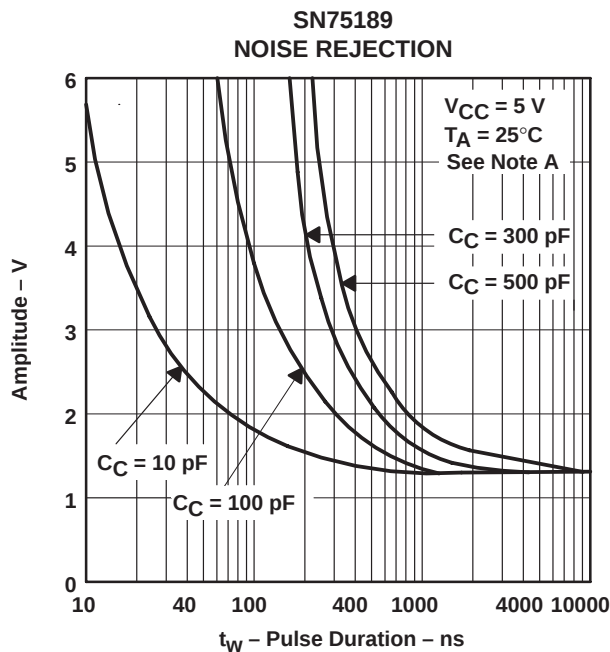
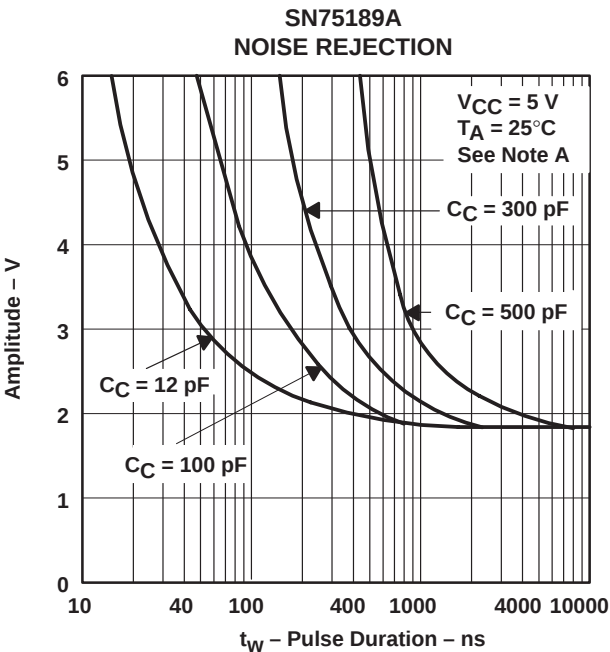


Figure 8



NOTE A: Maximum amplitude of a positive-going pulse that, starting from 0 V, will not cause a change in the output level.

Figure 9



NOTE A: Maximum amplitude of a positive-going pulse that, starting from 0 V, will not cause a change in the output level.

Figure 10

† Data for free-air temperatures below 0°C and above 70°C are applicable to SN55189 and SN55189A circuits only.

TYPICAL CHARACTERISTICS

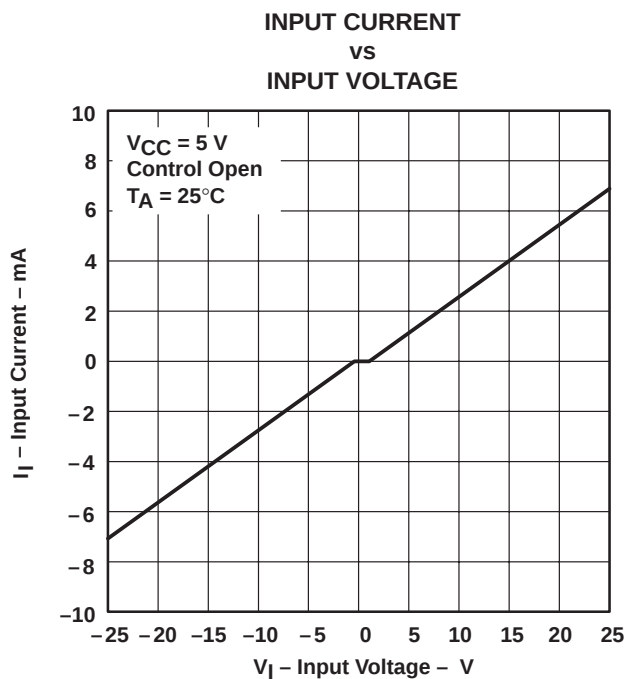


Figure 11

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-86888022A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Non-Green	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 86888022A SNJ55 189AFK	Samples
5962-8688802CA	ACTIVE	CDIP	J	14	1	Non-RoHS & Non-Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8688802CA SNJ55189AJ	Samples
5962-8688802DA	ACTIVE	CFP	W	14	1	Non-RoHS & Non-Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8688802DA SNJ55189AW	Samples
MC1489AN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	MC1489AN	Samples
MC1489N	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	MC1489N	Samples
MC1489NE4	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	MC1489N	Samples
SN55189AJ	ACTIVE	CDIP	J	14	1	Non-RoHS & Non-Green	SNPB	N / A for Pkg Type	-55 to 125	SN55189AJ	Samples
SN75189AD	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75189A	Samples
SN75189ADR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75189A	Samples
SN75189ADRG4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75189A	Samples
SN75189AN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN75189AN	Samples
SN75189ANSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75189A	Samples
SN75189ANSRG4	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75189A	Samples
SN75189APWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		A189A	Samples
SN75189D	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75189	Samples
SN75189DR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75189	Samples
SN75189N	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN75189N	Samples
SN75189NSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75189	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SNJ55189AFK	ACTIVE	LCCC	FK	20	1	Non-RoHS & Non-Green	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 86888022A SNJ55 189AFK	Samples
SNJ55189AJ	ACTIVE	CDIP	J	14	1	Non-RoHS & Non-Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8688802CA SNJ55189AJ	Samples
SNJ55189AW	ACTIVE	CFP	W	14	1	Non-RoHS & Non-Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8688802DA SNJ55189AW	Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN55189A, SN75189A :

- Catalog: [SN75189A](#)
- Military: [SN55189A](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75189ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN75189ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN75189ANSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN75189APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN75189DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN75189NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75189ADR	SOIC	D	14	2500	333.2	345.9	28.6
SN75189ADR	SOIC	D	14	2500	853.0	449.0	35.0
SN75189ANSR	SO	NS	14	2000	853.0	449.0	35.0
SN75189APWR	TSSOP	PW	14	2000	853.0	449.0	35.0
SN75189DR	SOIC	D	14	2500	853.0	449.0	35.0
SN75189NSR	SO	NS	14	2000	853.0	449.0	35.0

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



J 14

GENERIC PACKAGE VIEW

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

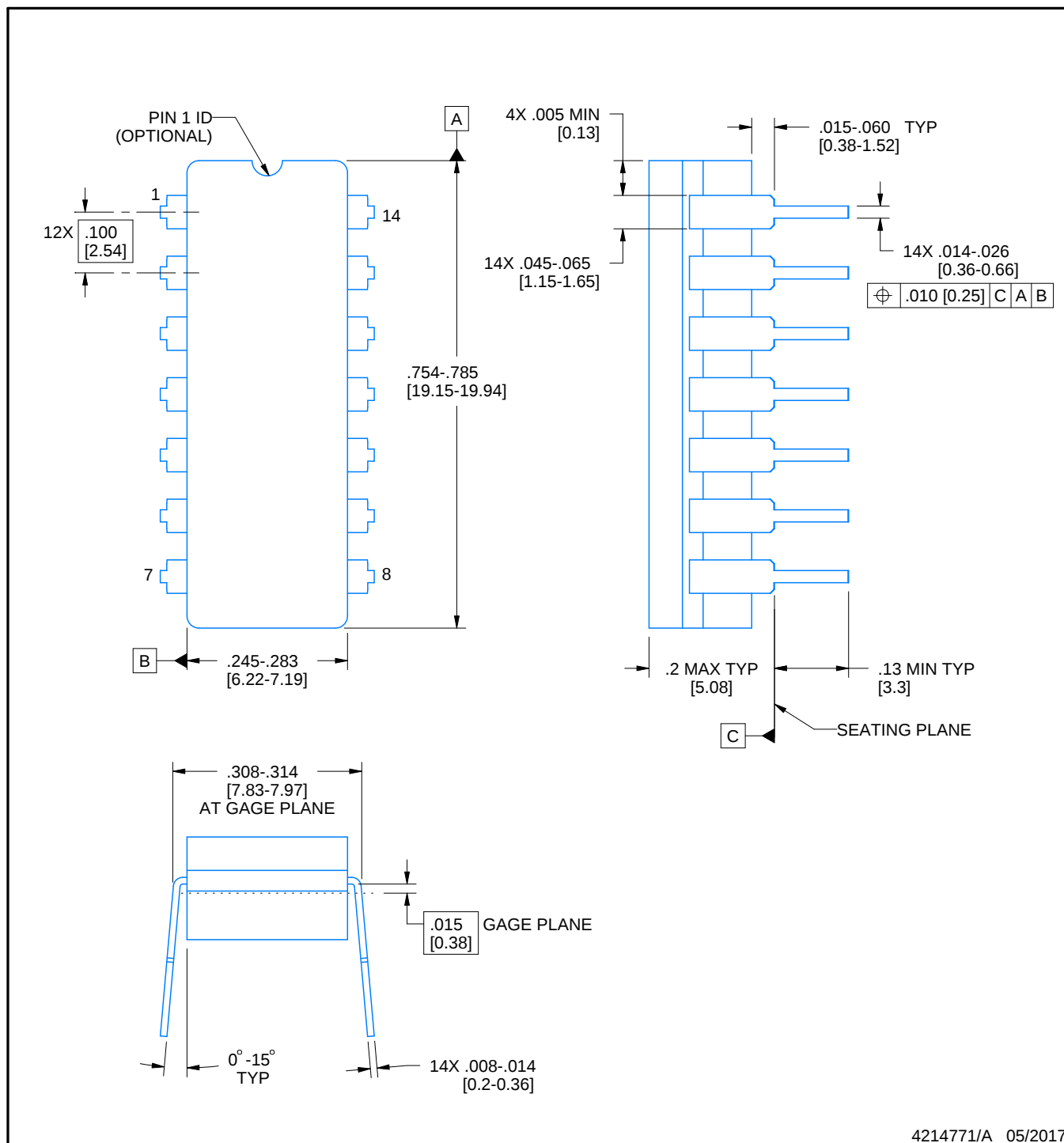


J0014A

PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

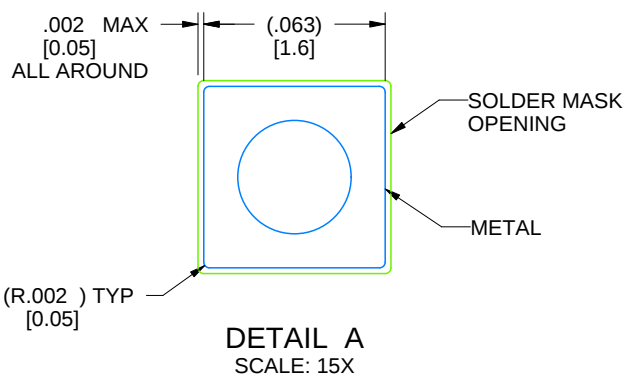
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



4214771/A 05/2017

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



14/18 Pin Only
20 Pin vendor option

4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

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