



## Description

The STP75NF75 uses advanced trench technology and design to provide excellent  $R_{DS(ON)}$  with low gate charge. It can be used in a wide variety of applications.

## General Features

$V_{DS} = 80V, I_D = 96A$

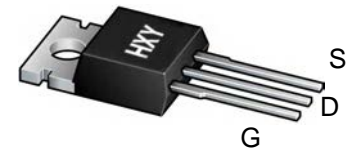
$R_{DS(ON)} < 7.2m\Omega @ V_{GS} = 10V$

## Application

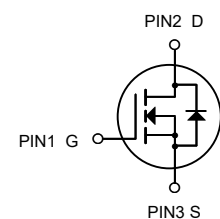
High efficiency switch mode power supplies

Power factor correction

Electronic lamp ballast



TO-220C  
(TO-220FPAB-3)



N-Channel MOSFET

## Package Marking and Ordering Information

Product ID	Pack	Brand	Units Tube
STP75NF75	TO-220C(TO-220FPAB-3)	HXY MOSFET	50

## Absolute Maximum Ratings@ $T_J = 25^\circ C$ (unless otherwise specified)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	80	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous	$I_D$	96	A
Drain Current-Continuous( $T_C = 100^\circ C$ )	$I_D(100^\circ C)$	67	A
Pulsed Drain Current	$I_{DM}$	368	A
Maximum Power Dissipation	$P_D$	146	W
Derating factor	-	1.06	W/ $^\circ C$
Single pulse avalanche energy (Note 5)	$E_{AS}$	625	mJ
Thermal Resistance, Junction-to-Case (Note 2)	$R_{\theta JC}$	1.02	$^\circ C/W$
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 150	$^\circ C$



**Electrical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>DS</sub> = 0, I <sub>D</sub> = 250 μA	80			V
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	2.0		4.0	
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 80 V , V <sub>GS</sub> = 0 V			1	μA
		V <sub>DS</sub> = 80 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C			50	
		V <sub>DS</sub> = 80 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 150 °C			250	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> ≥ 10 V, V <sub>GS</sub> = 10 V	96			A
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 40 A		6.2	7.2	mΩ
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 40 A		13		S
Dynamic <sup>b</sup>						
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 25 V, f = 1 MHz		6395		pF
Output Capacitance	C <sub>oss</sub>			386		
Reverse Transfer Capacitance	C <sub>rss</sub>			255		
Total Gate Charge <sup>c</sup>	Q <sub>g</sub>	V <sub>DS</sub> = 50 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 40 A		116		nC
Gate-Source Charge <sup>c</sup>	Q <sub>gs</sub>			27		
Gate-Drain Charge <sup>c</sup>	Q <sub>gd</sub>			39		
Turn-On Delay Time <sup>c</sup>	t <sub>d(on)</sub>	V <sub>DD</sub> = 30 V, R <sub>L</sub> = 2.5 Ω I <sub>D</sub> = 40 A, V <sub>GEN</sub> = 10 V, R <sub>g</sub> = 1 Ω		22		ns
Rise Time <sup>c</sup>	t <sub>r</sub>			50		
Turn-Off Delay Time <sup>c</sup>	t <sub>d(off)</sub>			65		
Fall Time <sup>c</sup>	t <sub>f</sub>			22		
Source-Drain Diode Ratings and Characteristics T <sub>C</sub> = 25 °C <sup>b</sup>						
Continuous Current	I <sub>S</sub>				96	A
Pulsed Current	I <sub>SM</sub>				368	
Forward Voltage <sup>a</sup>	V <sub>SD</sub>	I <sub>F</sub> = 40 A, V <sub>GS</sub> = 0 V		0.89		V
Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 10 A, dI/dt = 100 A/μs		41		NS
Peak Reverse Recovery Current	I <sub>RM(REC)</sub>			3.0		A
Reverse Recovery Charge	Q <sub>rr</sub>			86		nC

Notes:

a. Pulse test; pulse width  $\leq 300 \mu\text{s}$ , duty cycle  $\leq 2\%$ .

b. Guaranteed by design, not subject to production testing.

c. Independent of operating temperature.



## Typical Characteristics

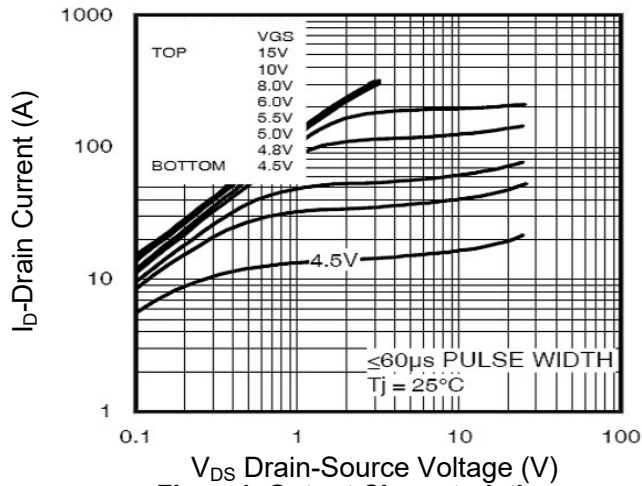


Figure1. Output Characteristics

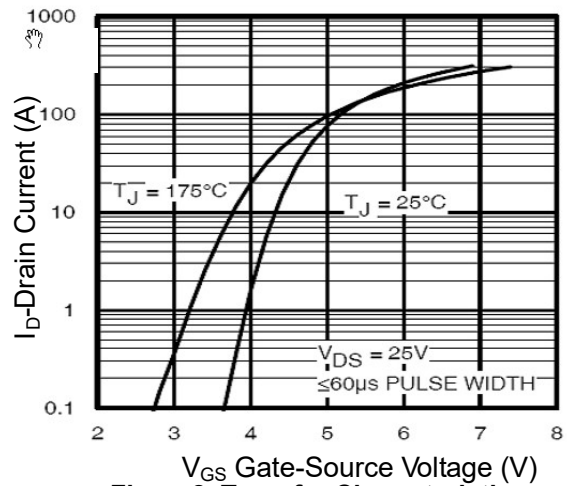


Figure2. Transfer Characteristics

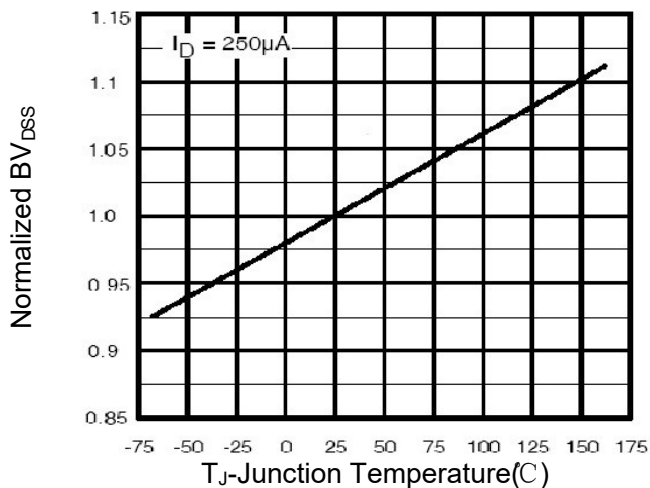


Figure3.BVDSS vs Junction Temperature

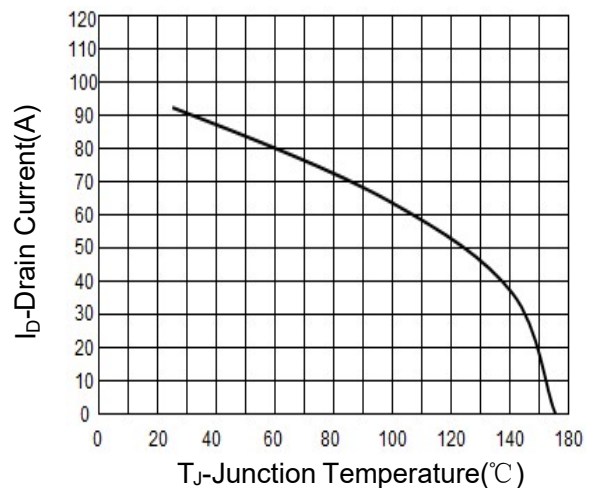


Figure4.ID vs Junction Temperature

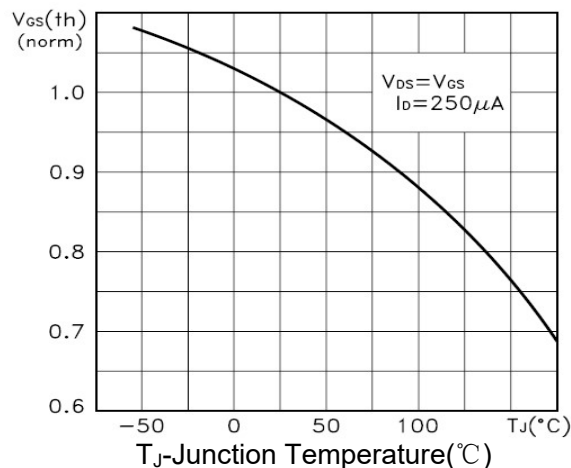


Figure5.VGS(th) vs Junction Temperature

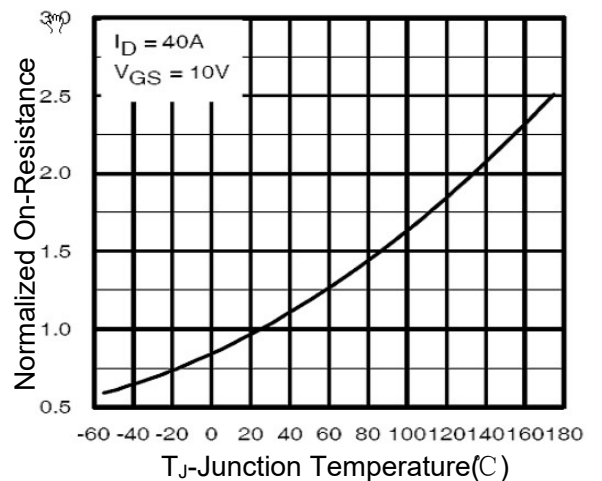


Figure6. Rdson Vs Junction Temperature

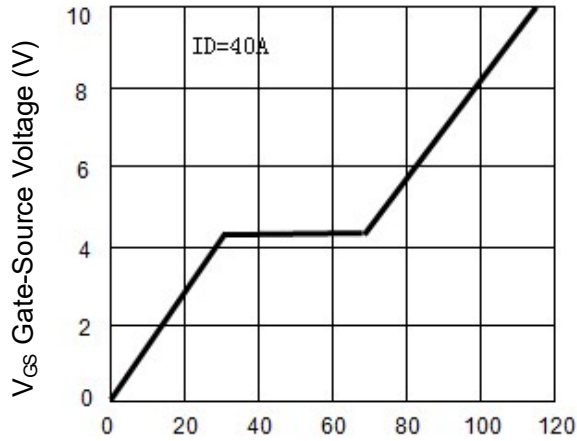


Figure7. Gate Charge

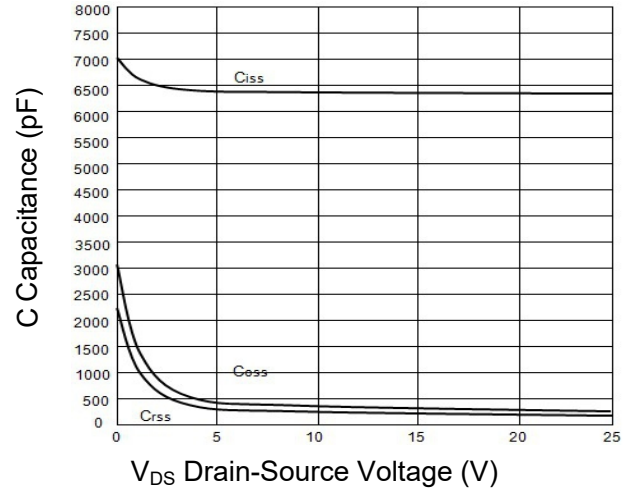


Figure8. Capacitance vs Vds

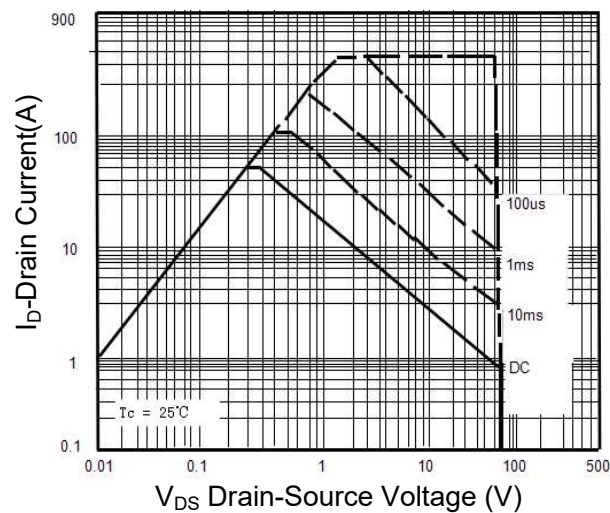


Figure9. Safe Operation Area

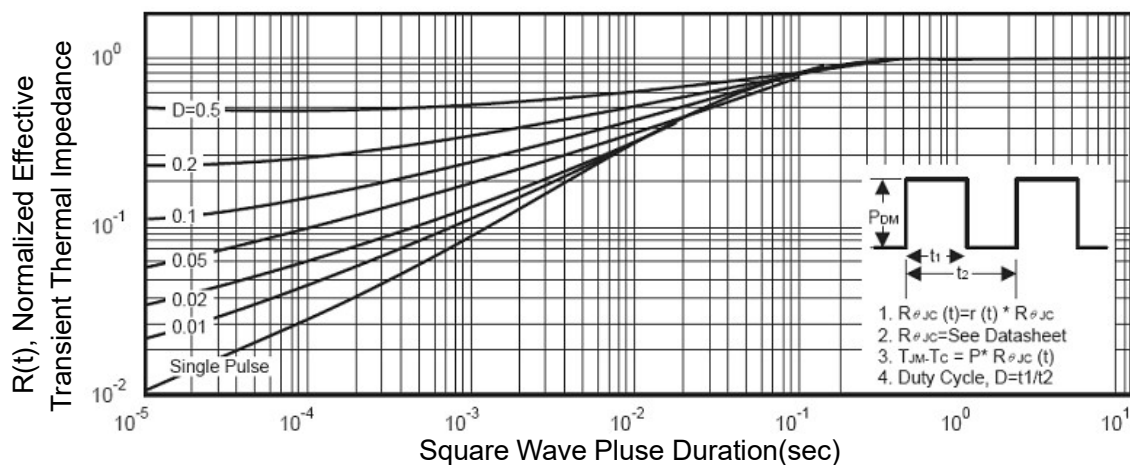
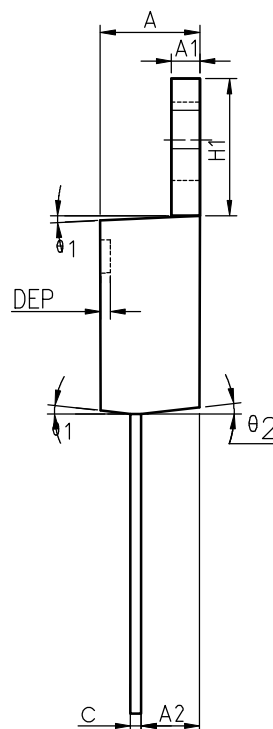
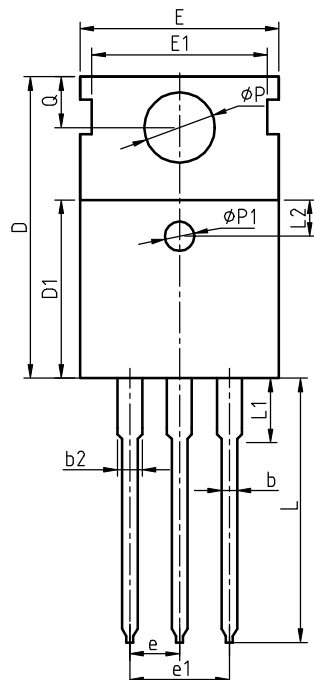


Figure11. Normalized Maximum Transient Thermal Impedance

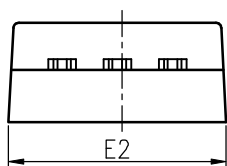


Package Information  
TO-220C(TO-220FPAB-3)



COMMON DIMENSIONS

SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
A	4.40	4.57	4.70	0.173	0.180	0.185
A1	1.27	1.30	1.33	0.050	0.051	0.052
A2	2.35	2.40	2.50	0.093	0.094	0.098
b	0.77	0.80	0.90	0.030	0.031	0.035
b2	1.17	1.27	1.36	0.046	0.050	0.054
c	0.48	0.50	0.56	0.019	0.020	0.022
D	15.40	15.60	15.80	0.606	0.614	0.622
D1	9.00	9.10	9.20	0.354	0.358	0.362
DEP	0.05	0.10	0.20	0.002	0.004	0.008
E	9.80	10.00	10.20	0.386	0.394	0.402
E1	-	8.70	-	-	0.343	-
E2	9.80	10.00	10.20	0.386	0.394	0.402
e		2.54	BSC		0.100	BSC
e1		5.08	BSC		0.200	BSC
H1	6.40	6.50	6.60	0.252	0.256	0.260
L	12.75	13.50	13.65	0.502	0.531	0.537
L1	-	3.10	3.30	-	0.122	0.130
L2		2.50	REF		0.098	REF
P	3.50	3.60	3.63	0.138	0.142	0.143
P1	3.50	3.60	3.63	0.138	0.142	0.143
Q	2.73	2.80	2.87	0.107	0.110	0.113
θ 1	5°	7°	9°	5°	7°	9°
θ 2	1°	3°	5°	1°	3°	5°
θ 3	1°	3°	5°	1°	3°	5°





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