



STB12NM50N, STD12NM50N, STI12NM50N STF12NM50N, STP12NM50N

N-channel 500 V, 0.29 Ω , 11 A MDmesh™ II Power MOSFET
TO-220 - DPAK - D²PAK - I²PAK - TO-220FP

Features

Type	V _{DSS} (@T _{jmax})	R _{DS(on)} max	I _D
STB12NM50N	550 V	0.38 Ω	11 A
STD12NM50N	550 V	0.38 Ω	11 A
STI12NM50N	550 V	0.38 Ω	11 A
STF12NM50N	550 V	0.38 Ω	11 A ⁽¹⁾
STP12NM50N	550 V	0.38 Ω	11 A

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

Application

- Switching applications

Description

This series of devices is realized with the second generation of MDmesh™ technology. This revolutionary Power MOSFET associates a new vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters.

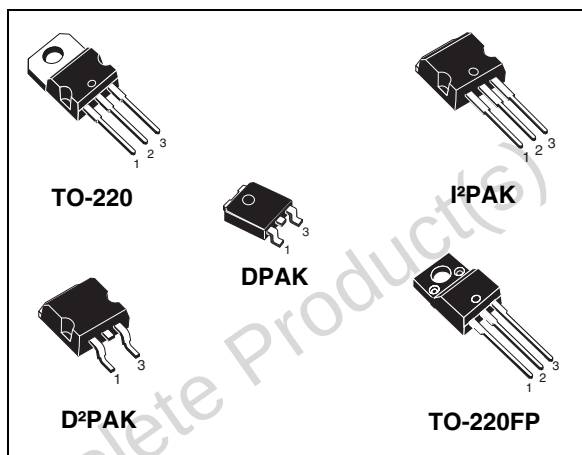


Figure 1. Internal schematic diagram

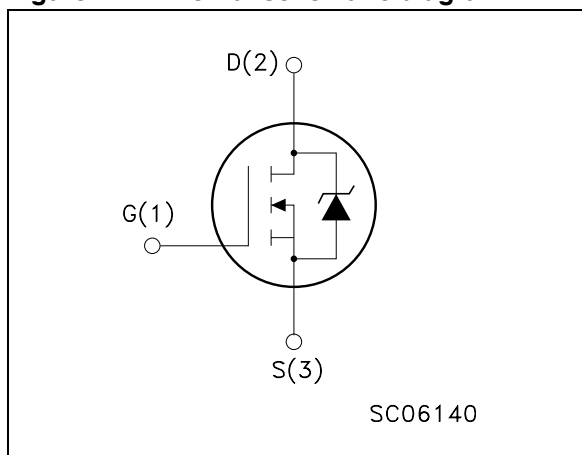


Table 1. Device summary

Order codes	Marking	Package	Packaging
STB12NM50N	B12NM50N	D ² PAK	Tape and reel
STD12NM50N	D12NM50N	DPAK	Tape and reel
STI12NM50N	I12NM50N	I ² PAK	Tube
STF12NM50N	F12NM50N	TO-220FP	Tube
STP12NM50N	P12NM50N	TO-220	Tube

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		TO-220 / I ² PAK D ² PAK / DPAK	TO-220FP	
V _{DS}	Drain-source voltage (V _{GS} = 0)	500		V
V _{GS}	Gate-source voltage	± 25		V
I _D	Drain current (continuous) at T _C = 25 °C	11	11 ⁽¹⁾	A
I _D	Drain current (continuous) at T _C =100 °C	6.7	6.7 ⁽¹⁾	A
I _{DM} ⁽²⁾	Drain current (pulsed)	44	44 ⁽¹⁾	A
P _{TOT}	Total dissipation at T _C = 25 °C	100	25	W
dv/dt ⁽³⁾	Peak diode recovery voltage slope	15		V/ns
V _{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t=1 s; T _C =25 °C)	--	2500	V
T _{stg}	Storage temperature	-55 to 150		°C
T _J	Max. operating junction temperature	150		°C

1. Limited only by maximum temperature allowed
2. Pulse width limited by safe operating area
3. I_{SD} ≤ 11A, di/dt ≤ 400A/μs, V_{DD} = 80%V_{(BR)DSS}

Table 3. Thermal data

Symbol	Parameter	Value					Unit
		TO-220	I ² PAK	DPAK	D ² PAK	TO-220FP	
R _{thj-case}	Thermal resistance junction-case max	1.25				5	°C/W
R _{thj-amb}	Thermal resistance junction-amb max	62.5	--	--	--	62.5	°C/W
R _{thj-pcb}	Thermal resistance junction-pcb max	--	--	50	30	--	°C/W
T _l	Maximum lead temperature for soldering purposes	300					°C

Table 4. Avalanche characteristics

Symbol	Parameter	Value	Unit
I _{AS}	Avalanche current, repetitive or not-repetitive (pulse width limited by T _J Max)	5	A
E _{AS}	Single pulse avalanche energy (starting T _J =25°C, I _d =I _{as} , V _{dd} =50V)	350	mJ

2 Electrical characteristics

($T_{CASE}=25\text{ }^{\circ}\text{C}$ unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$, $V_{GS} = 0$	500			V
$dv/dt^{(1)}$	Peak diode recovery voltage slope	$V_{DD}=400\text{ V}$, $I_D=11\text{ A}$, $V_{GS}=10\text{ V}$	44			V/ns
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{max rating}$, $V_{DS} = \text{max rating}@125\text{ }^{\circ}\text{C}$			1 100	μA μA
I_{GSS}	Gate body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20\text{ V}$			100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}$, $I_D = 5.5\text{ A}$		0.29	0.38	Ω

1. Characteristic value at turn off inductive load

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS}=15\text{ V}$, $I_D = 5.5\text{ A}$		8		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS}=50\text{ V}$, $f=1\text{ MHz}$, $V_{GS}=0$		940 100 10		pF pF pF
$C_{oss\text{ eq}}^{(2)}$	Equivalent output capacitance	$V_{GS}=0$, $V_{DS}=0\text{ to }400\text{ V}$		130		pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	$V_{DD}=400\text{ V}$, $I_D = 11\text{ A}$ $V_{GS}=10\text{ V}$ (see Figure 17)		30 6 15		nC nC nC
R_g	Gate input resistance	$f=1\text{ MHz}$ Gate DC Bias=0 test signal level=20 mV open drain		4.5		Ω

1. Pulsed: pulse duration=300 μs , duty cycle 1.5%

2. $C_{oss\text{ eq}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7. Switching times

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD}=250\text{ V}$, $I_D=5.5\text{ A}$, $R_G=4.7\ \Omega$, $V_{GS}=10\text{ V}$ (see Figure 16)		15		ns
t_r	Rise time			15		ns
$t_{d(off)}$	Turn-off delay time			60		ns
t_f	Fall time			14		ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD}	Source-drain current				11	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				44	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD}=11\text{ A}$, $V_{GS}=0$			1.3	V
t_{rr}	Reverse recovery time	$I_{SD}=11\text{ A}$, $V_{DD}=100\text{ V}$ $di/dt = 100\text{ A}/\mu\text{s}$, (see Figure 18)		340		ns
Q_{rr}	Reverse recovery charge			3.5		μC
I_{RRM}	Reverse recovery current			20		A
t_{rr}	Reverse recovery time	$I_{SD}=11\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD}=100\text{ V}$, $T_J=150\text{ }^\circ\text{C}$ (see Figure 18)		420		ns
Q_{rr}	Reverse recovery charge			4		μC
I_{RRM}	Reverse recovery current			20		A

1. Pulse width limited by safe operating area

2. Pulsed: pulse duration=300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for TO-220/
DPAK/ D²PAK / I²PAK

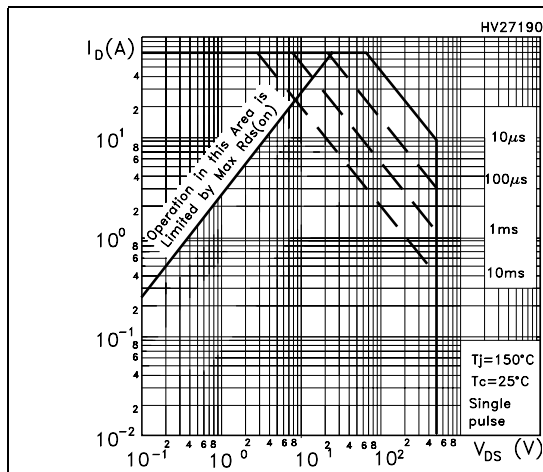


Figure 3. Thermal impedance for TO-220/
DPAK/ D²PAK / I²PAK

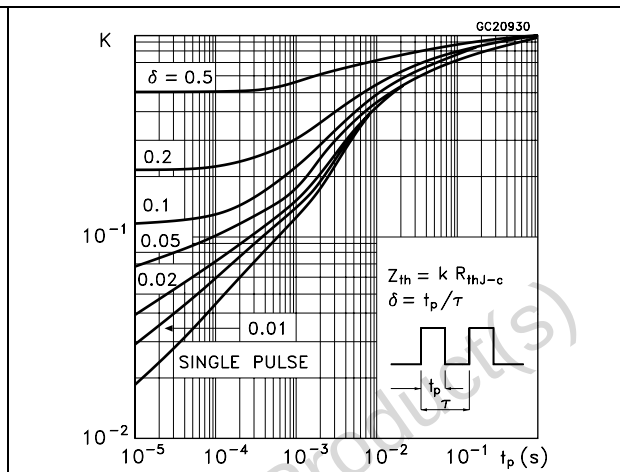


Figure 4. Safe operating area for TO-220FP

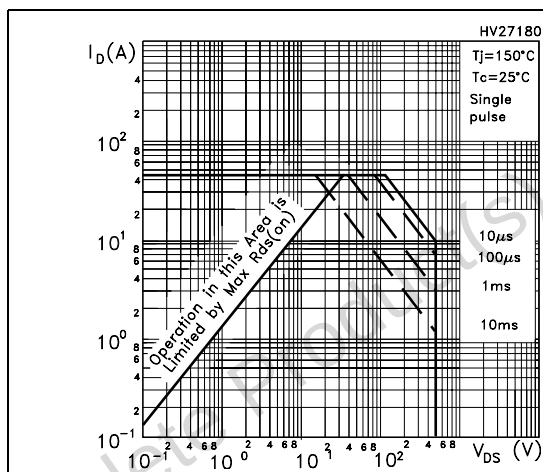


Figure 5. Thermal impedance for TO-220FP

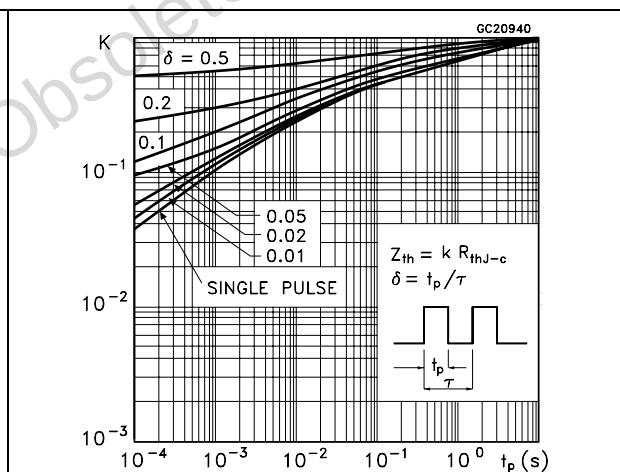


Figure 6. Output characteristics

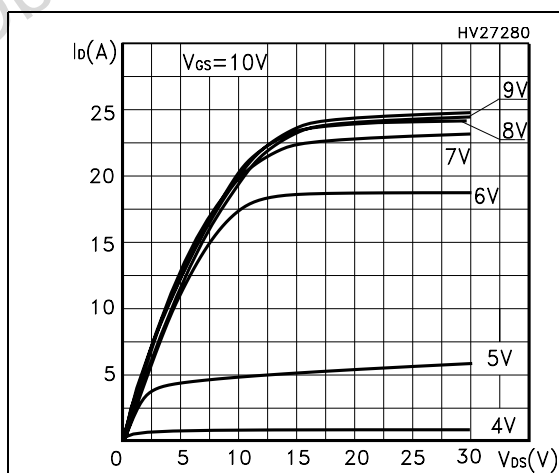


Figure 7. Transfer characteristics

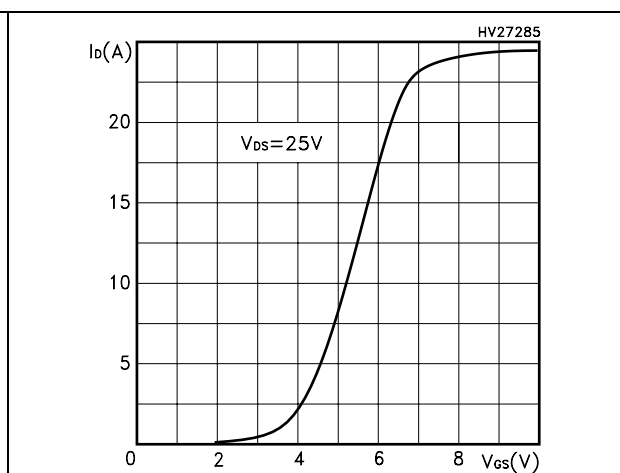


Figure 8. Transconductance

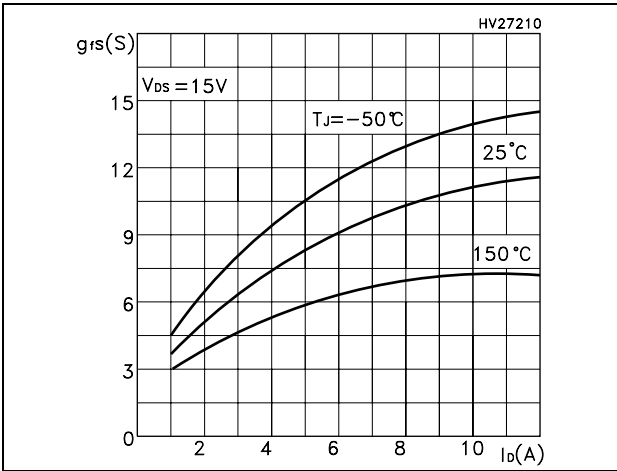


Figure 9. Static drain-source on resistance

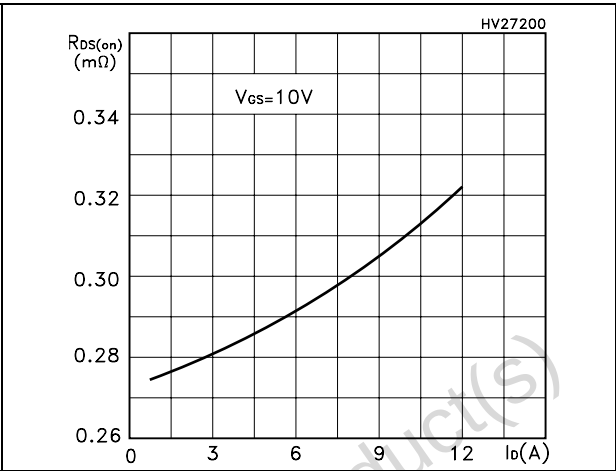


Figure 10. Gate charge vs gate-source voltage

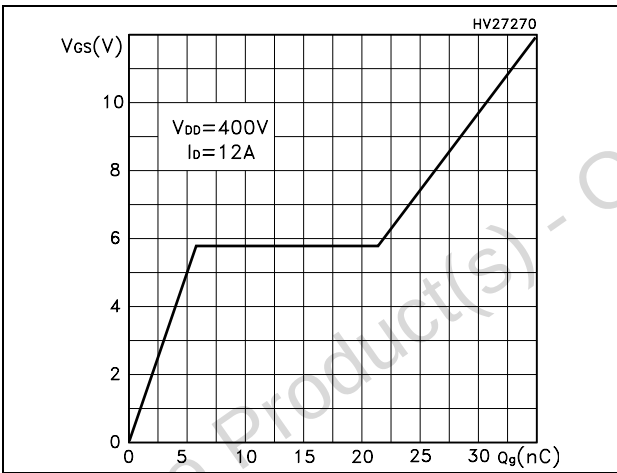


Figure 11. Capacitance variations

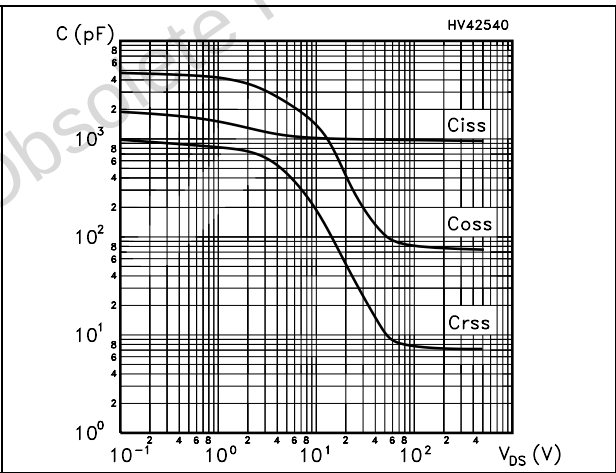


Figure 12. Normalized gate threshold voltage vs temperature

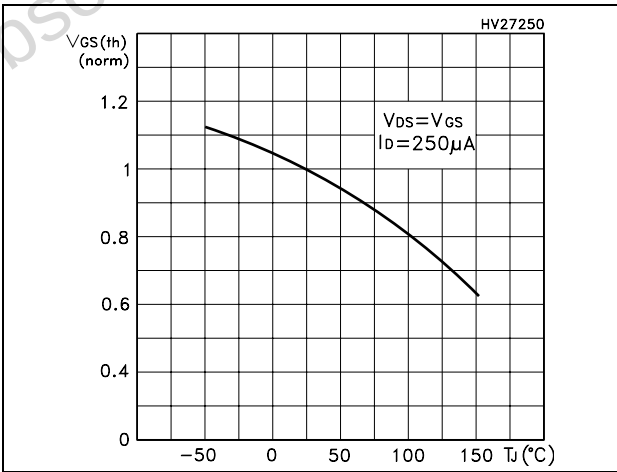


Figure 13. Normalized on resistance vs temperature

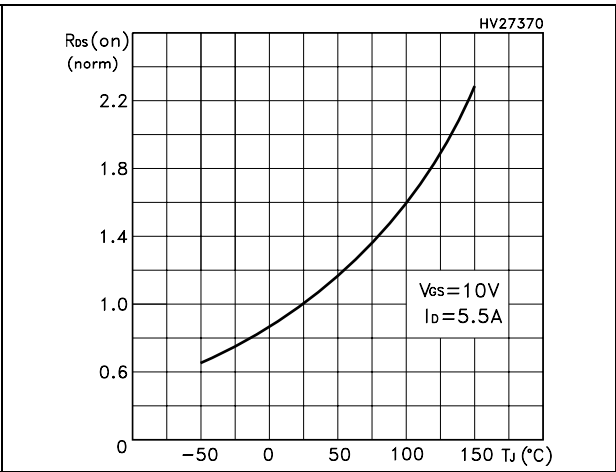


Figure 14. Source-drain diode forward characteristics

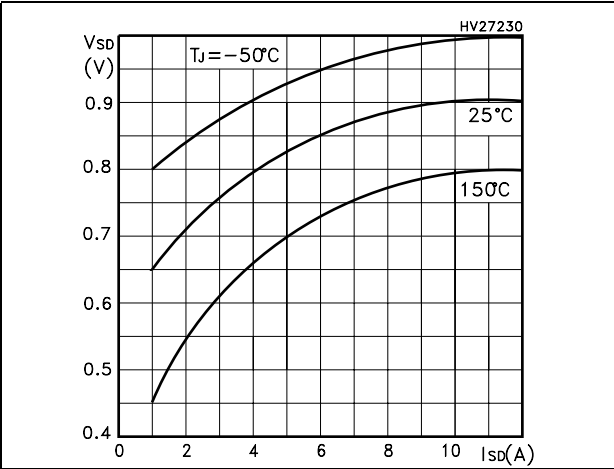
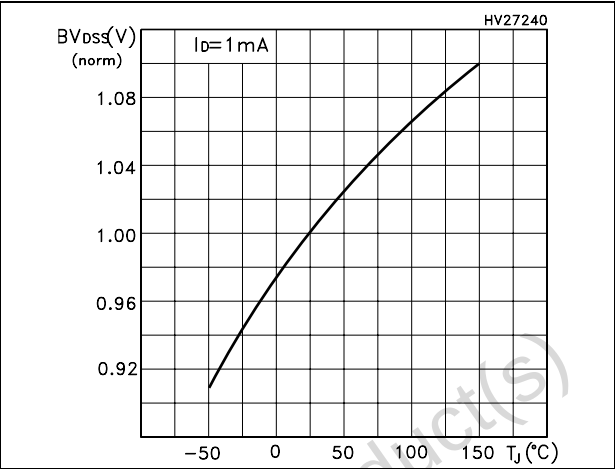


Figure 15. Normalized $B_{V_{DSS}}$ vs temperature



3 Test circuit

Figure 16. Switching times test circuit for resistive load

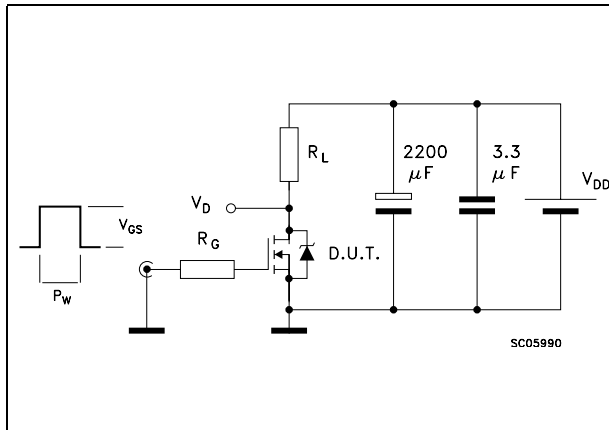


Figure 17. Gate charge test circuit

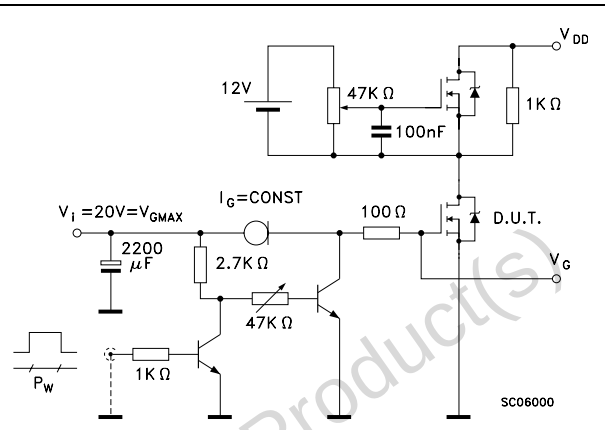


Figure 18. Test circuit for inductive load switching and diode recovery times

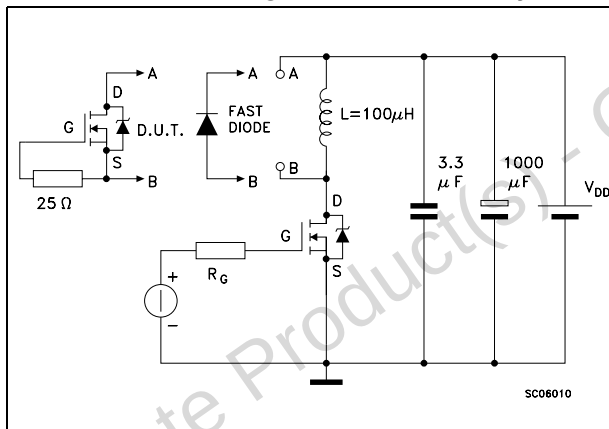


Figure 19. Unclamped Inductive load test circuit

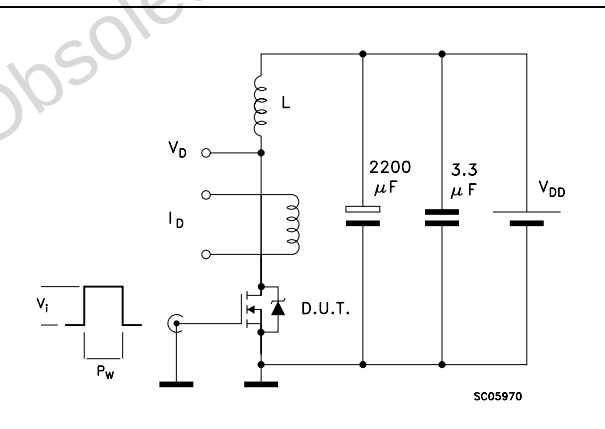


Figure 20. Unclamped inductive waveform

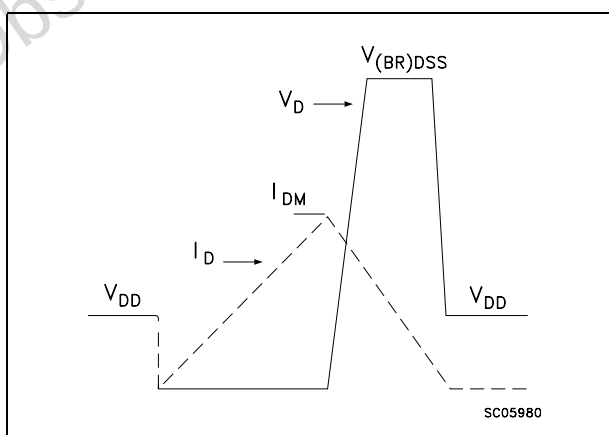
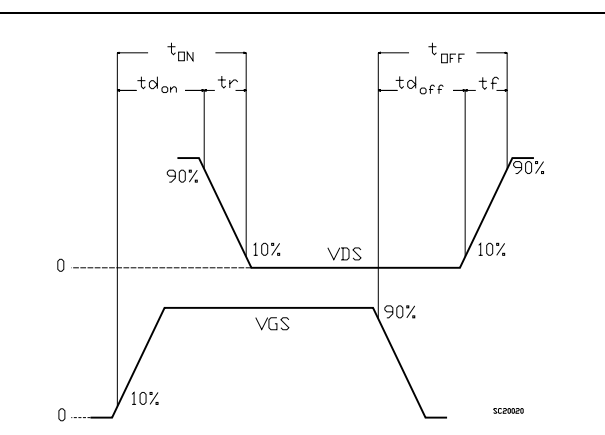


Figure 21. Switching time waveform



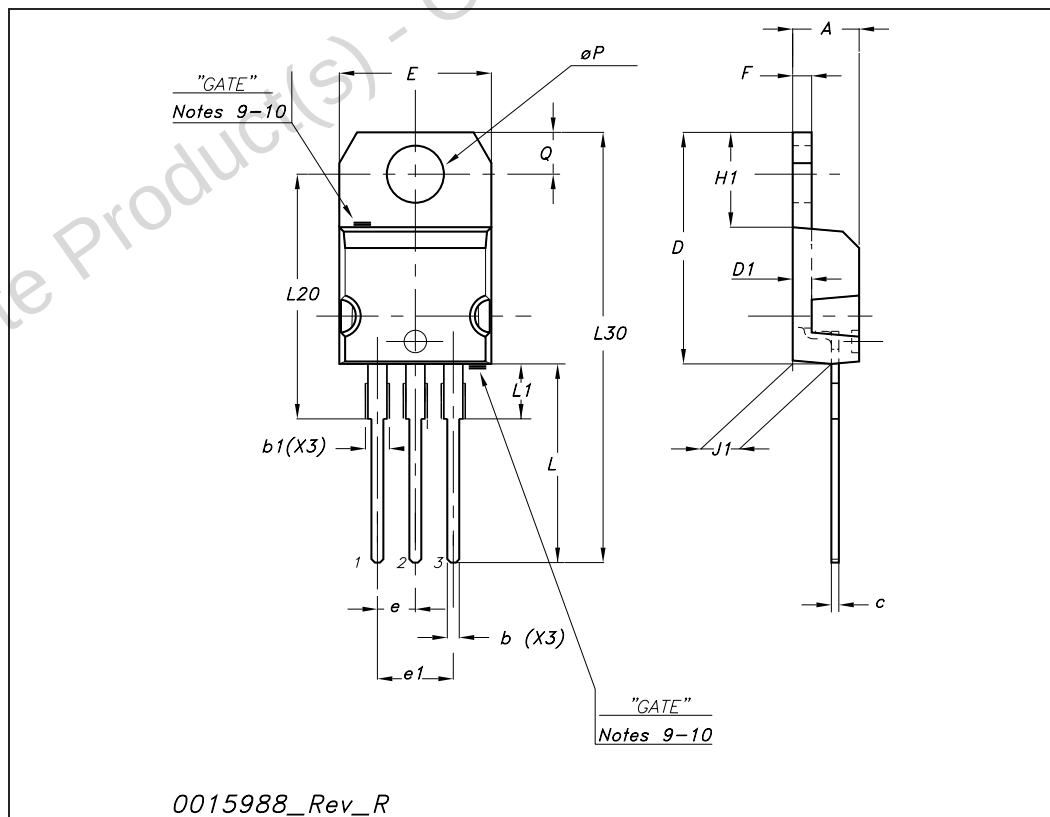
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

Obsolete Product(s) - Obsolete Product(s)

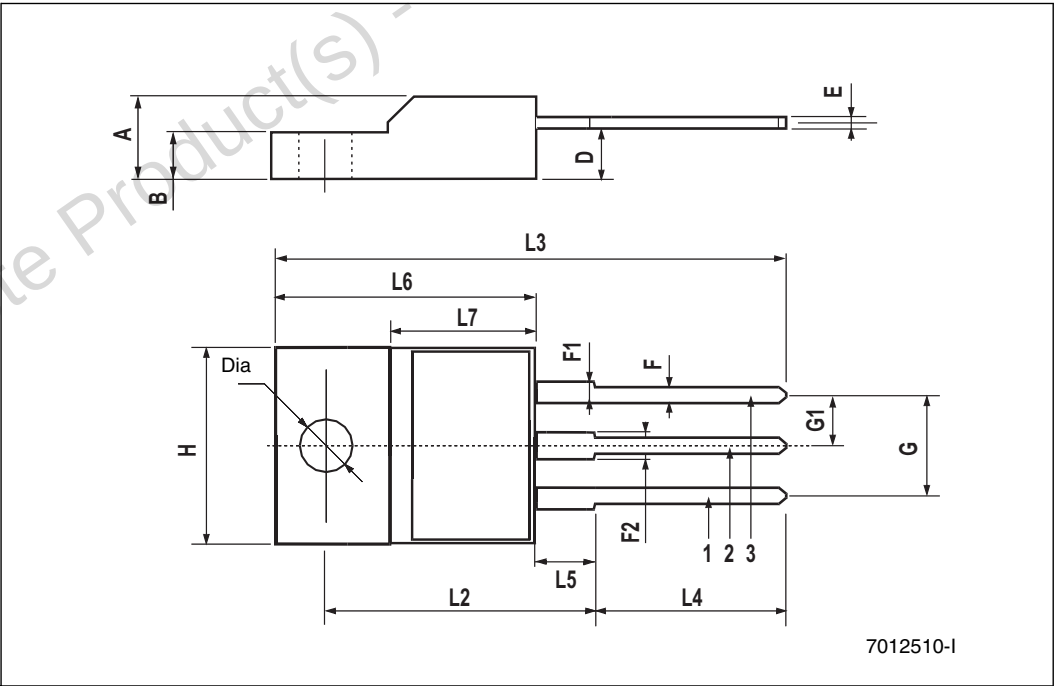
TO-220 mechanical data

Dim	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.14		1.70	0.044		0.066
c	0.48		0.70	0.019		0.027
D	15.25		15.75	0.6		0.62
D1		1.27			0.050	
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.051
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
ØP	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



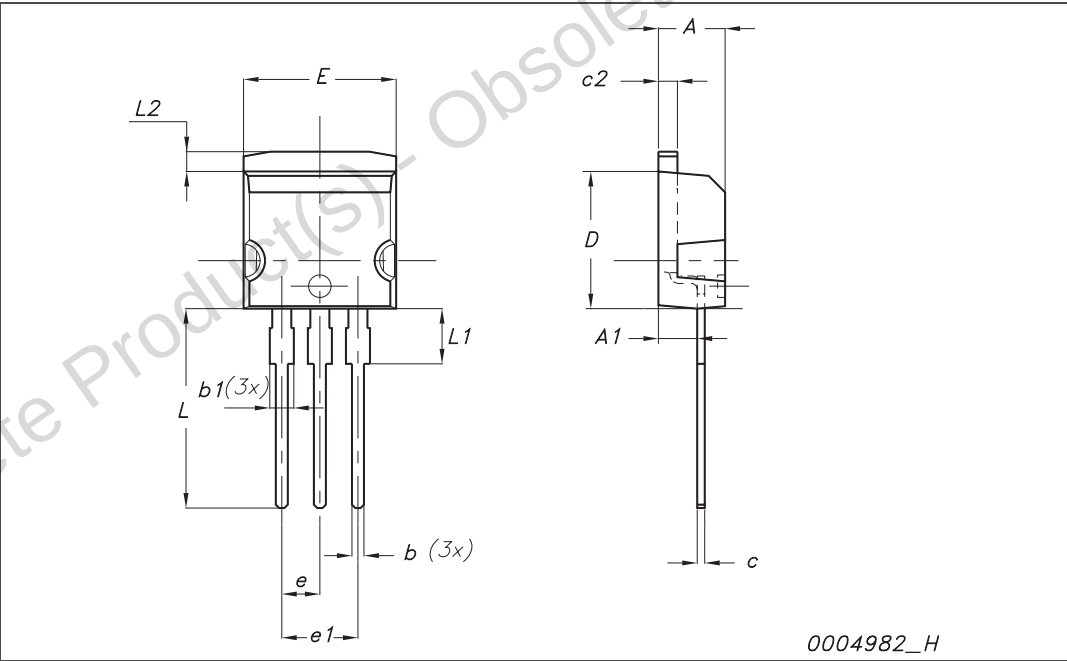
TO-220FP mechanical data

Dim.	mm.			inch		
	Min.	Typ	Max.	Min.	Typ.	Max.
A	4.40		4.60	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.45		0.70	0.017		0.027
F	0.75		1.00	0.030		0.039
F1	1.15		1.50	0.045		0.067
F2	1.15		1.50	0.045		0.067
G	4.95		5.20	0.195		0.204
G1	2.40		2.70	0.094		0.106
H	10		10.40	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.80		10.60	0.385		0.417
L5	2.9		3.6	0.114		0.141
L6	15.90		16.40	0.626		0.645
L7	9		9.30	0.354		0.366
Dia	3		3.2	0.118		0.126



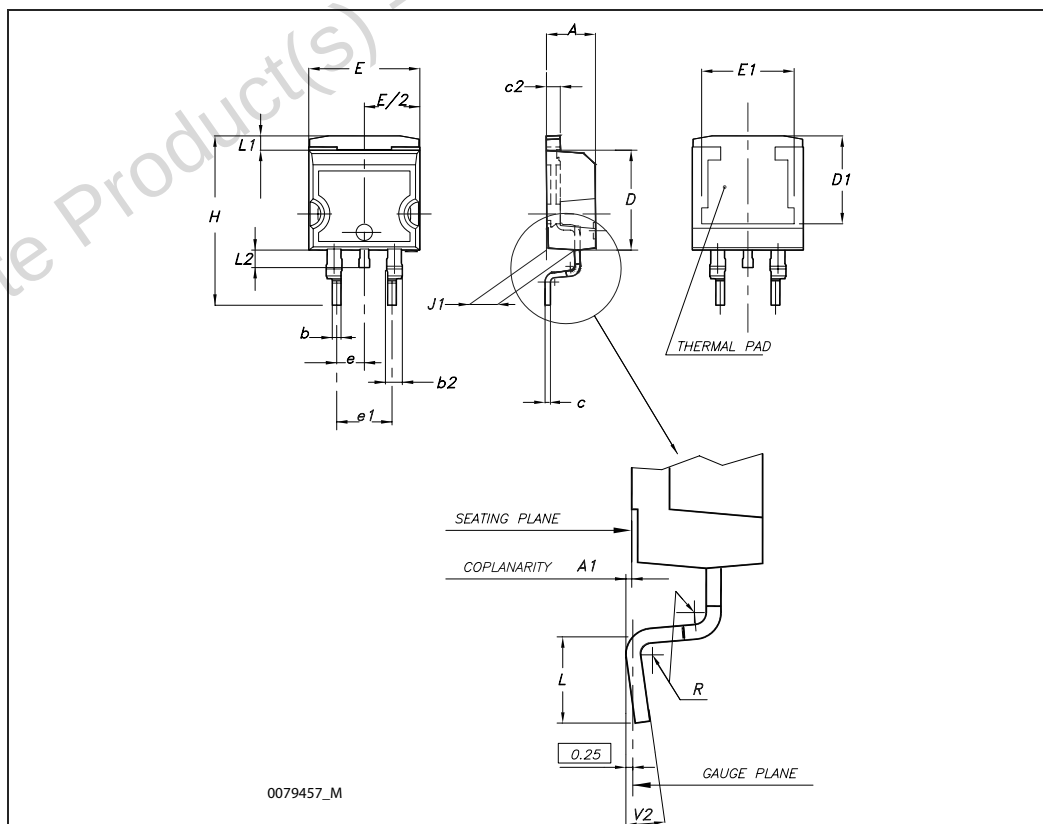
I²PAK (TO-262) mechanical data

Dim	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A	4.40		4.60	0.173		0.181
A1	2.40		2.72	0.094		0.107
b	0.61		0.88	0.024		0.034
b1	1.14		1.70	0.044		0.066
c	0.49		0.70	0.019		0.027
c2	1.23		1.32	0.048		0.052
D	8.95		9.35	0.352		0.368
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
E	10		10.40	0.393		0.410
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L2	1.27		1.40	0.050		0.055



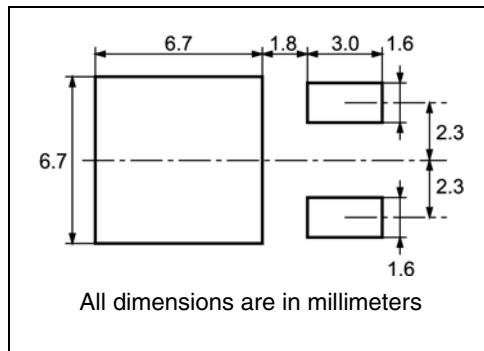
D²PAK (TO-263) mechanical data

Dim	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A	4.40		4.60	0.173		0.181
A1	0.03		0.23	0.001		0.009
b	0.70		0.93	0.027		0.037
b2	1.14		1.70	0.045		0.067
c	0.45		0.60	0.017		0.024
c2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
D1	7.50			0.295		
E	10		10.40	0.394		0.409
E1	8.50			0.334		
e		2.54			0.1	
e1	4.88		5.28	0.192		0.208
H	15		15.85	0.590		0.624
J1	2.49		2.69	0.099		0.106
L	2.29		2.79	0.090		0.110
L1	1.27		1.40	0.05		0.055
L2	1.30		1.75	0.051		0.069
R		0.4			0.016	
V2	0°		8°	0°		8°

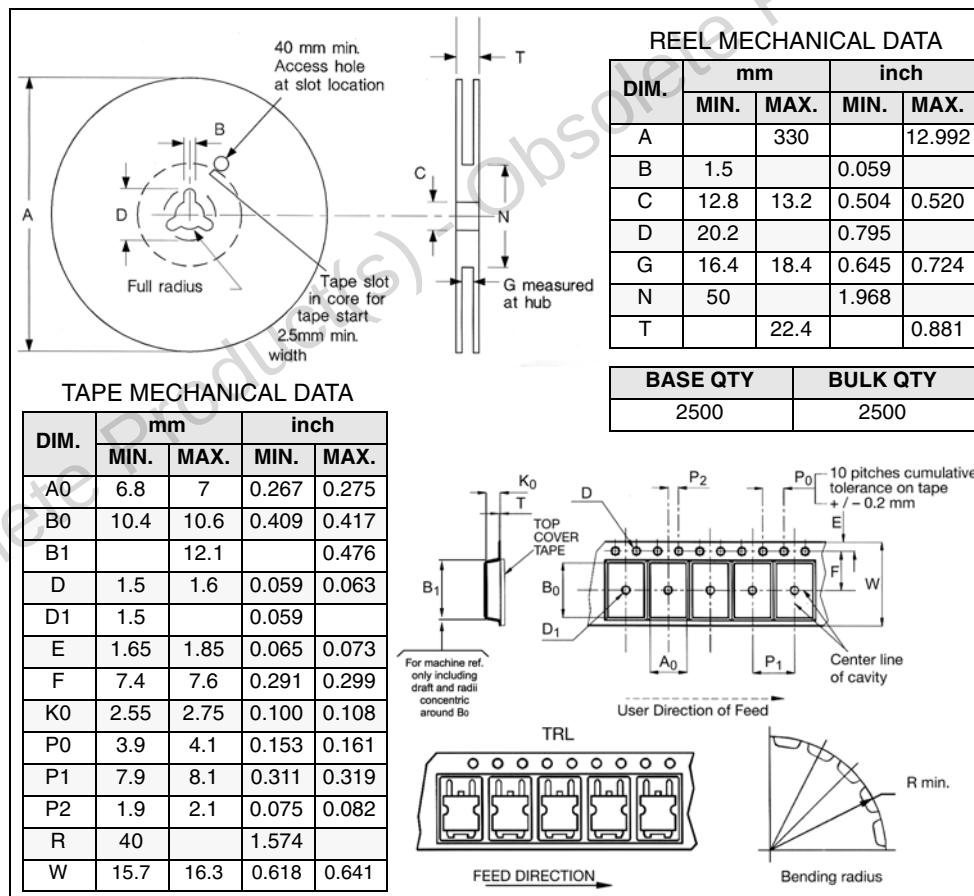


5 Packaging mechanical data

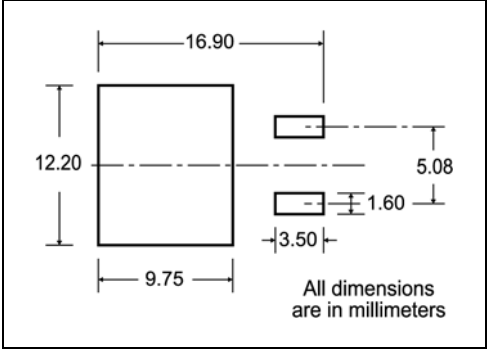
DPAK FOOTPRINT



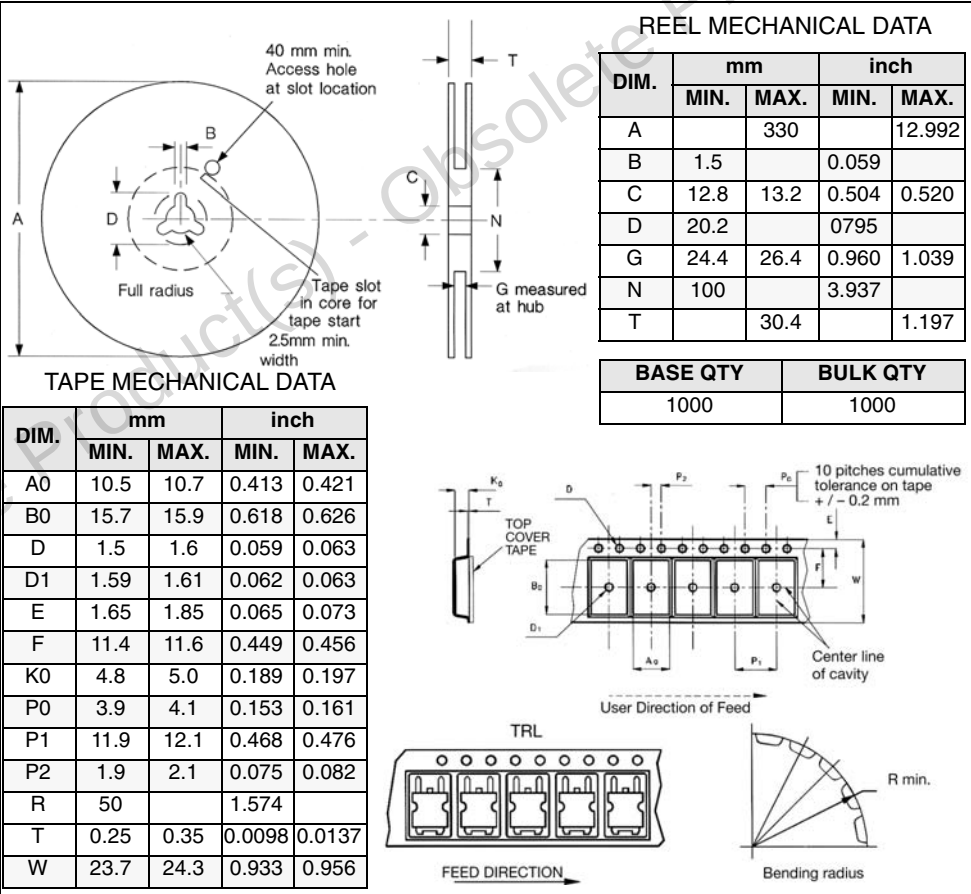
TAPE AND REEL SHIPMENT



D²PAK FOOTPRINT



TAPE AND REEL SHIPMENT



* on sales type

6 Revision history

Table 9. Document revision history

Date	Revision	Changes
24-May-2005	1	Initial release
10-Jun-2005	2	Inserted new row in Table 7.: Switching times
28-Sep-2005	3	Document status promoted from preliminary data to datasheet.
14-Oct-2005	4	Modified Figure 6 , Figure 9
06-Mar-2006	5	Modified Figure 8
29-Mar-2006	6	Modified value on Table 5 .
14-Nov-2006	7	Document reformatted no content change
24-Jul-2008	8	– Added I²PAK; – Table 3: Thermal data has been updated; – Figure 11: Capacitance variations changed.

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