



SGM61006

High Efficiency 600mA Buck Converter

GENERAL DESCRIPTION

The SGM61006 is a high efficiency and miniature size synchronous Buck converter for low input voltage applications. This high frequency device does not need external compensation and is a perfect solution for compact designs. The 1.8V to 5.5V input voltage range is suitable for kinds of battery applications. The minimum input voltage can be as low as 1.6V after startup. It operates in PWM mode at heavy loads and automatically enters power-save mode (PSM) at light loads to maintain its high efficiency.

This device allows a wide range of output capacitors from 22μF to 100μF and even more. This flexibility makes the device a good choice for system power rails supplies. With its adaptive hysteresis and pseudo-constant on-time control (AHP-COT) architecture, the load transient performance is excellent and the output voltage regulation accuracy is achieved. The device is available in a Green WLCSP-0.9×1.3-6B-A package.

FEATURES

- 1.8V to 5.5V Input Voltage Range
- 0.5V to V_{IN} Adjustable Output Voltage
- AHP-COT Architecture for Fast Transient Regulation
- Up to 90% Efficiency
- Low $R_{DS(on)}$ MOSFET Switches (100m Ω /95m Ω)
- 26 μ A (TYP) Operating Quiescent Current
- Power-Save Mode for Light Load Efficiency
- 100% Duty Cycle for Lowest Dropout
- Output Discharge Function
- Power Good Output
- Thermal Shutdown Protection
- Available in a Green WLCSP-0.9 \times 1.3-6B-A Package

APPLICATIONS

- Battery-Powered Applications
- Point-of-Load
- Processor Supplies
- OLED/LCD Module Power Supply

TYPICAL APPLICATION

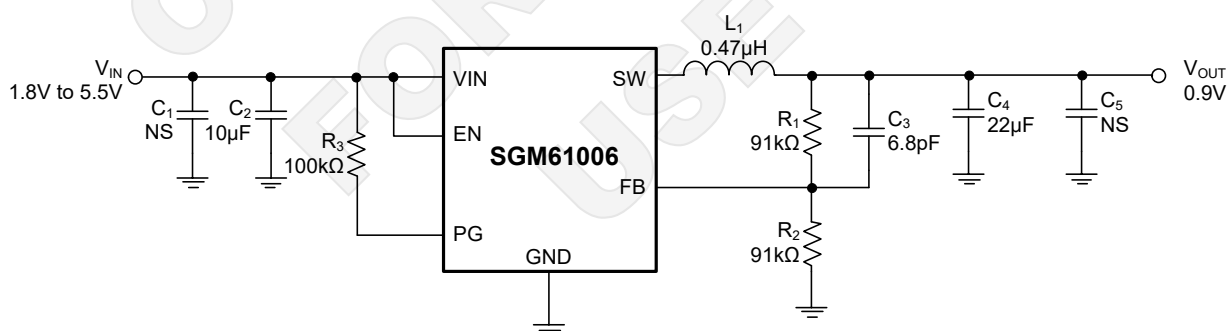


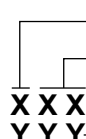
Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM61006	WLCSP-0.9×1.3-6B-A	-40°C to +125°C	SGM61006XG/TR	XXX MBX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXX = Date Code and Trace Code.


 Date Code - Year
 Trace Code
 XXX
 YYY — Serial Number

Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Voltages Referred to GND

VIN, FB, EN, PG -0.3V to 6V

SW (DC) -0.3V to VIN + 0.3V

SW (AC, Less than 10ns) while Switching -2V to 8V

Package Thermal Resistance

WLCSP-0.9×1.3-6B-A, θ_{JA} 158°C/W

Junction Temperature +150°C

Storage Temperature Range -65°C to +150°C

Lead Temperature (Soldering, 10s) +260°C

ESD Susceptibility

HBM 2000V

CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Input Voltage Range, VIN 1.8V to 5.5V

Output Voltage Range, VOUT 0.5V to VIN

Sink Current at PG Pin, ISINK_PG 1mA

Pull-Up Resistor Voltage, VPG 5.5V

Operating Junction Temperature -40°C to +125°C

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

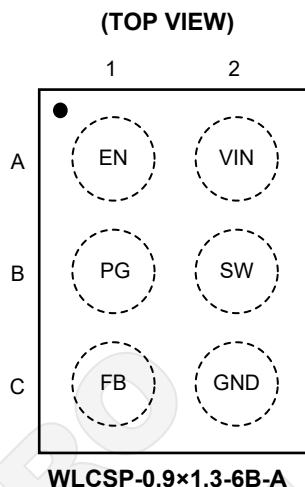
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION



PIN DESCRIPTION

PIN	NAME	I/O	DESCRIPTION
A1	EN	I	Active High Device Enable Input Pin. Pull this pin to logic high to enable the device and pull it low to disable it. An internal 435kΩ (TYP) pull-down resistor disables the device by default. This resistor is removed when the device is enabled.
A2	VIN	P	Input Voltage Pin.
B1	PG	O	Open-Drain Power Good Output Pin. This output is released to go high if the device is in power good status. Pull up this pin to a 5.5V or less voltage rail. It can be left open if not used.
B2	SW	P	Switch Node of the Power Converter. Connect it to the output inductor.
C1	FB	I	Feedback Pin. Connect a resistor divider between the output voltage sense point and ground and tap it to the FB pin to set the output voltage.
C2	GND	G	Ground Pin.

NOTE: I = input, O = output, G = ground, P = power.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 3.3V, T_J = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply						
Quiescent Current into VIN Pin	I _Q	Not switching		26		μA
Shutdown Current into VIN Pin	I _{SD}	EN = Low		0.01		μA
Under-Voltage Lockout Threshold	V _{UVLO}	V _{IN} falling		1.5		V
		V _{IN} rising		1.575		V
Thermal Shutdown	T _{JSD}	Junction temperature rising		150		°C
		Junction temperature falling		135		°C
Logic Interface						
High-Level Threshold at EN Pin	V _{IH}	T _J = -40°C to +125°C	1.2			V
Low-Level Threshold at EN Pin	V _{IL}	T _J = -40°C to +125°C			0.4	V
Pull-Down Resistance at EN Pin	R _{PD}	EN = Low		435		kΩ
EN Input Leakage Current	I _{ENLKG}	V _{EN} = V _{IN} = 5.5V		0.05		μA
Power Good						
Power Good Threshold	V _{PG}	V _{PG} rising, V _{FB} referenced to V _{FB} nominal		96.1		%
		V _{PG} falling, V _{FB} referenced to V _{FB} nominal		91.1		
V _{OUT} Over-Voltage Threshold	V _{OVF}	V _{PG} rising, V _{FB} referenced to V _{FB} nominal		105.4		%
		V _{PG} falling, V _{FB} referenced to V _{FB} nominal		110.4		
Power Good Low-Level Output Voltage	V _{PG_OL}	I _{SINK} = 1mA		0.1		V
Input Leakage Current into PG Pin	I _{PG_LKG}	V _{PG} = 5.0V		0.01		μA
Output						
Feedback Regulation Voltage	V _{FB}	PWM mode		0.450		V
Feedback Input Leakage Current	I _{FB}	V _{FB} = 0.45V		0.01		μA
Output Discharge Resistor	R _{DIS}	EN = Low, V _{OUT} = 1.8V		1032		Ω
Power Switch						
High-side FET On-Resistance	R _{DS(ON)}	V _{IN} = 1.8V, I _{SW} = 500mA		181		mΩ
		V _{IN} = 3.3V, I _{SW} = 500mA		99		
Low-side FET On-Resistance		V _{IN} = 1.8V, I _{SW} = 500mA		165		mΩ
		V _{IN} = 3.3V, I _{SW} = 500mA		95		
High-side FET Current Limit	I _{LIM}	Rising inductor current		1.2		A
Switching Frequency	f _{SW}	V _{OUT} = 1.2V		3.5		MHz

The diagram illustrates the control architecture of a synchronous buck converter. Key components and their interconnections include:

- Enable Logic:** The **EN** pin is connected to a 435kΩ resistor and a MOSFET gate. The MOSFET's source is grounded, and its drain is connected to the **Enable** pin.
- Control Logic:** Receives inputs from **UVLO** (Undervoltage Lockout), **Thermal Shutdown**, **MIN_ON**, **MIN_OFF**, **Adaptive On-Time**, **PWM**, **PSM** (Pulse-Width Modulation), **High-side Current Limit** (V_{HCL}), and **Low-side Current Limit** (V_{LCL}).
- Gate Driver:** Receives the **PWM** signal from the **Control Logic** and drives the gates of the high-side and low-side MOSFETs.
- Power Stage:** Consists of a high-side MOSFET and a low-side MOSFET. The high-side MOSFET's source is connected to **VIN**, and the low-side MOSFET's source is connected to **GND**. The drains are connected to the **SW** (switching node).
- Active Output Discharge:** A MOSFET circuit that discharges the output capacitor when the **EN** pin is pulled down.
- Feedback and Regulation:** The **FB** (feedback) pin is connected to the output voltage divider. The **Soft-Start** pin is connected to the **SS** (soft-start) pin of the **Control Logic**. The **Bandgap** reference is connected to the **EA** (error amplifier) input.
- Current Limiting:** The **High-side Current Limit** (V_{HCL}) and **Low-side Current Limit** (V_{LCL}) comparators monitor the MOSFETs for overcurrent.
- Zero-Current Detection (ZCD):** The **ZCD** comparator monitors the low-side MOSFET for zero-current conditions, outputting V_{ZCD} .
- Protection:** The **UVLO** (Undervoltage Lockout) and **Thermal Shutdown** comparators provide protection against undervoltage and overheating.

Figure 2. Block Diagram

DETAILED DESCRIPTION

Overview

The SGM61006 is a high-efficiency Buck converter with AHP-COT architecture and advanced regulation topology.

At medium to heavy loads, the device works in pulse width modulation (PWM) mode. At light loads, it automatically switches to power-save mode (PSM). In PWM mode, the device works with a nominal switching frequency of 3.5MHz. When the load current falls, the device goes into PSM to achieve high efficiency with reducing switching frequency and minimizing quiescent current. PSM mode can reduce the standby energy consumption of system. During shutdown mode, the energy consumption falls below 1μA.

Under-Voltage Lockout (UVLO)

The device implements the under-voltage lockout (UVLO) with a 75mV (TYP) hysteresis. When the input voltage falls below the V_{UVLO} , it shuts down the device.

Enable and Disable

A logic high input to EN activates the device, and a logic low disables the device. An internal 435kΩ (TYP) pull-down resistor disables the device by default. This resistor is removed when the device is enabled.

Power Good (PG)

The power good output of SGM61006 will be low in the condition that the output voltage is less than its nominal value. If the output exceeds 96.1% of the regulated voltage, the power good is in high-impedance state. If the output voltage is less than 91.1% of the regulated voltage, the power good is driven to low.

The PG pin is an open-drain output with a maximum sink current of 1mA. A pull-up resistor connecting to power good output is required. When the device is disabled or under-voltage lockout, the PG pin is driven to low (see Table 1). The PG signal connected to the

EN pin of other converters can be used for multiple rails sequences. Leave the PG pin floating when not in use.

Table 1. Logic Table of PG Pin

Device Information		Logic Status	
		High Z	Low
Enable (EN = High)	EN = High, V_{FB} Rising $\geq 0.433V$	√	
	EN = High, V_{FB} Falling $\leq 0.410V$		√
	EN = High, V_{FB} Rising $\geq 0.497V$		√
	EN = High, V_{FB} Falling $\leq 0.474V$	√	
Shutdown (EN = Low)			√
UVLO	$0.7V < V_{IN} < V_{UVLO}$		√
Thermal Shutdown	$T_J > T_{JSD}$		√
Power Supply Removal	$V_{IN} < 0.7V$	undefined	

100% Duty Cycle

The device provides low input-to-output voltage drop by going into 100% duty cycle mode. In this mode, the high-side MOSFET is constantly turned on and the low-side MOSFET is turned off. This function can increase the operation time to the utmost extent for battery powered applications. To maintain an appropriate output voltage, the minimum input voltage is calculated by:

$$V_{IN_MIN} = V_{OUT} + I_{OUT_MAX} \times (R_{DS(on)} + R_L) \quad (1)$$

where:

- V_{IN_MIN} is the minimum input voltage.
- I_{OUT_MAX} is the maximum output current.
- $R_{DS(on)}$ is the high-side MOSFET on-resistance.
- R_L is the inductor ohmic resistance.

Output Discharge

Whenever the device is disabled by enable, thermal shutdown or under-voltage lockout, the output is discharged by the SW pin through a typical discharge resistor of R_{DIS} .

DETAILED DESCRIPTION (continued)

Soft-Start

When EN is set to logic high and after about 260 μ s delay, the device starts switching and V_{OUT} increases with 600 μ s (TYP) internal soft-start circuit.

Inductor Current Limit

The device implements an inductor current limit if there is over-current or short-circuit. Both the peak current of high-side and valley current of low-side power MOSFETs are limited to protect the device. The high-side MOSFET is turned off and the low-side MOSFET is turned on to reduce the inductor current when the high-side switch current limit is triggered. The low-side MOSFET is turned off and the high-side switch is turned on again when the inductor current drops to the low-side switch current limit. It repeats until the inductor current falls below the high-side switch current limit. The actual current limit value may be larger than the static current limit due to internal propagation delays.

Power-Save Mode (PSM)

Once the load current decreases, the SGM61006 will enter power-save mode. Then, the device has a reduced switching frequency and works with the minimum quiescent current to keep high efficiency. In power-save mode, the inductor current is discontinuous. Then a fixed on-time architecture is activated and the typical on-time is $t_{ON} = 286\text{ns} \times (V_{OUT}/V_{IN})$.

Thermal Shutdown

To protect the device from overheating damage, thermal protection is included in the device. If the junction temperature exceeds the typical T_{JSD} (+150°C TYP), the switching will stop. When the device temperature drops below the threshold minus hysteresis, the switching will resume automatically.

APPLICATION INFORMATION

The SGM61006 is a synchronous Buck converter with output voltage adjusted by feedback dividers. Taking SGM61006 typical application as a reference, the following sections discuss the design of external components and how to achieve the application.

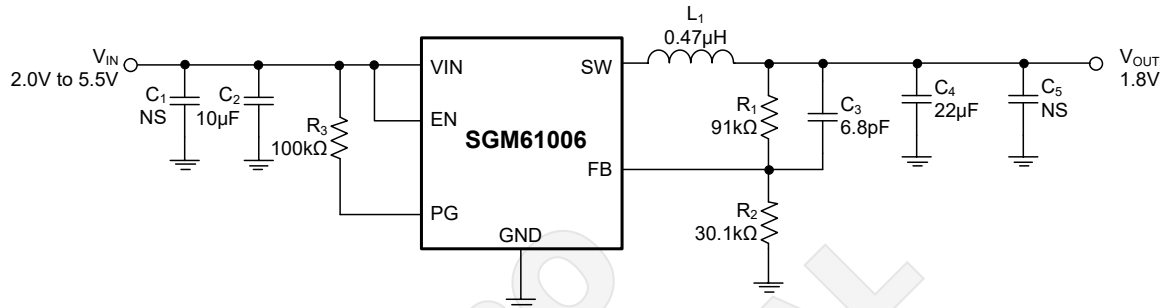


Figure 3. SGM61006 Typical Application Circuit

Requirements

The design parameters given in Table 2 are used for this design example.

Table 2. Design Parameters

Design Parameter	Example Value
Input Voltage	2.0V to 5.5V
Output Voltage	1.8V
Output Ripple Voltage	< 20mV
Output Current (MAX)	600mA

Design Details

Table 3 shows the components included in this example.

Table 3. Components List

Reference	Description	Manufacturer
L ₁	0.47µH, Power Inductor, DCR = 45mΩ, I _{SAT} = 3.3A, I _{RMS} = 2.6A DFE18SANR47MG0L	Murata
C ₂	10µF, Ceramic Capacitor, 10V, X5R, Size 0603	Standard
C ₃	6.8pF, Ceramic Capacitor, 50V, C0G, Size 0603	Standard
C ₄	22µF, Ceramic Capacitor, 10V, X5R, Size 0603	Standard
R ₁	91kΩ, Chip Resistor, 1/16W, 1%, Size 0603	Standard
R ₂	30.1kΩ, Chip Resistor, 1/16W, 1%, Size 0603	Standard
R ₃	100kΩ, Chip Resistor, 1/16W, 1%, Size 0603	Standard

Adjustable Output Voltage

An external resistor divider connected to FB pin is used for setting the output voltage. Through adjusting R₁ and R₂, the output voltage can be programmed to the

desired value. Calculate R₁ and R₂ with Equation 2.

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R_1}{R_2}\right) = 0.45V \times \left(1 + \frac{R_1}{R_2}\right) \quad (2)$$

R₂ should be less than 40kΩ for higher accuracy. Make sure that the current flowing through R₂ is at least 100 times greater than the current of FB pin. A lower value of R₂ increases the robustness against noise injection, and higher values reduce the input current.

A feed-forward capacitor is recommended to improve the performance of smooth transition into power-save mode and reduce undershoot during load transient. 5pF to 10pF is enough for typical applications.

Output Filter

The output low pass filter is the combination of inductor and output capacitor. Table 4 shows the suggested value.

Table 4. Inductor and Capacitor Combinations

L (µH) ⁽¹⁾	C _{OUT} (µF) ⁽²⁾		
	10	22	47
0.33		√	√
0.47		√ ⁽³⁾⁽⁴⁾	√
1	√	√	

NOTES:

- Expected inductor tolerance and current de-rating. Effective inductance has +20% and -30% variation.
- Expected capacitance tolerance and bias voltage de-rating. Effective capacitance has +20% and -50% variation.
- "√" means the recommended filter combinations.
- Filter combination in typical application.

APPLICATION INFORMATION (continued)

Inductor Design

Equation 3 is conventionally used to calculating the output inductance of a Buck converter. The inductor should be selected by its value and the saturation current. The saturation current of inductor should be higher than I_{L_MAX} in Equation 3, and sufficient margin should be reserved. Typically, the current above high-side current limit is enough, and a 20% to 40% ripple current is selected to calculate the inductance. Larger inductor can reduce the ripple current, but with an increasing response time.

$$I_{L_MAX} = I_{OUT_MAX} + \frac{\Delta I_L}{2}$$

$$\Delta I_L = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f_{SW}} \quad (3)$$

where:

- I_{OUT_MAX} is the maximum output current.
- ΔI_L is the inductor current ripple.
- f_{SW} is the switching frequency.
- L is the inductor value.

Capacitor Design

For input capacitor design, an X5R/X7R dielectric ceramic capacitor should be selected for its low ESR and high-frequency performance. 10μF is enough for

most applications. The voltage rating of input capacitor must be considered for its significant bias effect. The input ripple voltage can be calculated from Equation 4.

$$\Delta V_{IN} = \frac{I_{OUT} \times D \times (1-D)}{C_{IN} \times f_{SW}} \quad (4)$$

The ripple current rating of input capacitor should be greater than I_{CIN_RMS} in Equation 5 and the maximum value occurs at 50% duty cycle. A bulk capacitor is suggested to add if the input wire long.

$$I_{CIN_RMS} = I_{OUT} \times \sqrt{\frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times V_{IN}}} = I_{OUT} \times \sqrt{D \times (1-D)} \quad (5)$$

For output capacitor design, output ripple, transient response and loop stability should be considered. Minimum capacitance of output ripple criteria can be calculated from Equation 6.

$$C_{OUT} > \frac{\Delta I_L}{8 \times f_{SW} \times V_{OUT_RIPPLE}} \quad (6)$$

Both the input and output capacitors should be placed as close to VIN and GND pins as possible to reduce noise caused by PCB parasitic parameters.

To simplify customer's design process, the inductor and output capacitor combinations are recommended in Table 4.

APPLICATION INFORMATION (continued)

Layout Considerations

Good PCB layout is the key factor for high performance operation of a device regarding the stability, regulation, efficiency and other performance measures.

A list of guidelines for designing the PCB layout of SGM61006 is provided below:

- ◆ Place the power components close together and connect them with short and wide routes. The

low-side of the capacitors must be connected to GND properly to avoid potential shift.

- ◆ FB pin is noise sensitive and must be placed away from SW. Connect the inductor with a short trace to minimize noise.

- ◆ Typical suggested layout is provided in Table 4.

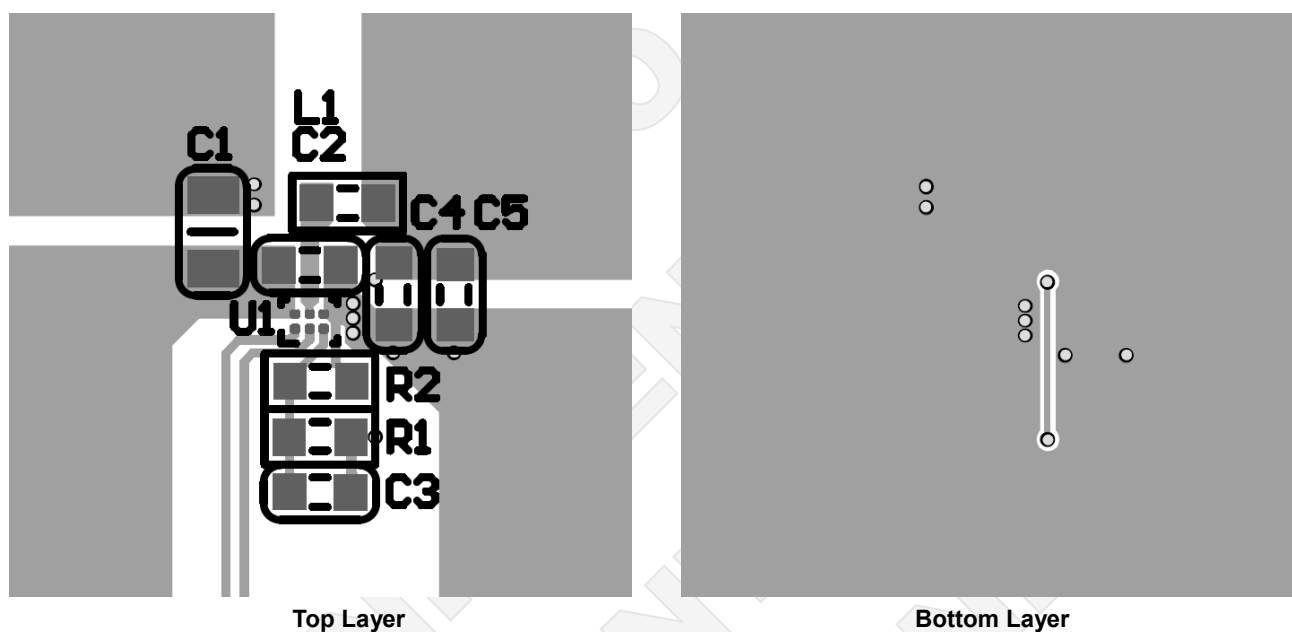
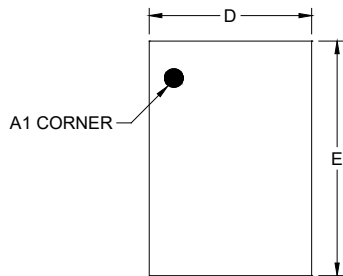


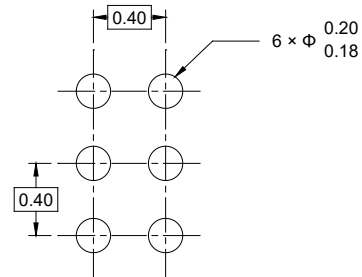
Figure 4. PCB Layout

PACKAGE OUTLINE DIMENSIONS

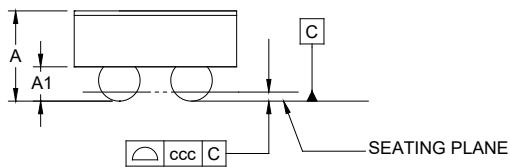
WLCSP-0.9×1.3-6B-A



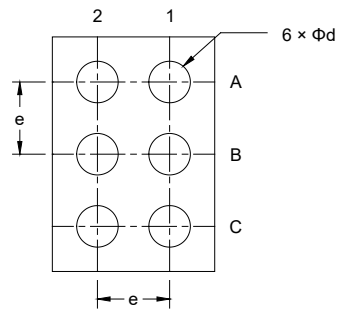
TOP VIEW



RECOMMENDED LAND PATTERN (Unit: mm)



SIDE VIEW



BOTTOM VIEW

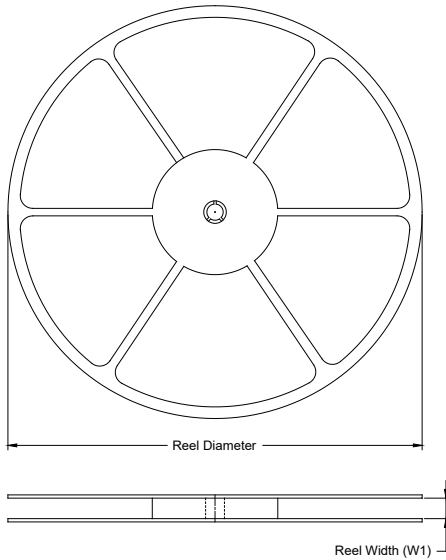
Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	-	-	0.545
A1	0.170	-	0.210
D	0.870	-	0.930
E	1.270	-	1.330
d	0.200	-	0.260
e	0.400 BSC		
ccc	0.050		

NOTE: This drawing is subject to change without notice.

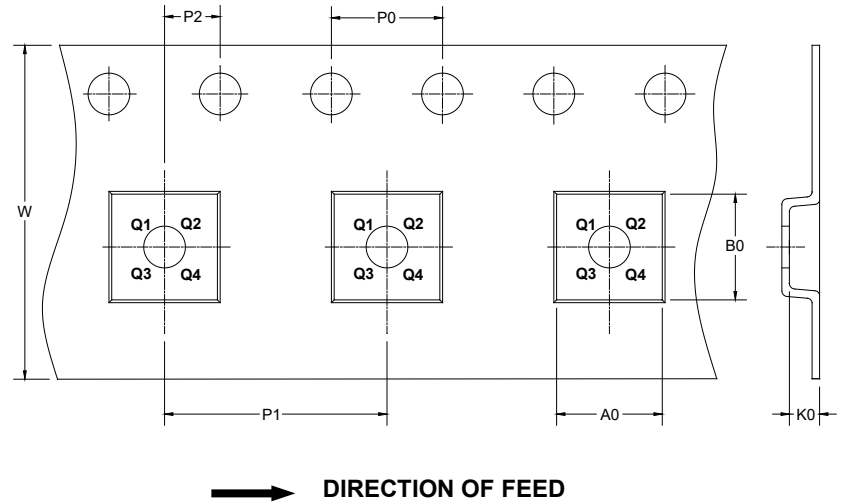
PACKAGE INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
WLCSP-0.9×1.3-6B-A	7"	9.5	1.00	1.40	0.62	4.0	4.0	2.0	8.0	Q1

DD00001

PACKAGE INFORMATION

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7" (Option)	368	227	224	8
7"	442	410	224	18

DD0002