

## DC-to-DC Converter Control Circuits

### DESCRIPTION

The MC33063 series is a monolithic control circuit containing primary functions required for DC-to-DC converters. These devices consist of an internal temperature-compensated reference, comparator, controlled duty cycle oscillator with an active current limit circuit, driver and high current output switch. This series was specifically designed to be incorporated in step-down and step-up and voltage-inverting applications with a minimum number of external components.

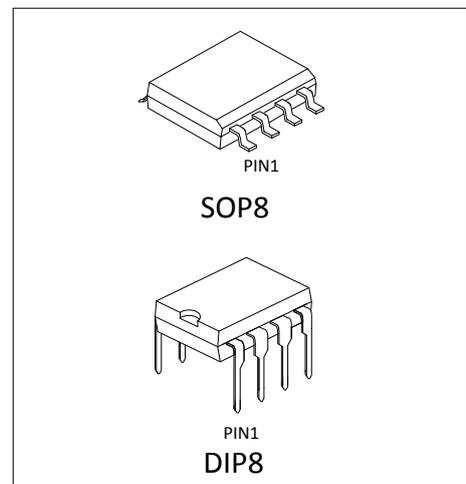
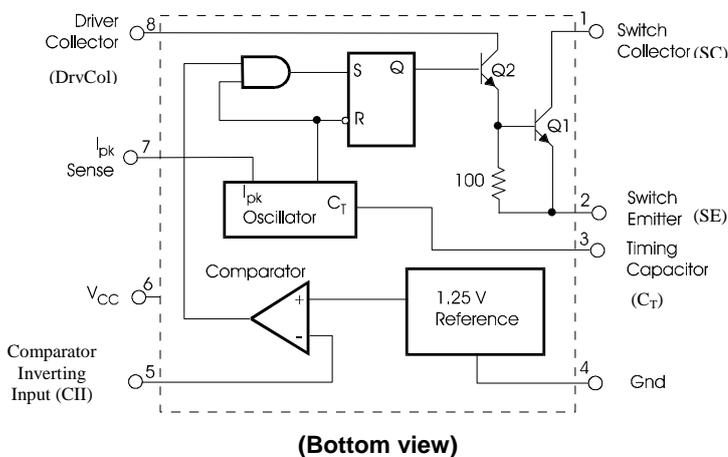
### ORDERING INFORMATION

DEVICE	Package Type	MARKING	Packing	Packing Qty
MC33063N	DIP8	MC33063	TUBE	2000/box
MC33063M/TR	SOP8	MC33063	REEL	2500/reel

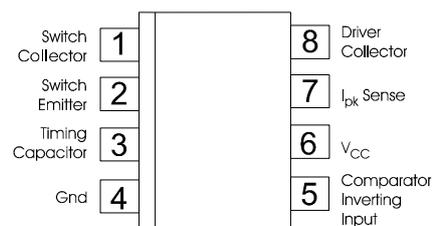
### FEATURES

- Operation from 3.0V to 40V input
- Low standby current
- Current limiting
- Output switch current up to 1.5A
- Adjustable output voltage
- Operation at frequencies up to 100kHz
- Precision reference (2%)

### SCHEMATIC DIAGRAM



### PIN CONNECTIONS



(Top view)

### ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power supply voltage	$V_{CC}$	40	V
Comparator input voltage range	$V_{IR}$	-0.3 to +40	V
Switch collector voltage	$V_{C(Switch)}$	40	V
Switch emitter voltage ( $V_{Pin1}=40V$ )	$V_{E(Switch)}$	40	V
Switch collector-to-emitter voltage	$V_{CE(Switch)}$	40	V
Driver collector voltage	$V_{C(Driver)}$	40	V
Driver collector current (Note 1)	$I_{C(Driver)}$	100	mA
Switch current	$I_{Sw}$	1.5	A
Operating junction temperature	$T_J$	+150	°C
Operating ambient temperature range	$T_A$	-40 to +85	°C
Storage temperature range	$T_{STG}$	-65 to +150	°C
ESD (HBM)		2500	V

**ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5.0V, T<sub>A</sub>=T<sub>Low</sub> to T<sub>High</sub>, unless otherwise specified.)**

Characteristics	Symbol	Min	Typ	Max	Unit
<b>OSCILLATOR</b>					
Frequency (V <sub>Pin5</sub> =0V, C <sub>T</sub> =1.0nF, T <sub>A</sub> =25°C)	f <sub>osc</sub>	24	33	42	kHz
Charge current (V <sub>CC</sub> =5.0V to 40V, T <sub>A</sub> =25°C)	I <sub>chg</sub>	24	35	42	μA
Discharge current (V <sub>CC</sub> =5.0V to 40V, T <sub>A</sub> =25°C)	I <sub>dischg</sub>	140	220	260	μA
Discharge-to-charge current ratio (Pin7 to V <sub>CC</sub> , T <sub>A</sub> =25°C)	I <sub>dischg</sub> /I <sub>chg</sub>	5.2	6.5	7.5	-
Current limit sense voltage (I <sub>chg</sub> =I <sub>dischg</sub> , T <sub>A</sub> =25°C)	V <sub>lpk(sense)</sub>	250	300	350	mV
<b>OUTPUT SWITCH (Note 2)</b>					
Saturation voltage, Darlington connection I <sub>Sw</sub> =1.0A, Pins1, 8 connected	V <sub>CE(sat)</sub>	-	1.0	1.3	V
Saturation voltage, Darlington connection (I <sub>Sw</sub> =1.0A, R <sub>Pin8</sub> =82Ω to V <sub>CC</sub> , forced β=20)	V <sub>CE(sat)</sub>	-	0.45	0.7	V
DC current gain (I <sub>Sw</sub> =1.0A, V <sub>CE</sub> =5.0, T <sub>A</sub> =25°C)	h <sub>FE</sub>	50	75	-	-
Collector off-state current (V <sub>CE</sub> =40V)	I <sub>C(off)</sub>	-	1.0	100	μA
<b>COMPARATOR</b>					
Threshold voltage	V <sub>th</sub>	1.225 1.21	1.25 -	1.275 1.29	V
Threshold voltage line regulation (V <sub>CC</sub> =3.0V to 40V)	Reg <sub>line</sub>	-	1.4	5.0	mV
Input bias current (V <sub>in</sub> =0V)	I <sub>IB</sub>	-	-20	-400	nA
<b>TOTAL DEVICE</b>					
Supply current (V <sub>CC</sub> =5.0V to 40V, C <sub>T</sub> =1.0nF, Pin7=V <sub>CC</sub> , V <sub>Pin5</sub> >V <sub>th</sub> , Pin2=Gnd, remaining pins - open)	I <sub>CC</sub>	-	-	4.0	mA

**Notes:**

1. Maximum package power dissipation limits must be observed.
2. Low duty cycle pulse techniques are used during the test to maintain the junction temperature as close to the ambient temperature as possible.

**TYPICAL PERFORMANCE CHARACTERISTICS**

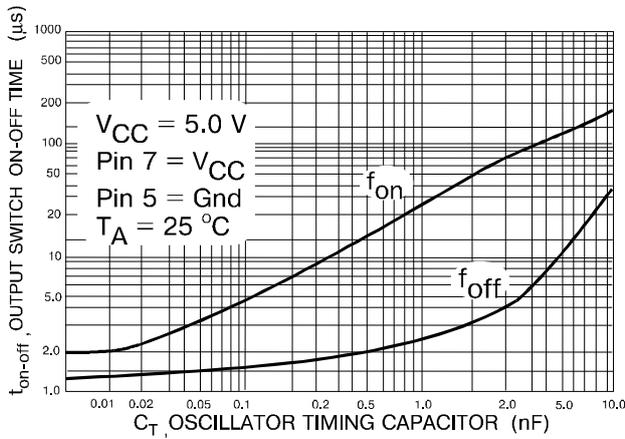


Fig.1. Output Switch on-off time versus Oscillator timing capacitor

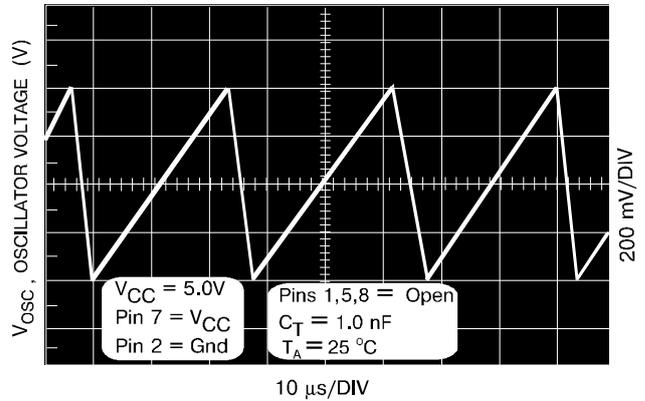


Fig.2. Timing capacitor waveform

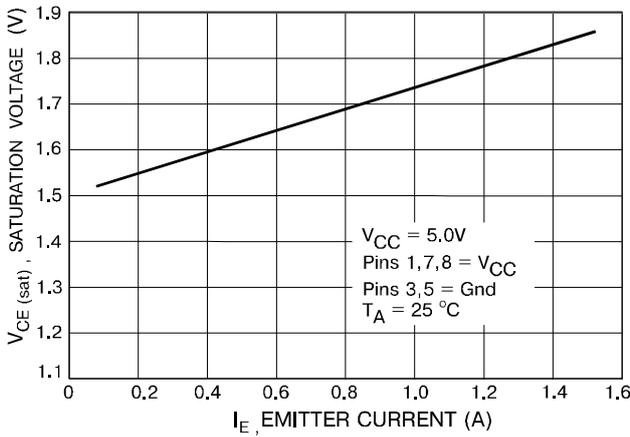


Fig.3. Emitter follower configuration output saturation voltage versus Emitter current

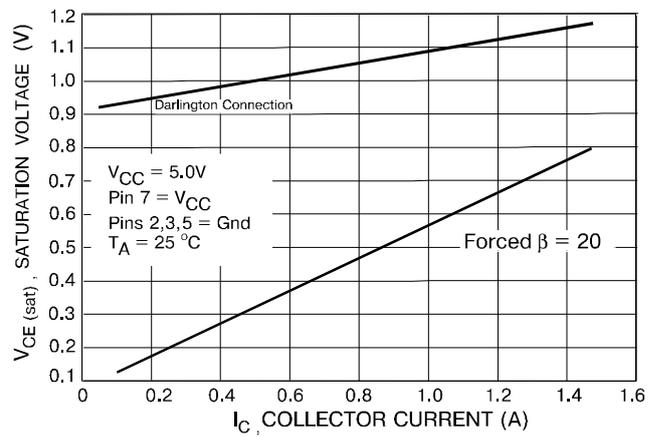


Fig.4. Common emitter configuration output saturation voltage versus Collector current

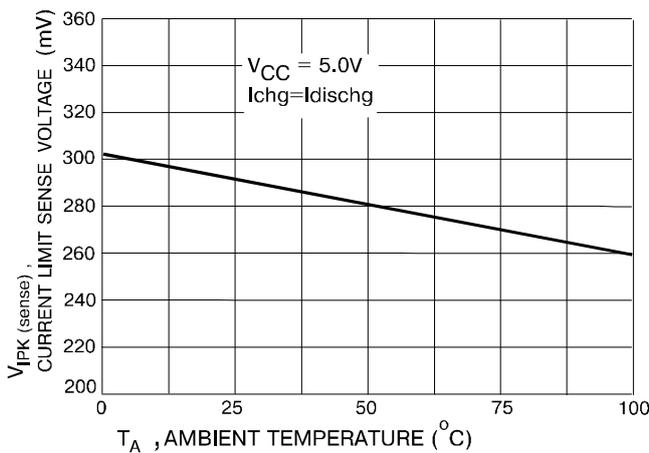


Fig.5. Current limit sense voltage versus Temperature

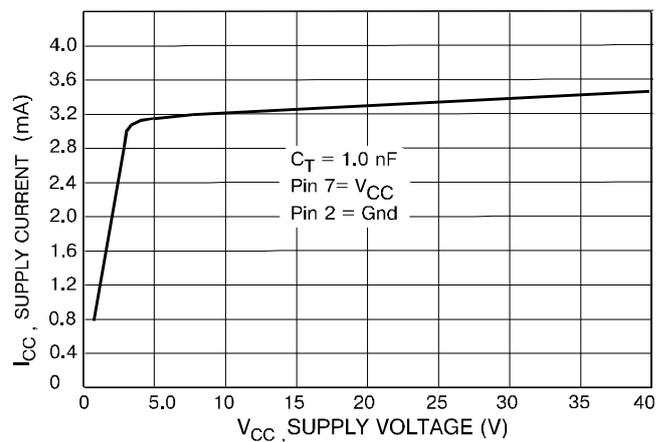
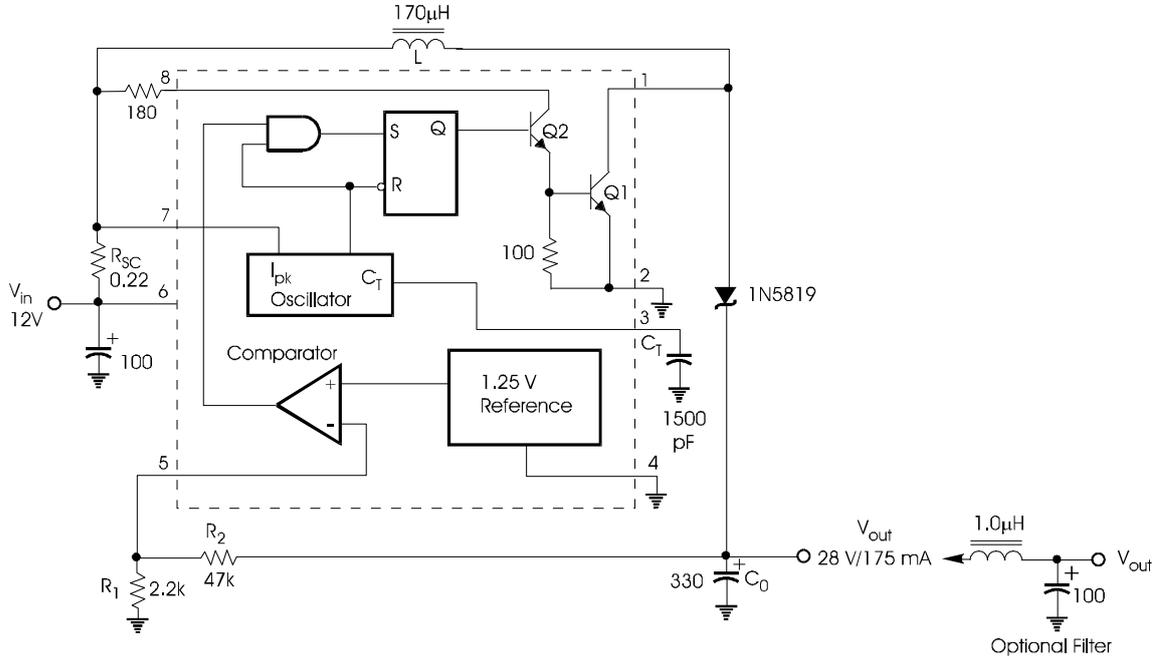


Fig.6. Standby supply current versus Supply voltage

**APPLICATION INFORMATION**

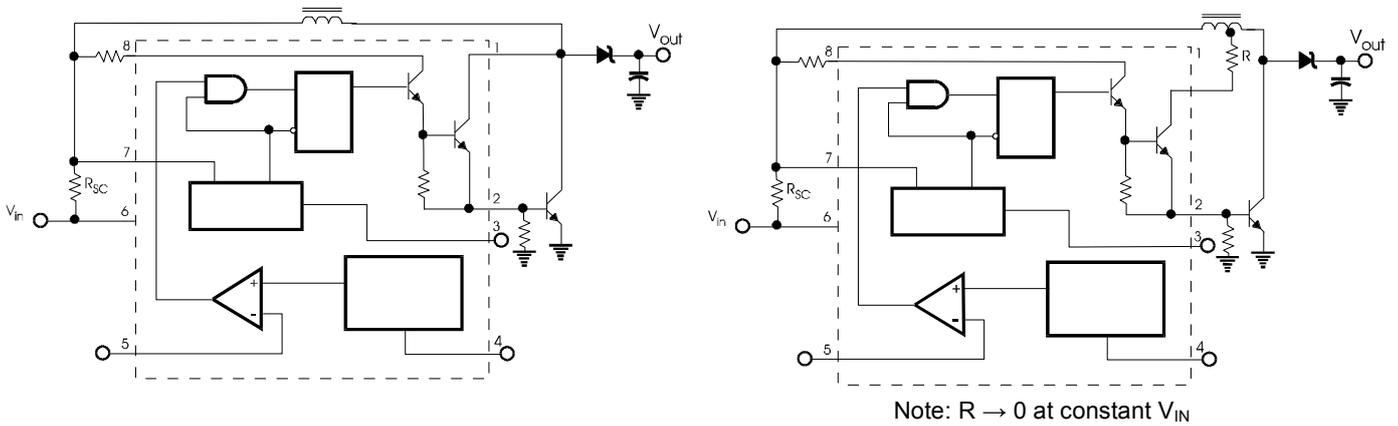
**Fig.1. Step-up converter**



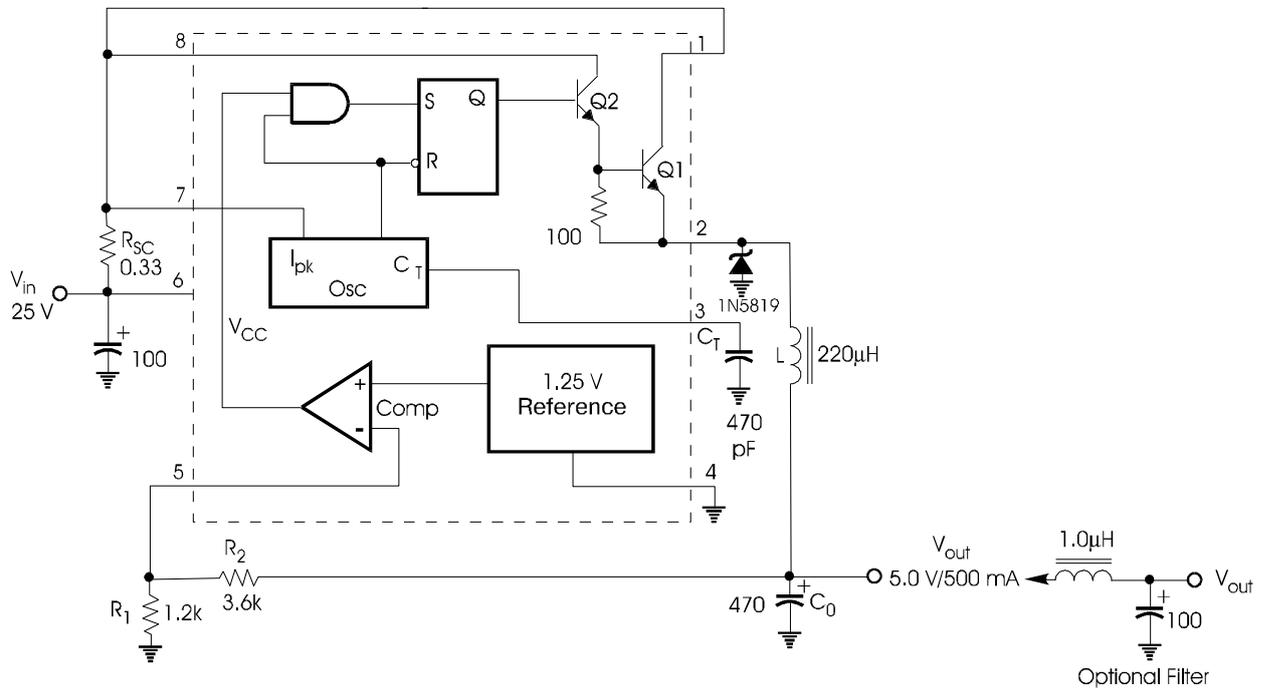
**Fig.2. External current boost connections for  $I_C$  Peak greater than 1.5A**

**2a. External NPN switch**

**2b. External NPN saturated switch**



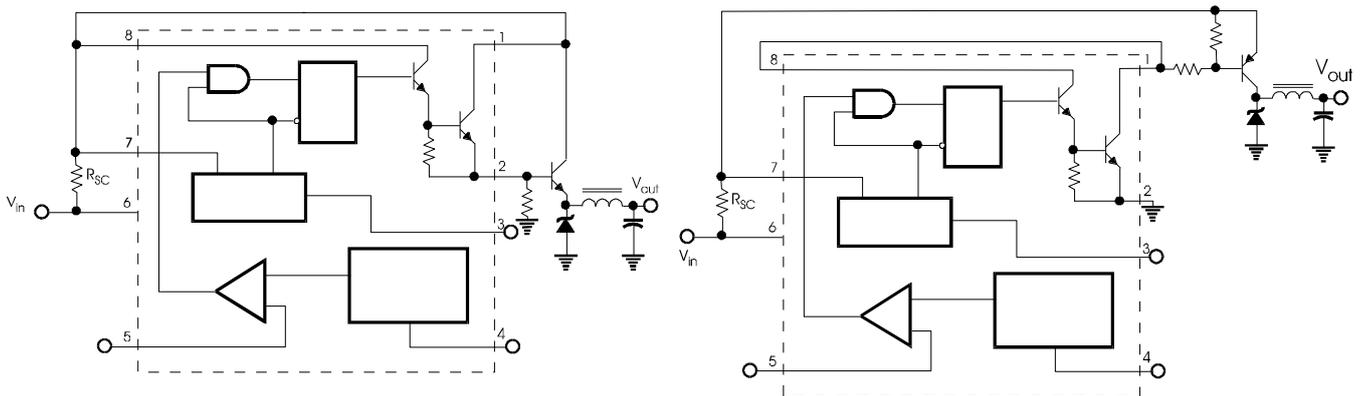
**Fig.3. Step-down Converter**



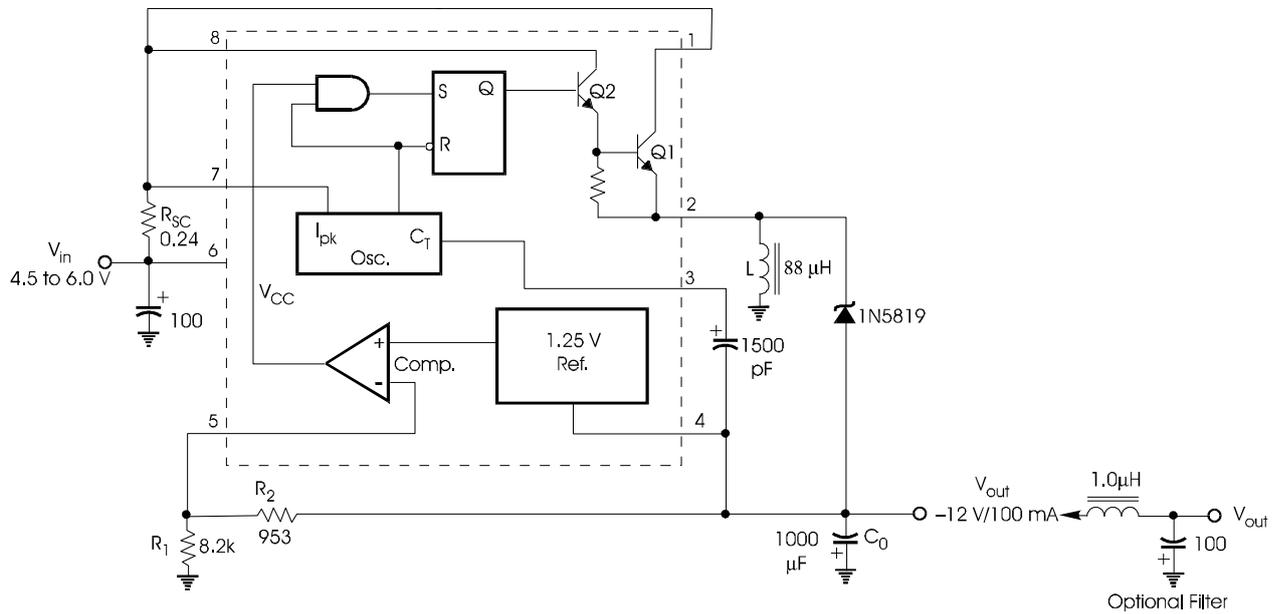
**Fig.4. External current boost connections for  $I_{C\ Peak}$  greater than 1.5A**

**4a. External NPN switch**

**4b. External PNP saturated switch**

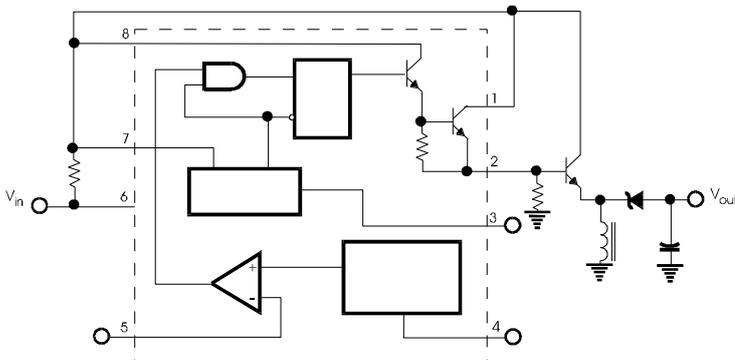


**Fig.5. Voltage inverting converter**

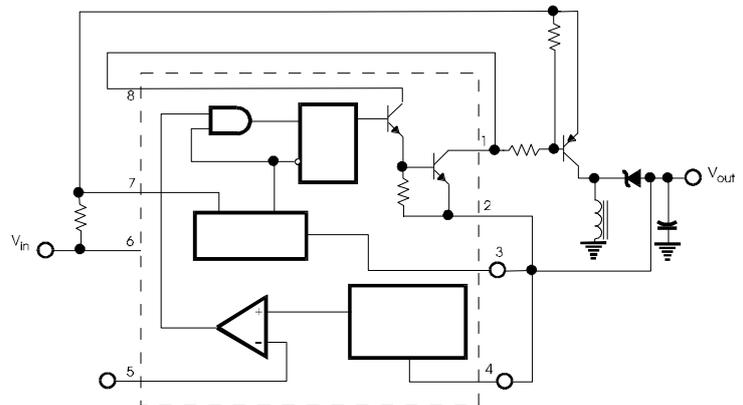


**Fig.6. External current boost connections for  $I_{C\ Peak}$  greater than 1.5A**

**6a. External NPN switch**



**6b. External PNP saturated switch**



**DESIGN FORMULA**

Calculation	Step-up	Step-down	Voltage-inverting
$t_{on}$	$\frac{V_{out} + V_F - V_{in(min)}}{V_{in(min)} - V_{sat}}$	$\frac{V_{out} + V_F}{V_{in(min)} - V_{sat} - V_{out}}$	$\frac{ V_{out}  + V_F}{V_{in} + V_{sat}}$
$(t_{on} + t_{off})_{max}$	$\frac{1}{f_{min}}$	$\frac{1}{f_{min}}$	$\frac{1}{f_{min}}$
$C_T$	$4.0 \times 10^{-5} t_{on}$	$4.0 \times 10^{-5} t_{on}$	$4.0 \times 10^{-5} t_{on}$
$I_{pk( switch )}$	$2I_{out(max)} \left( \frac{t_{on}}{t_{off}} + 1 \right)$	$2I_{out(max)}$	$2I_{out(max)} \left( \frac{t_{on}}{t_{off}} + 1 \right)$
$R_{sc}$	$0.3/I_{pk( Switch )}$	$0.3/I_{pk( Switch )}$	$0.3/I_{pk( Switch )}$
$L_{(min)}$	$\left( \frac{V_{in(min)} - V_{sat}}{I_{pk( switch )}} \right) \times t_{on(max)}$	$\left( \frac{V_{in(min)} - V_{sat} - V_{out}}{I_{pk( switch )}} \right) \times t_{on(max)}$	$\left( \frac{V_{in(min)} - V_{sat}}{I_{pk( switch )}} \right) \times t_{on(max)}$
$C_o$	$9 \frac{I_{out} t_{on}}{V_{ripple(pp)}}$	$\frac{I_{pk( switch )} (t_{on} + t_{off})}{8V_{ripple(pp)}}$	$9 \frac{I_{out} t_{on}}{V_{ripple(pp)}}$

**TERMS AND DEFINITIONS**

$V_{sat}$  – Saturation voltage of the output switch.

$V_F$  – Forward voltage drop of the output rectifier.

**The following power supply characteristics must be chosen:**

$V_{in}$  – Nominal input voltage.

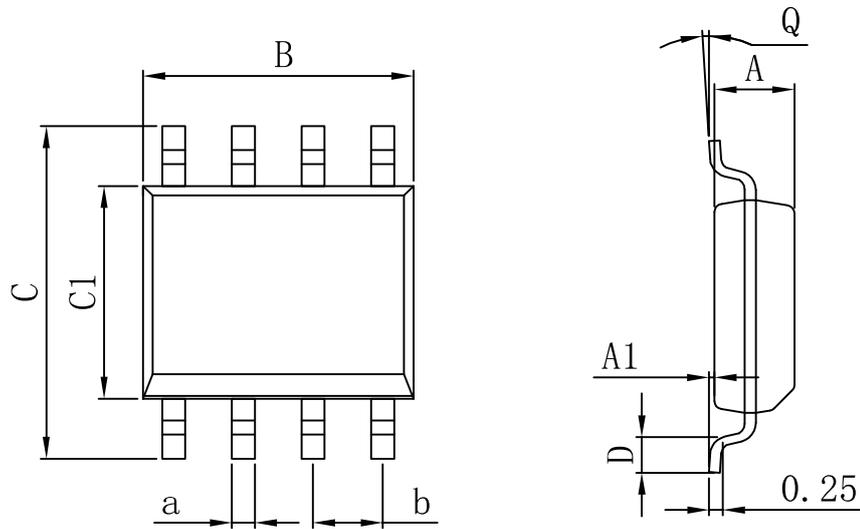
$V_{out}$  – Desired output voltage,  $|V_{out}| = 1.25 \left( 1 + \frac{R_2}{R_1} \right)$

$f_{min}$  – Minimum desired output switching frequency at the selected values of  $V_{in}$  and  $I_{out}$ .

$V_{ripple(p-p)}$  – Desired peak-to-peak output ripple voltage. In practice, the calculated capacitor value will need to be increased due to its equivalent series resistance and board layout. The ripple voltage should be kept to a low value since it will directly affect the line and load regulation.

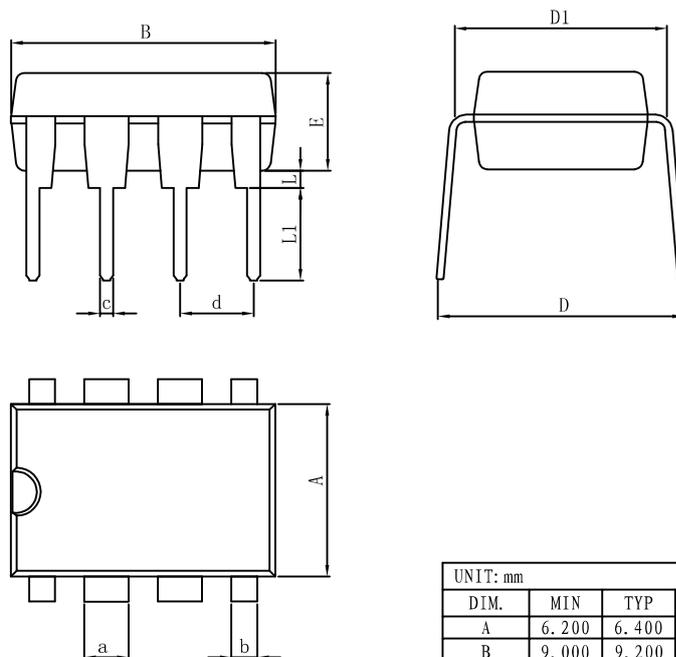
PACKAGE

SOP8



UNIT: mm							
DIM.	MIN	TYP	MAX	DIM.	MIN	TYP	MAX
A	4.520	4.570	4.620	a	0.400	0.420	0.440
A1	0.100	-	0.250	b	1.260	1.270	1.280
B	4.800	4.920	5.100	Q	0°	-	8°
C	5.800	6.100	6.250				
C1	3.800	3.900	4.000				
D	0.400	-	0.950				

DIP8



UNIT: mm							
DIM.	MIN	TYP	MAX	DIM.	MIN	TYP	MAX
A	6.200	6.400	6.680	a	1.504	1.524	1.544
B	9.000	9.200	9.500	b	-	0.889	-
D	8.200	8.700	9.200	c	0.437	0.457	0.477
D1	7.42	7.62	7.82	d	2.530	2.540	2.550
E	3.100	3.300	3.550	L	0.500	-	0.700
				L1	3.000	3.200	3.600

### Important statement:

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