

N-Channel and P-Channel Enhancement Mode Power MOSFET

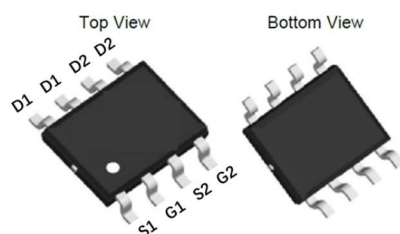
Features

- N-Channel: 60V, 5A
 $R_{DS(ON)} < 28 \text{ m}\Omega @ V_{GS} = 10\text{V}$
 $R_{DS(ON)} < 31 \text{ m}\Omega @ V_{GS} = 4.5\text{V}$
- P-Channel: -60V, -3.1A
 $R_{DS(ON)} < 62 \text{ m}\Omega @ V_{GS} = -10\text{V}$
 $R_{DS(ON)} < 72 \text{ m}\Omega @ V_{GS} = -4.5\text{V}$

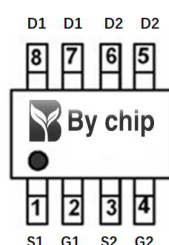
General Features

- Advanced Trench Technology
- Provide Excellent $R_{DS(ON)}$ and Low Gate Charge
- Lead Free and Green Available

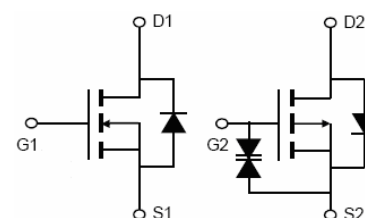
100% UIS TESTED!
100% ΔV_{ds} TESTED!



SOP-8 Dual



Pin Assignment



Schematic diagram

Absolute Maximum Ratings $T_C = 25^\circ\text{C}$, unless otherwise noted

Parameter	Symbol	NMOS	PMOS	Unit
Drain-Source Voltage	V_{DS}	60	-60	V
Continuous Drain Current	I_D	5	-3.1	A
Pulsed Drain Current (note1)	I_{DM}	20	-12.4	A
Gate-Source Voltage	V_{GS}	± 20	± 20	V
Power Dissipation	P_D	2.5	1.9	W
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 To 150	-55 To 150	$^\circ\text{C}$

Thermal Resistance

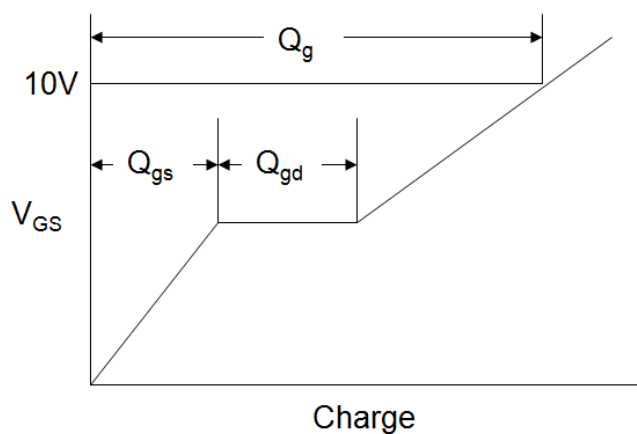
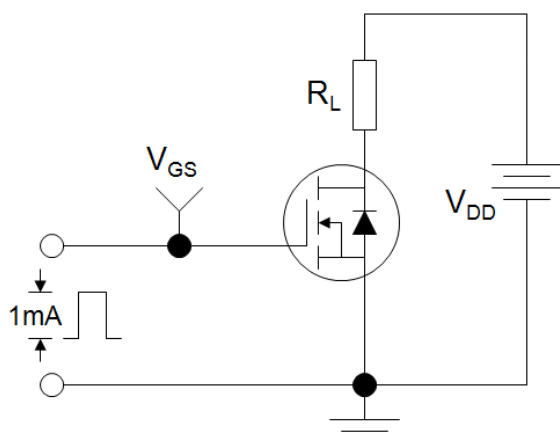
Parameter	Symbol	NMOS	PMOS	Unit
Thermal Resistance, Junction-to-Ambient	R_{thJA}	50	65	$^\circ\text{C/W}$

NMOS Specifications T _J = 25°C, unless otherwise noted						
Parameter	Symbol	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
Static Parameters						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0V, I _D = 250μA	60	--	--	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 60V, V _{GS} = 0V, T _J = 25°C	--	--	1	μA
Gate-Source Leakage	I _{GSS}	V _{GS} = ±20V	--	--	±100	nA
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250μA	1.0		2.5	V
Drain-Source On-Resistance	R _{DS(on)}	V _{GS} = 10V, I _D = 4.3A	--		28	mΩ
		V _{GS} = 4.5V, I _D = 3.9A	--		31	
Forward Transconductance	g _{FS}	V _{DS} =5V,I _D =4.3A	--	9.6	--	S
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{GS} = 0V, V _{DS} = 30V, f = 1.0MHz	--	1336	--	pF
Output Capacitance	C _{oss}		--	56	--	
Reverse Transfer Capacitance	C _{rss}		--	52	--	
Total Gate Charge	Q _g	V _{DS} = 30V, I _D = 5A, V _{GS} = 10V	--	22	--	nC
Gate-Source Charge	Q _{gs}		--	3.3	--	
Gate-Drain Charge	Q _{gd}		--	5.2	--	
Turn-on Delay Time	t _{d(on)}	V _{DD} = 30V, I _D = 5A, R _G = 3Ω	--	5.2	--	ns
Turn-on Rise Time	t _r		--	3	--	
Turn-off Delay Time	t _{d(off)}		--	17	--	
Turn-off Fall Time	t _f		--	2.5	--	
Drain-Source Body Diode Characteristics						
Body Diode Voltage	V _{SD}	T _J = 25°C, I _{SD} = 1.7A, V _{GS} = 0V	--	--	1.2	V
Continuous Body Diode Current	I _S	T _C = 25°C	--	--	5	A

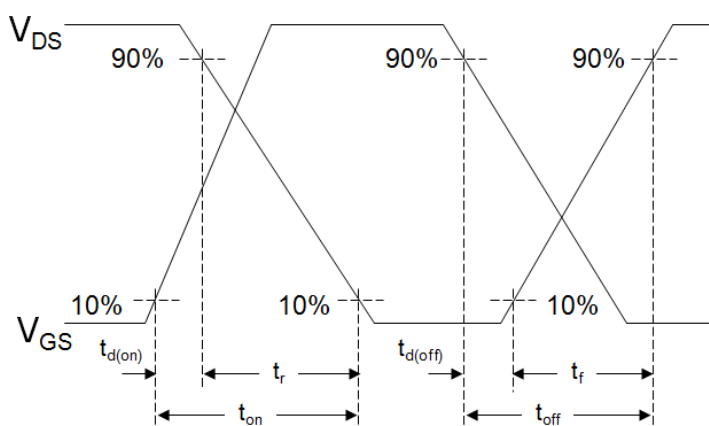
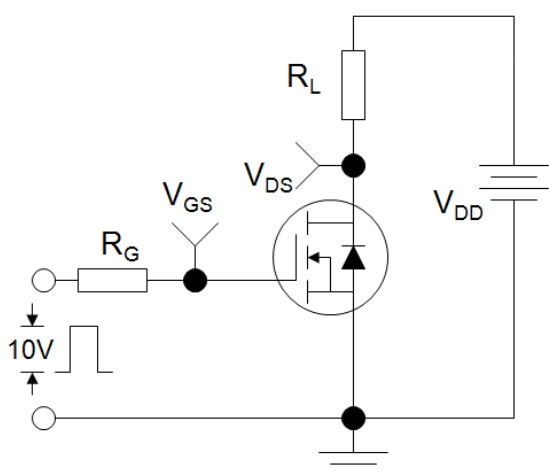
Notes

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. Identical low side and high side switch with identical R_G

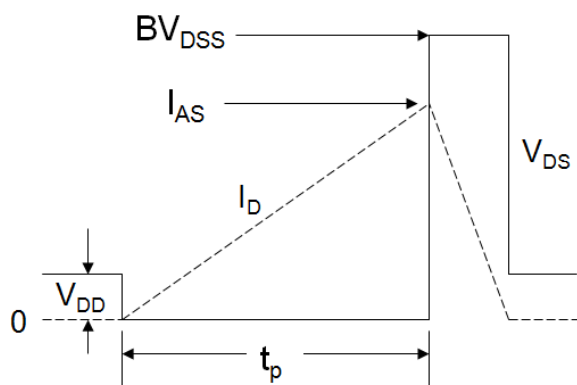
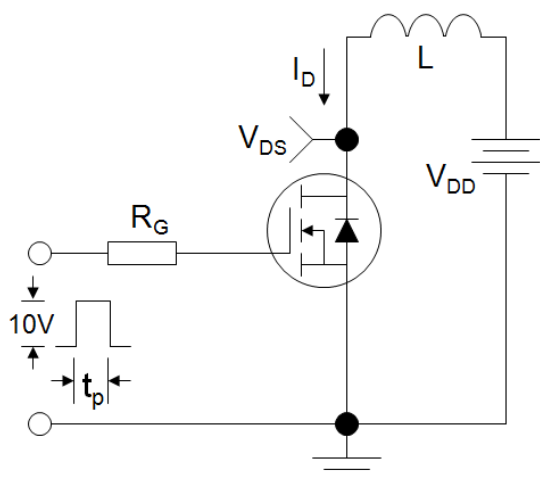
Gate Charge Test Circuit



Switch Time Test Circuit



EAS Test Circuit



NMOS Typical Characteristics $T_J = 25^\circ\text{C}$, unless otherwise noted

Figure 1. Output Characteristics

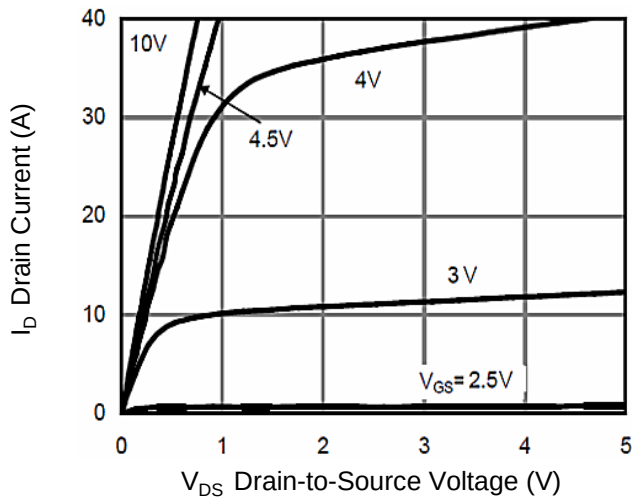


Figure 2. Transfer Characteristics

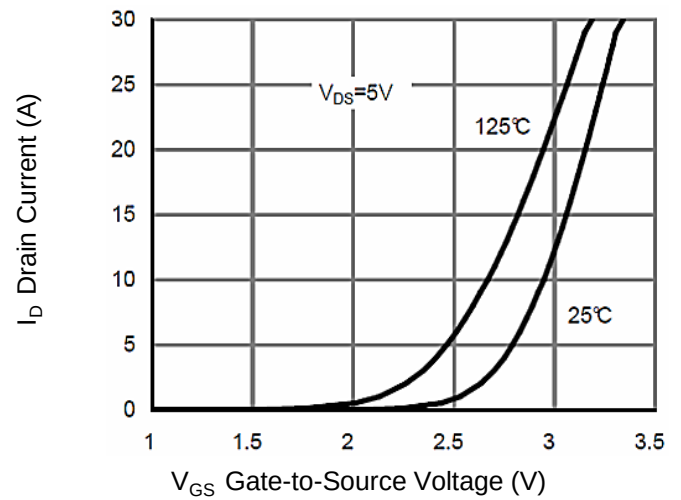


Figure 3. Drain-Source On-Resistance

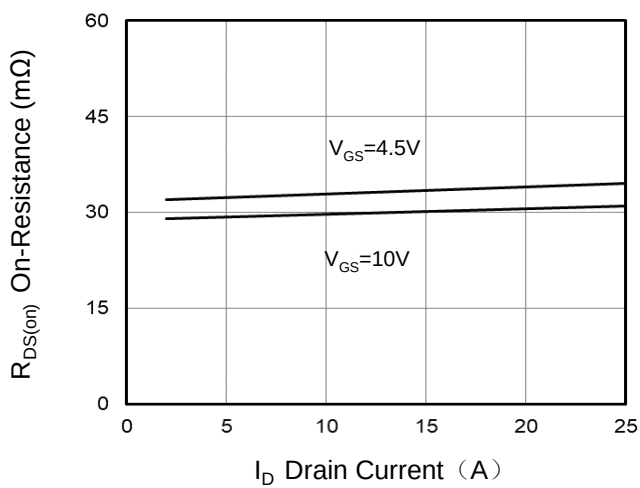


Figure 4. Gate Charge

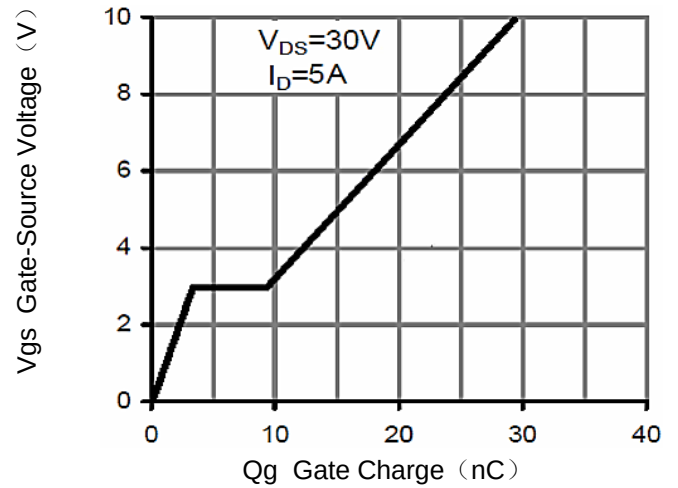


Figure 5. Capacitance

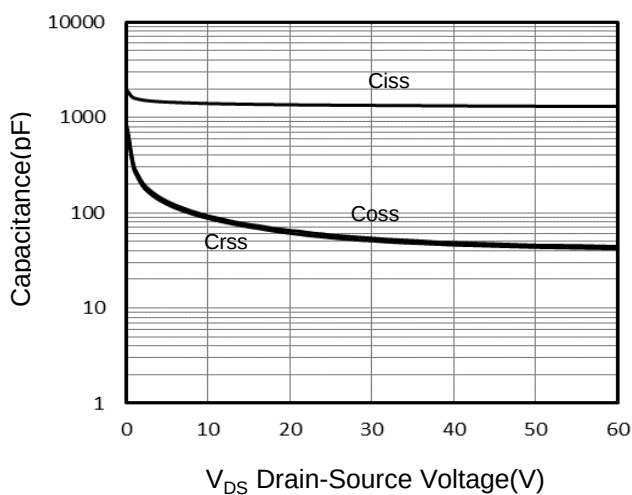
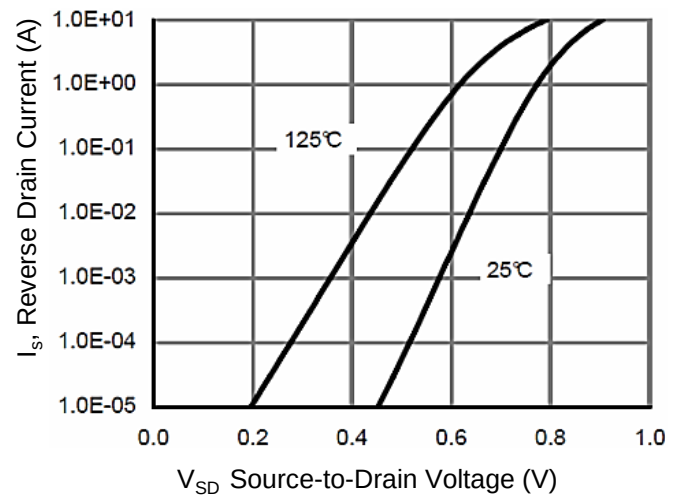


Figure 6. Source-Drain Diode Forward



NMOS Typical Characteristics $T_J = 25^\circ\text{C}$, unless otherwise noted

Figure 7. Drain-Source On-Resistance

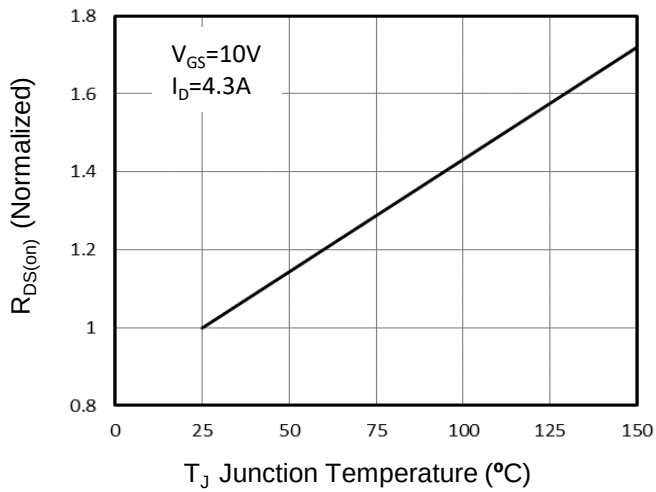


Figure 8. Safe Operation Area

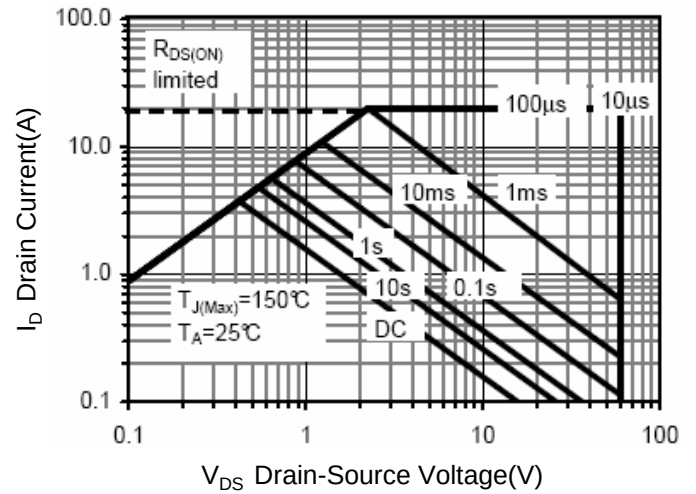
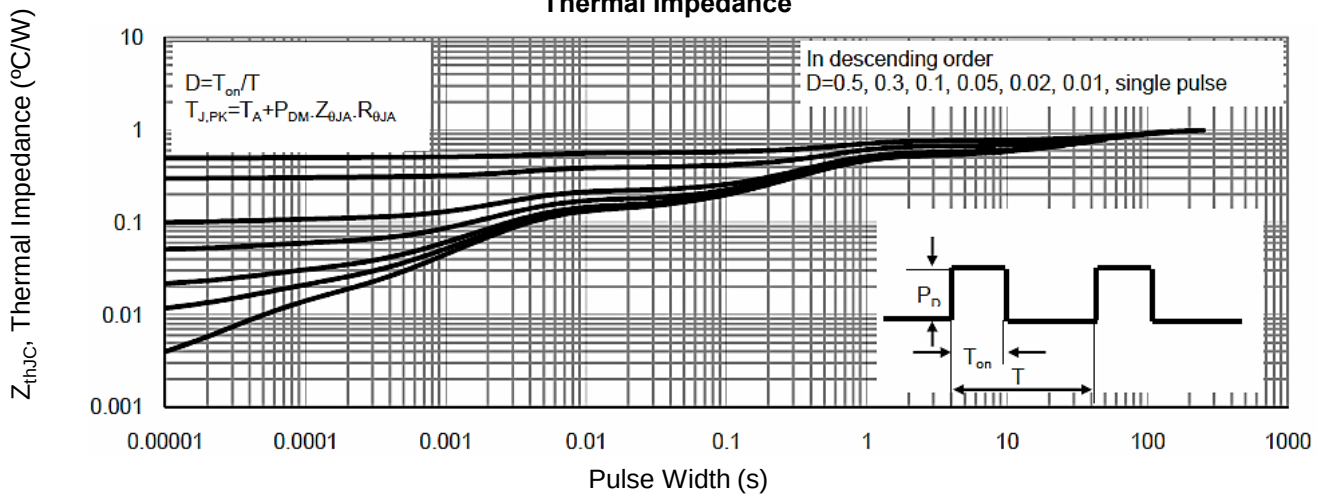


Figure 9. Normalized Maximum Transient Thermal Impedance



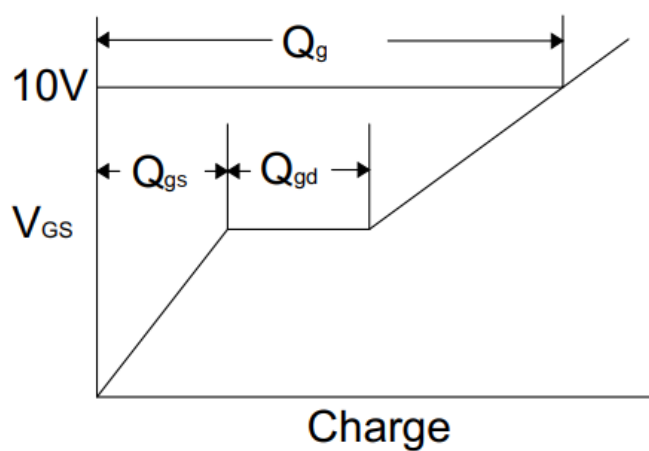
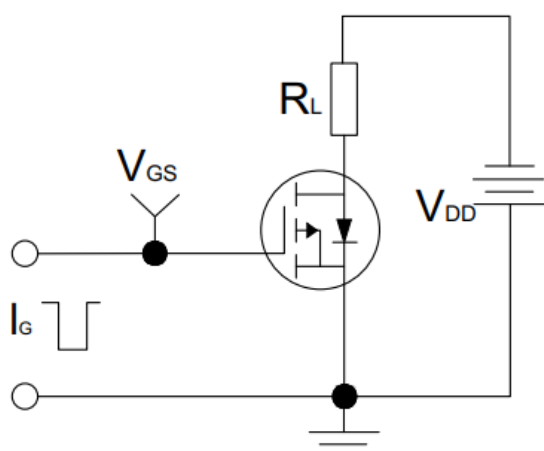
PMOS Specifications $T_J = 25^\circ\text{C}$, unless otherwise noted

Parameter	Symbol	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
Static Parameters						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0V, I _D = -250μA	-60	--	--	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -60V, V _{GS} = 0V, T _J = 25°C	--	--	-1	μA
Gate-Source Leakage	I _{GSS}	V _{GS} = ±20V	--	--	±100	nA
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250μA	-1.0		-2.5	V
Drain-Source On-Resistance	R _{DS(on)}	V _{GS} = -10V, I _D = -3.1A	--		62	mΩ
		V _{GS} = -4.5V, I _D = -0.2A	--		72	
Forward Transconductance	g _{FS}	V _{DS} =-5V,I _D =-3.1A	--	6.6	--	S
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{GS} = 0V, V _{DS} = -30V, f = 1.0MHz	--	1454	--	pF
Output Capacitance	C _{oss}		--	62	--	
Reverse Transfer Capacitance	C _{rss}		--	58	--	
Total Gate Charge	Q _g	V _{DD} = -30V, I _D = -3A, V _{GS} = -10V	--	37	--	nC
Gate-Source Charge	Q _{gs}		--	4.5	--	
Gate-Drain Charge	Q _{gd}		--	10.5	--	
Turn-on Delay Time	t _{d(on)}	V _{DD} = -30V, I _D = -3A, R _G = 3Ω	--	8	--	ns
Turn-on Rise Time	t _r		--	4	--	
Turn-off Delay Time	t _{d(off)}		--	32	--	
Turn-off Fall Time	t _f		--	7	--	
Drain-Source Body Diode Characteristics						
Continuous Body Diode Current	I _S	T _C = 25°C	--	--	-3.1	A
Body Diode Voltage	V _{SD}	T _J = 25°C, I _{SD} = -2A, V _{GS} = 0V	--	--	-1.2	V

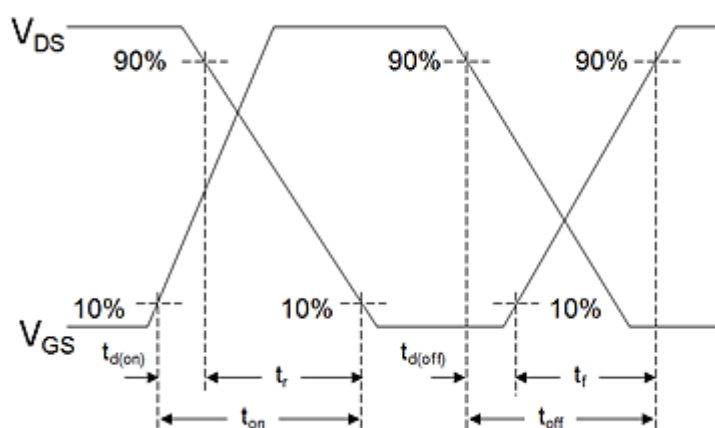
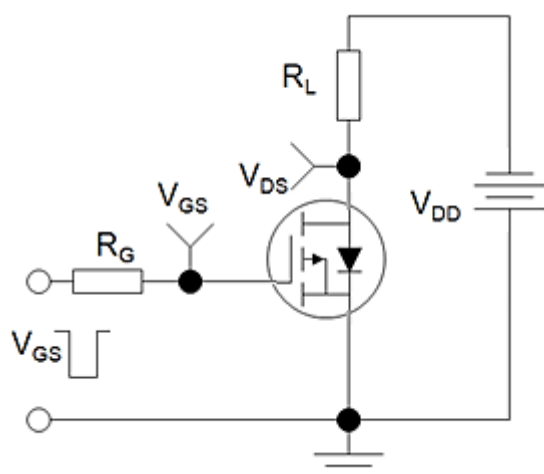
Notes

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. Identical low side and high side switch with identical R_G

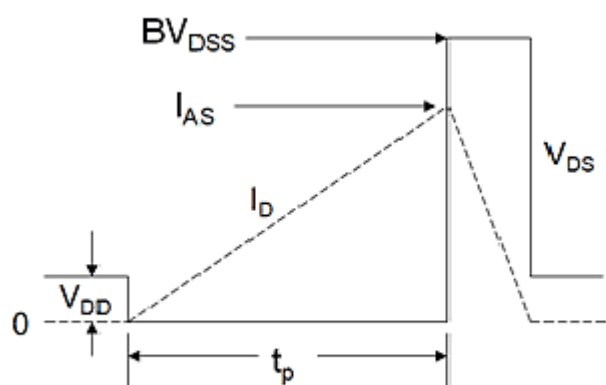
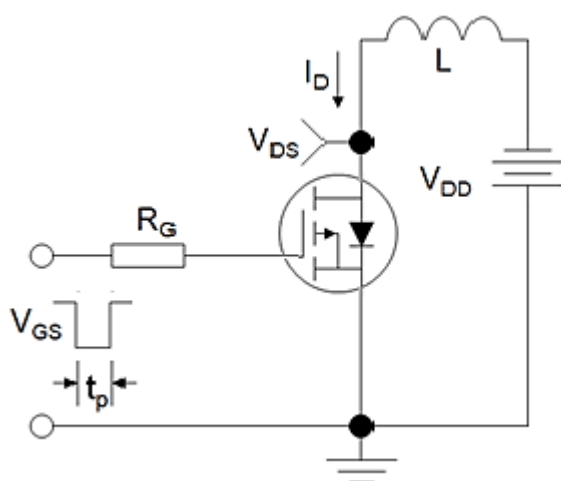
Gate Charge Test Circuit



Switch Time Test Circuit



EAS Test Circuit



PMOS Typical Characteristics $T_j = 25^\circ\text{C}$, unless otherwise noted

Figure 1. Output Characteristics

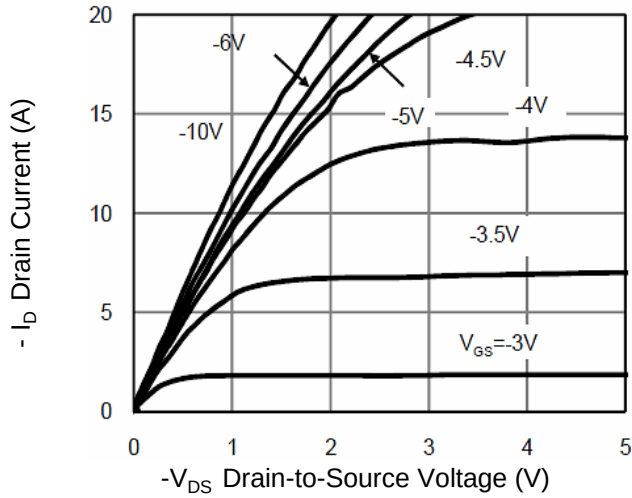


Figure 2. Transfer Characteristics

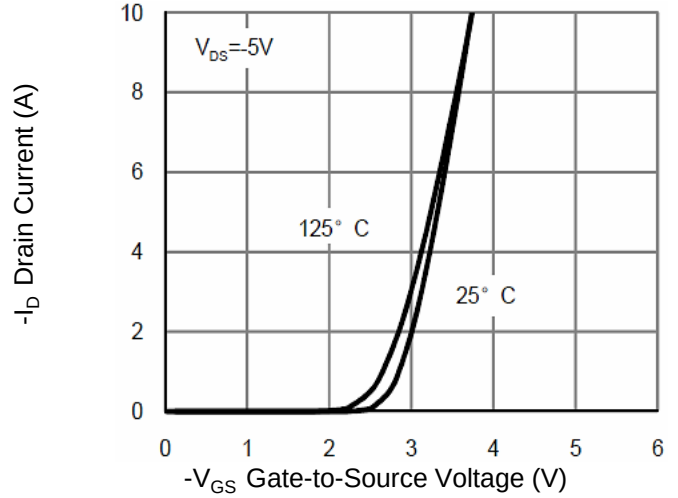


Figure 3. $R_{DS(on)}$ -Drain Current

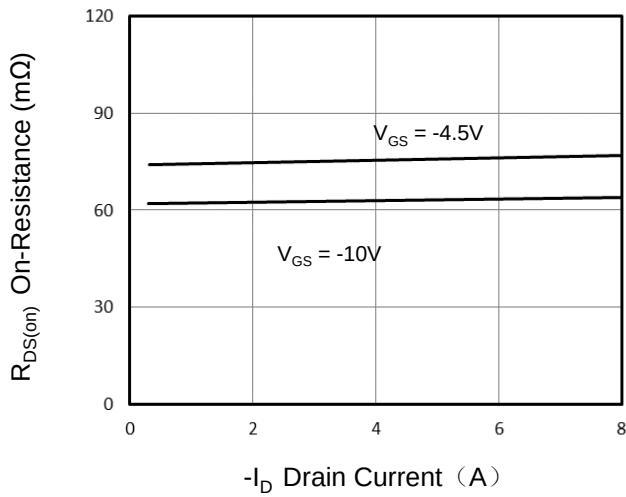


Figure 4. Gate Charge

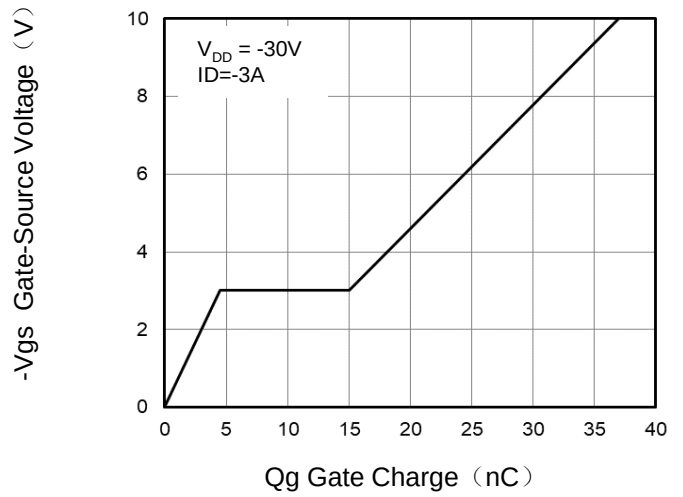


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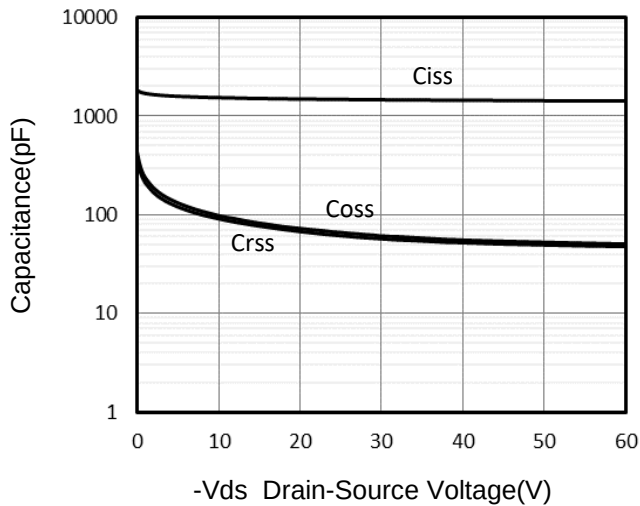
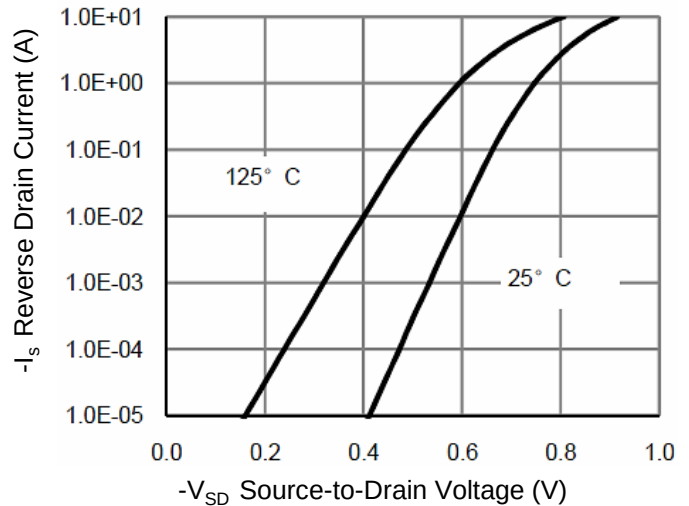


Figure 6. Source-Drain Diode Forward



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Figure 7. Drain-Source On-Resistance

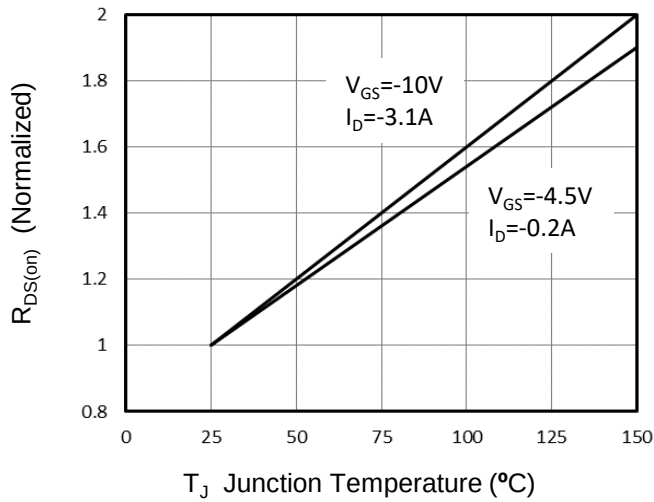


Figure 8. Safe Operation Area

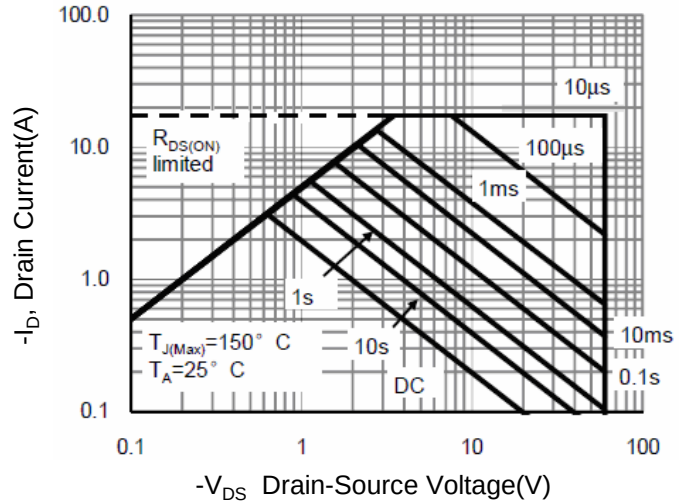


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