80V N-Channel Enhancement Mode MOSFET

Description

The SX100N08CMP is silicon N-channel Enhanced VDMOSFET, is obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency.

General Features

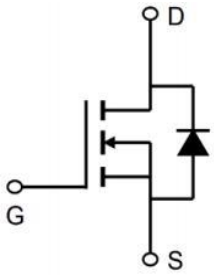
V_{DS} = 80V I_D =100A

$R_{DS(ON)}$ < 15mΩ @ V_{GS}=10V

Application

Uninterruptible Power Supply(UPS)

Power Factor Correction (PFC)



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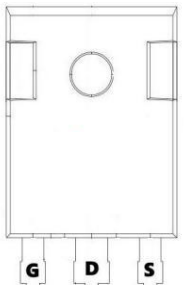


Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Symbol	Parameter	Rating	Units
VDS	Drain-Source Voltage	80	V
VGS	Gate-Source Voltage	±20	V
ID@TC=25℃	Continuous Drain Current, VGS @ 10V	100	A
ID@TC=100℃	Continuous Drain Current, VGS @ 10V	70	A
IDM	Pulsed Drain Current	480	A
EAS	Single Pulse Avalanche Energy	1054	mJ
IAS	Avalanche Current	60	A
PD@TC=25℃	Total Power Dissipation4	300	W
TSTG	Storage Temperature Range	-55 to 175	℃
TJ	Operating Junction Temperature Range	-55 to 175	℃
RθJA	Thermal Resistance Junction-Ambient	0.50	℃/W
RθJC	Thermal Resistance Junction-Case	40	℃/W

Electrical Characteristics (T_J=25℃, unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V(BR)DSS	Drain-Source Breakdown Voltage	V_{GS}=0; I_D= 10mA	80	-	-	V
VGS(TH)	Gate Threshold Voltage	VDS= VGS, ID= 1mA	1.2	1.7	2.0	V
RDS(ON)	Drain-Source On-stage Resistance	V_{GS}= 4V; I_D=30A	-	13	15	mΩ
		V_{GS}= 10V; I_D=30A	-	-	11	mΩ
IGSS	Gate Source Leakage Current	V_{GS}= ±20V; V_{DS}= 0	-	-	±10	uA
IDSS	Zero Gate Voltage Drain Current	VDS= 80V, VGS= 0V, TJ= 25ºC	-	-	100	μA
Ciss	Input Capacitance	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz	-	3795	-	pF
Coss	Output Capacitance		-	1456	-	
Crss	Reverse Transfer Capacitance		-	1101	-	
R_G	Gate resistance	f = 1.0MHz open drain	-	0.75	-	Ω
Q_g	Total Gate Charge	V_{DD} = 64V, I_D = 100A, V_{GS} =10V	-	338	-	nC
Qgs	Gate-Source Charge		-	12	-	
Qgd	Gate-Drain Charge		-	175	-	
td(on)	Turn-on Delay Time	V_{DD} = 40V, I_D = 100A, R_G = 25Ω	-	45	-	ns
t_r	Turn-on Rise Time		-	178	-	
td(off)	Turn-off Delay Time		-	1062	-	
t_f	Turn-off Fall Time		-	830	-	
ISD	Continuous Source Current	T_C = 25 ºC	-	-	100	A
ISM	Pulsed Source Current		-	-	400	
VSD	Diode Forward Voltage	I_S=60A; V_{GS}=0V	-	-	1.7	V
trr	Reverse Recovery Time	V_{DD} = 40V,IF = 30A, diF/dt =100A /μs	-	210	-	ns
Q_{rr}	Reverse Recovery Charge		-	1.5	-	uC

Note：

1、The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.

2、The data tested by pulsed，pulse width .The EAS data shows Max. rating .

3、The test cond ≦ 300us duty cycle ≦ 2%, duty cycle ition is V_{DD}=25V$_{GS}$=10V,L=0.4mH,I_{AS}=60A

4、The power dissipation is limited by 175℃junction temperature

5、The data is theoretically the same as ID and IDM，in real applications，should be limited by total power dissipation.

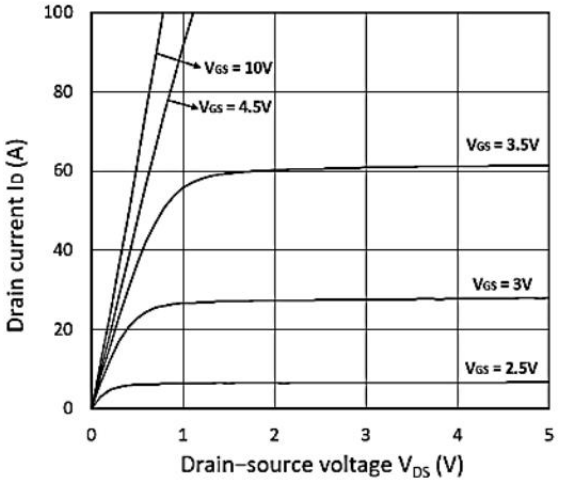


Figure 1. Output Characteristics

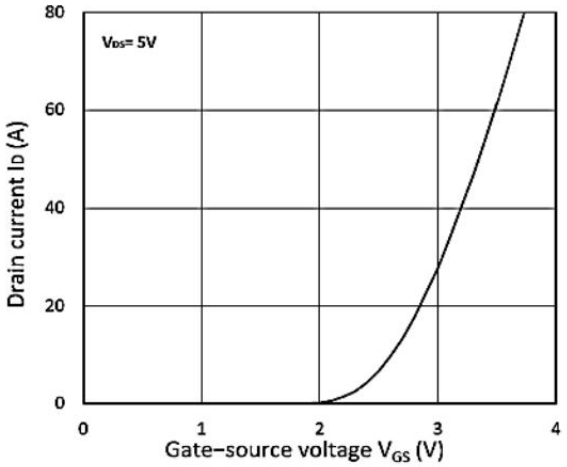


Figure 2. Transfer Characteristics

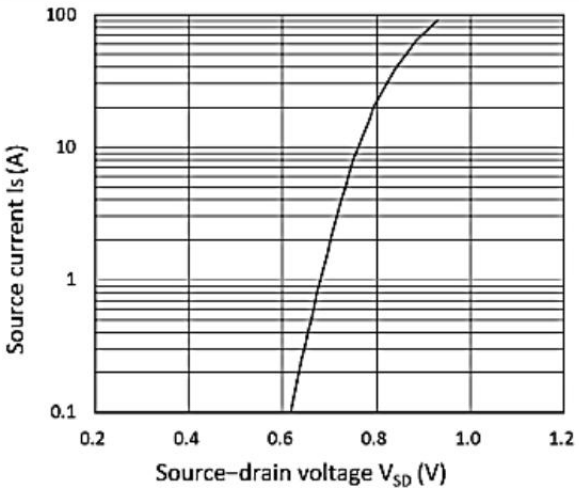


Figure 3. Forward Characteristics of Reverse

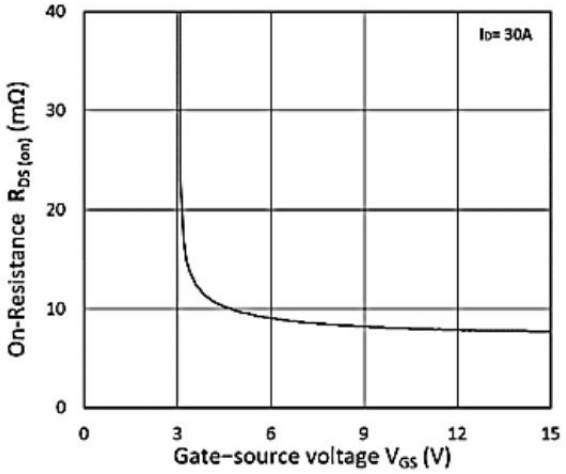


Figure 4. RDS(ON) vs. VGS

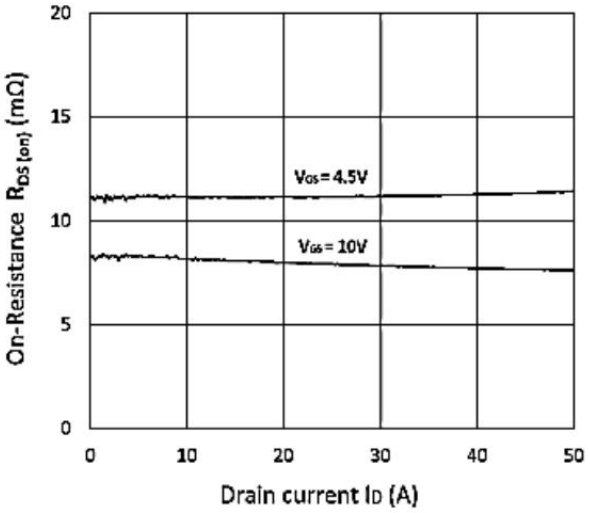


Figure 5. RDS(ON) vs. ID

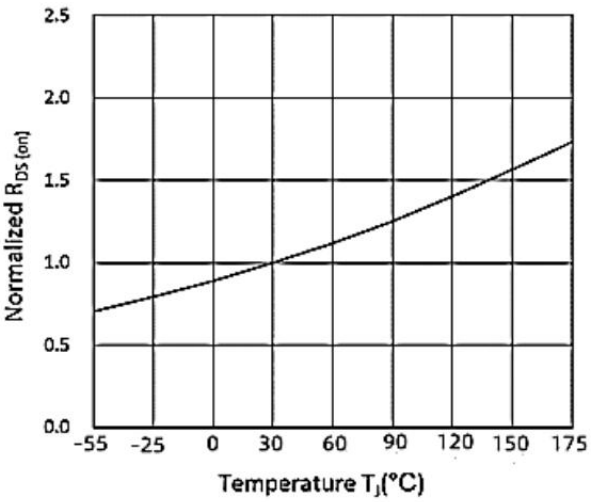


Figure 6. Normalized RDS(on) vs. Temperature

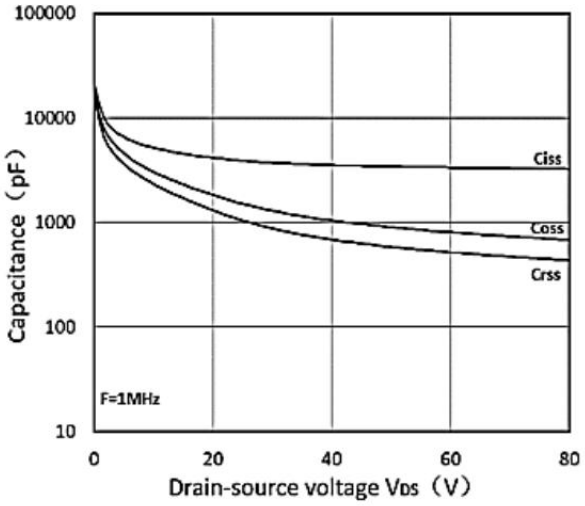


Figure 7. Capacitance Characteristics

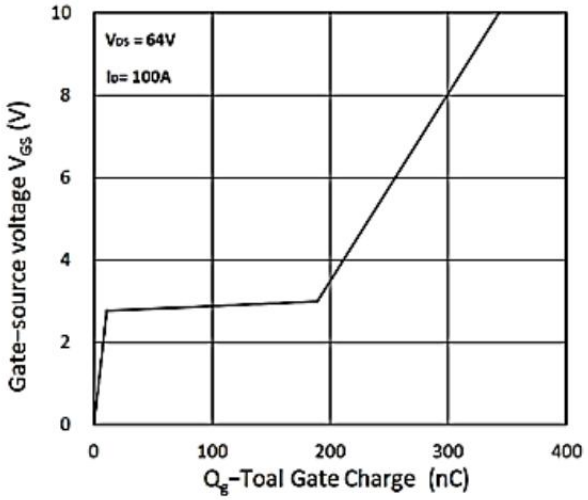


Figure 8. Gate Charge Characteristics

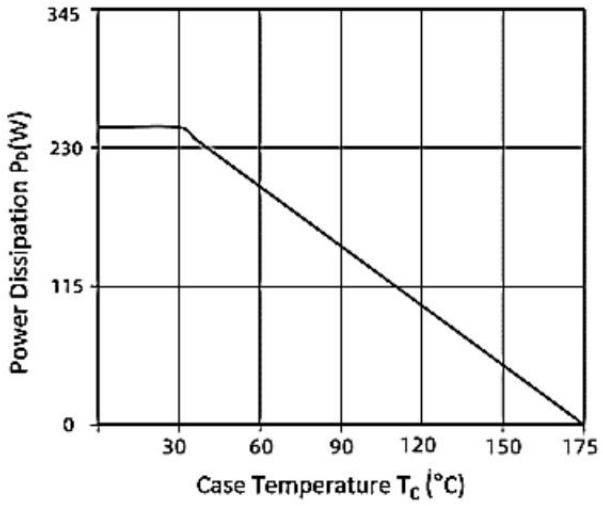


Figure 9. Power Dissipation

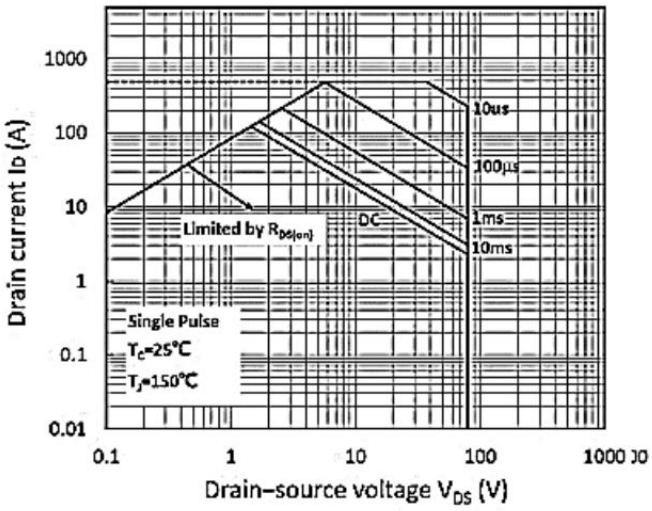


Figure10. Safe Operating Area

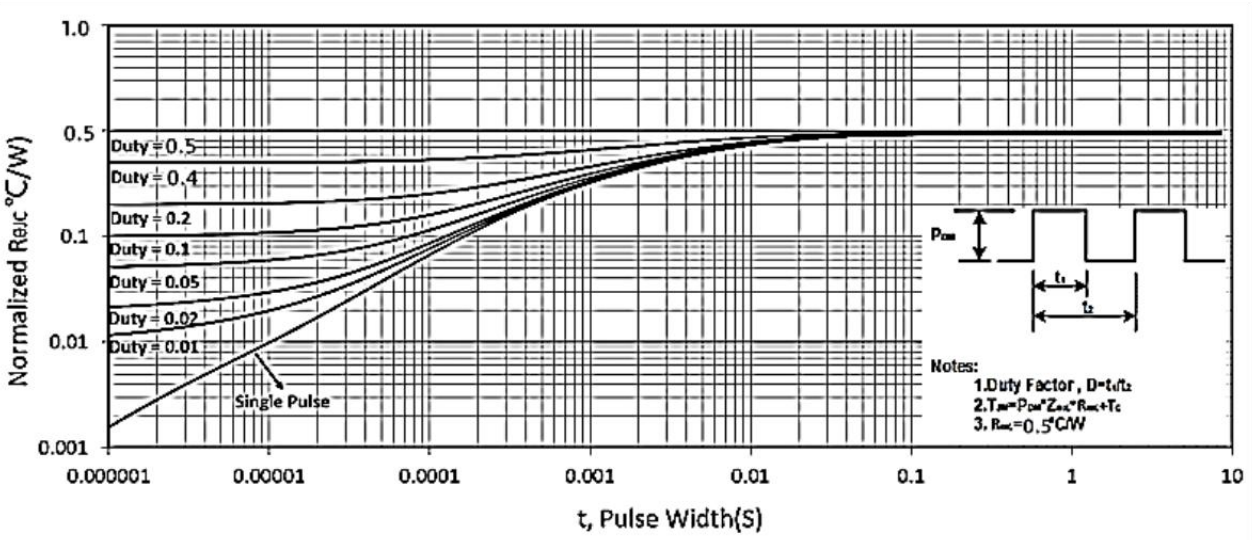
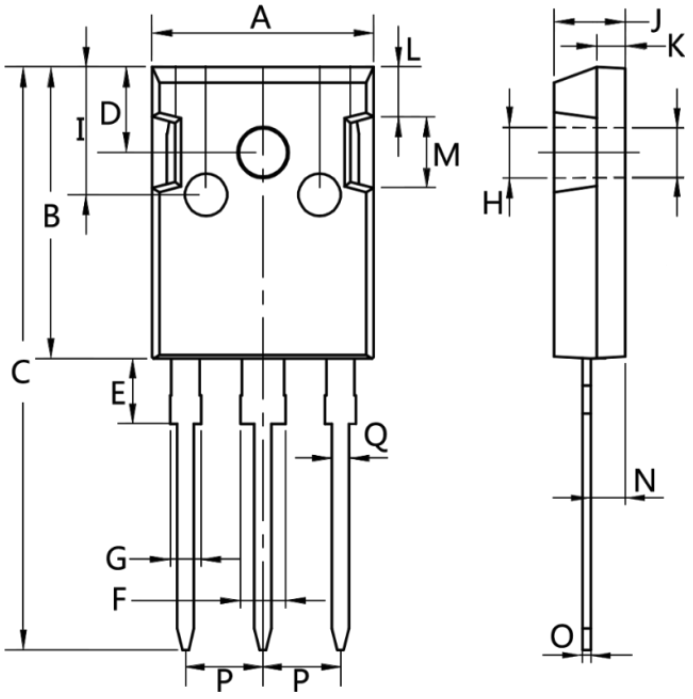


Figure 11. Normalized Maximum Transient Thermal Impedance

Package Mechanical Data-TO-247-3L



Symbol	Dim in mm	
	Min	Max
A	15.0	16.0
B	20.0	21.0
C	41.0	42.0
D	5.0	6.0
E	4.0	5.0
F	2.5	3.5
G	1.75	2.5
H	3.0	3.5
I	8.0	10.0
J	4.9	5.1
K	1.9	2.1
L	3.5	4.0
M	4.75	5.25
N	2.0	3.0
O	0.55	0.75
P	Typ 5.08	
Q	1.2	1.3

Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
TAPING	TO-247-3L		330