



Description

The IRF7420TRPBF uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 2.5V. This device is suitable for use as a Battery protection or in other Switching application.

General Features

$V_{DS} = -20V$ $I_D = -20A$

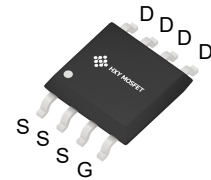
$R_{DS(ON)} < 19m\Omega @ V_{GS}=10V$

Application

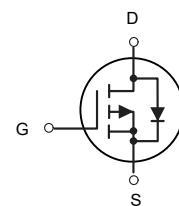
Battery protection

Load switch

Uninterruptible power supply



SOP-8
(SOIC-8)



P-Channel MOSFET

Package Marking and Ordering Information

Product ID	Pack	Brand	Qty(PCS)
IRF7420TRPBF	SOP-8(SOIC-8)	HXY MOSFET	3000

Absolute Maximum Ratings($T_c=25^\circ C$ unless otherwise noted)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	-20	V
V_{GS}	Gate-Source Voltage	± 12	V
$I_D @ T_A=25^\circ C$	Drain Current ³ , $V_{GS} @ 10V$	-20	A
$I_D @ T_A=70^\circ C$	Drain Current ³ , $V_{GS} @ 10V$	-16	A
I_{DM}	Pulsed Drain Current ¹	-68	A
$P_D @ T_A=25^\circ C$	Total Power Dissipation	18	W
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ C$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ C$
R_{thj-a}	Maximum Thermal Resistance, Junction-ambient ³	75	$^\circ C/W$



Electrical Characteristics (T_J=25°C, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =-250uA	-20	---	---	V
ΔBV _{DSS} /ΔT _J	BV _{DSS} Temperature Coefficient	Reference to 25°C, I _D =-1mA	---	-0.012	---	V/°C
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =-4.5V, I _D =-10A	---	15	19	mΩ
		V _{GS} =-2.5V, I _D =-8A	---	19	23	
V _{GS(th)}	Gate Threshold Voltage	V _{GS} =V _{DS} , I _D =-250uA	-0.4	-0.7	-1.0	V
ΔV _{GS(th)}	V _{GS(th)} Temperature Coefficient		---	2.94	---	mV/°C
I _{DSS}	Drain-Source Leakage Current	V _{DS} =-15V, V _{GS} =0V, T _J =25°C	---	---	1	uA
I _{GSS}	Gate-Source Leakage Current	V _{GS} =±12V, V _{DS} =0V	---	---	±100	nA
g _{fs}	Forward Transconductance	V _{DS} =-5V, I _D =-10A	---	43	---	S
Q _g	Total Gate Charge (-4.5V)		---	35	---	nC
Q _{gs}	Gate-Source Charge	V _{DS} =-10V, V _{GS} =-4.5V, I _D =-10A	---	5.0	---	
Q _{gd}	Gate-Drain Charge		---	10	---	
T _{d(on)}	Turn-On Delay Time		---	12.0	---	ns
T _r	Rise Time	V _{DD} =-10V, V _{GS} =-4.5V,	---	40.0	---	
T _{d(off)}	Turn-Off Delay Time	R _G =3.3Ω, I _D =-10A	---	30	---	
T _f	Fall Time		---	10	---	
C _{iss}	Input Capacitance		---	2800	---	pF
C _{oss}	Output Capacitance	V _{DS} =-15V, V _{GS} =0V, f=1MHz	---	690	---	
C _{rss}	Reverse Transfer Capacitance		---	590	---	
I _S	Continuous Source Current ^{1,4}	V _G =V _D =0V, Force Current	---	---	-20.0	A
I _{SM}	Pulsed Source Current ^{2,4}		---	---	---	A
V _{SD}	Diode Forward Voltage ²	V _{GS} =0V, I _S =-1A, T _J =25°C	---	---	-1.2	V
t _{rr}	Reverse Recovery Time	I _F =-10A, dI/dt=100A/μs,	---	27	---	nS
Q _{rr}	Reverse Recovery Charge	T _J =25°C	---	17.8	---	nC

Note :

1.The data tested by surface mounted on a 1 inch² FR-4 board with 20Z copper.

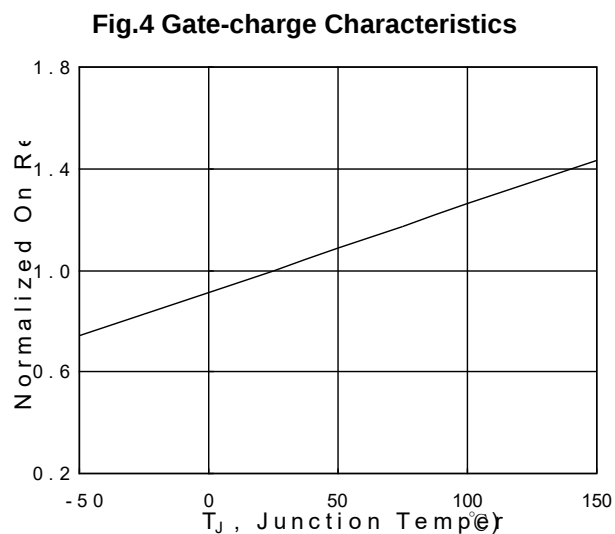
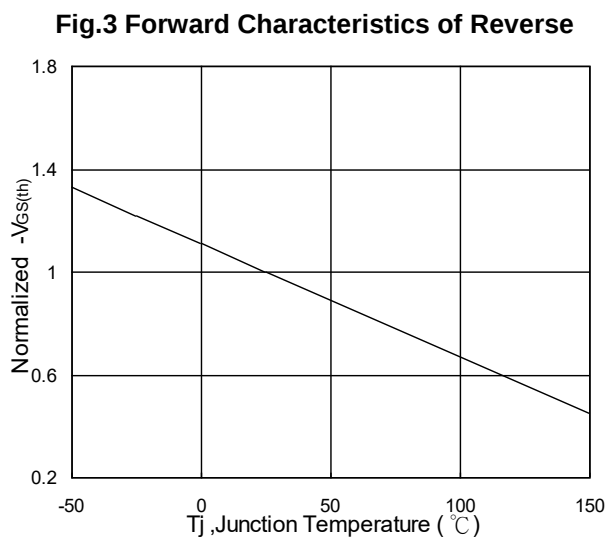
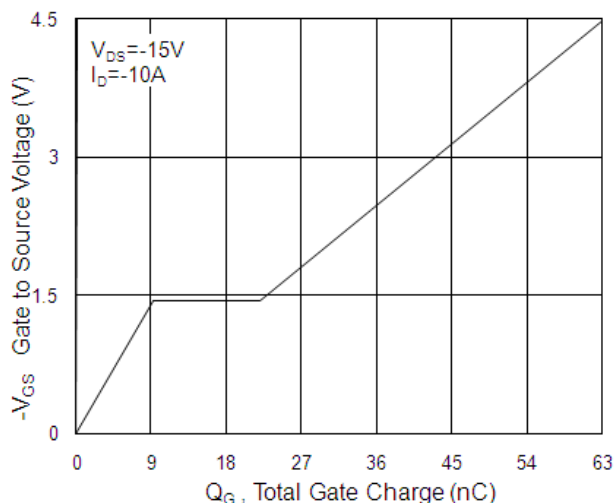
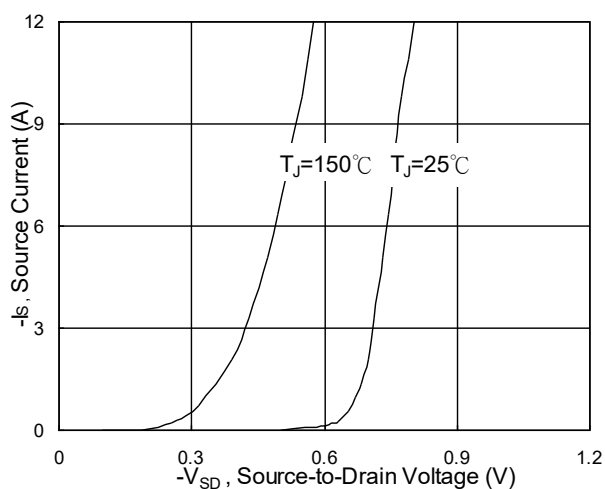
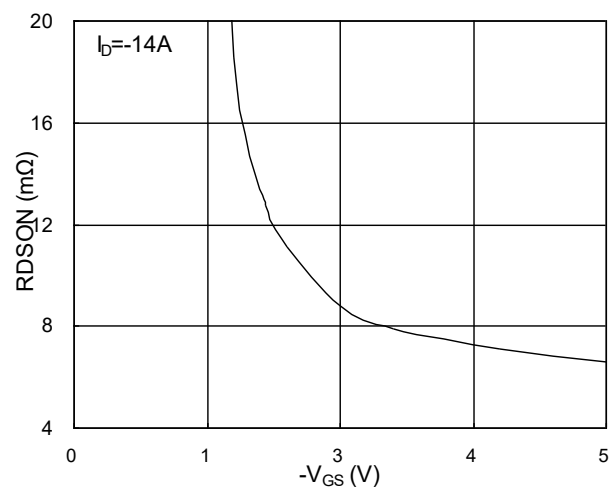
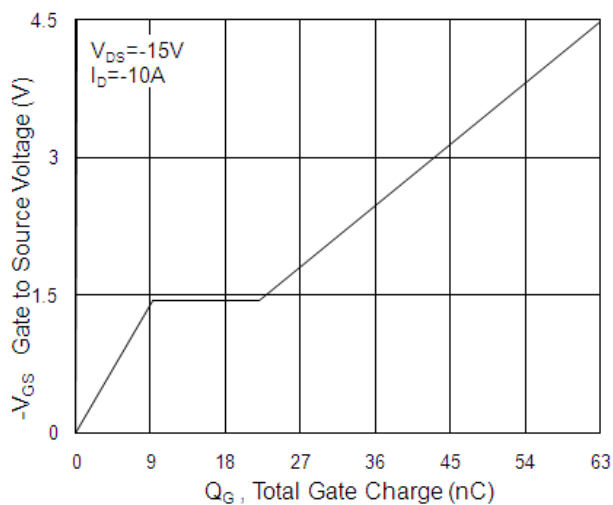
2.The data tested by pulsed, pulse width ≤ 300us, duty cycle ≤ 2%

3.The power dissipation is limited by 150°C junction temperature

4.The data is theoretically the same as I_D and I_{DM}, in real applications, should be limited by total power dissipation.



Typical Characteristics



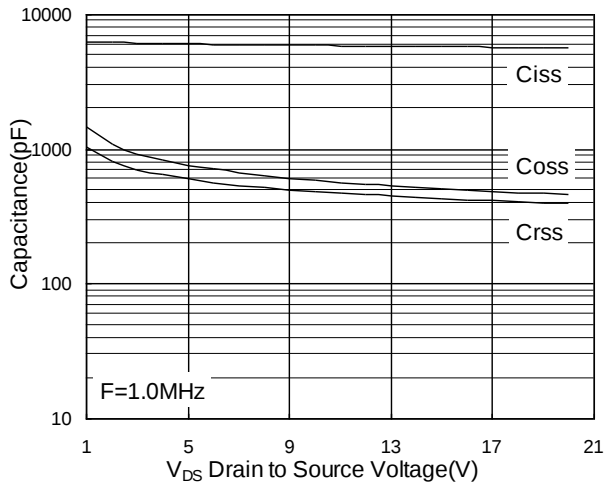


Fig.7 Capacitance

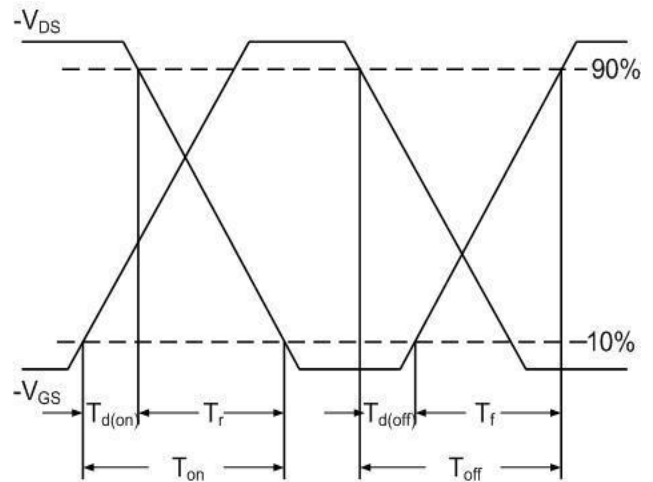


Fig.8 Safe Operating Area

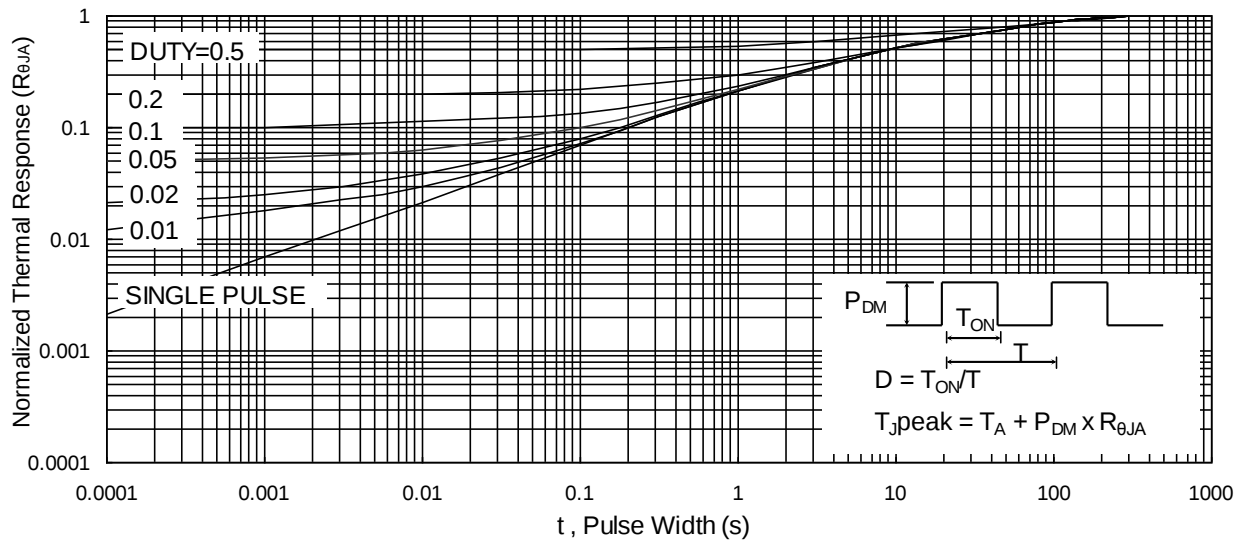


Fig.9 Normalized Maximum Transient Thermal Impedance

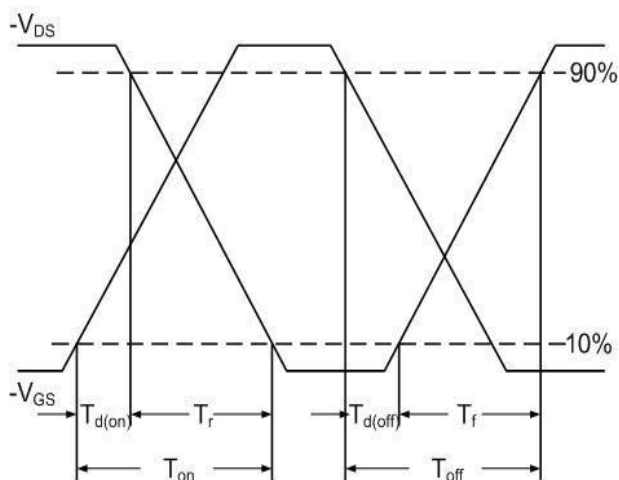


Fig.10 Switching Time Waveform

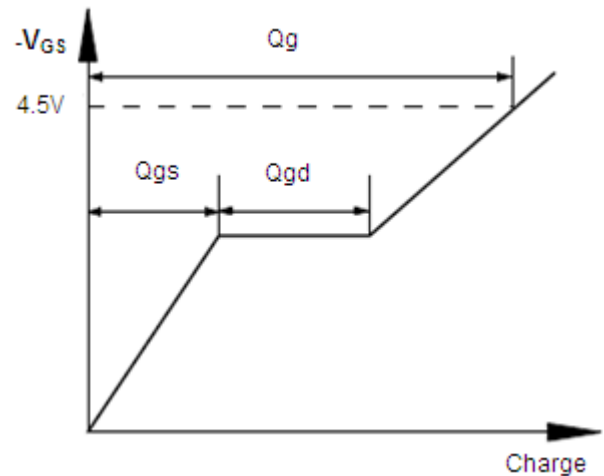
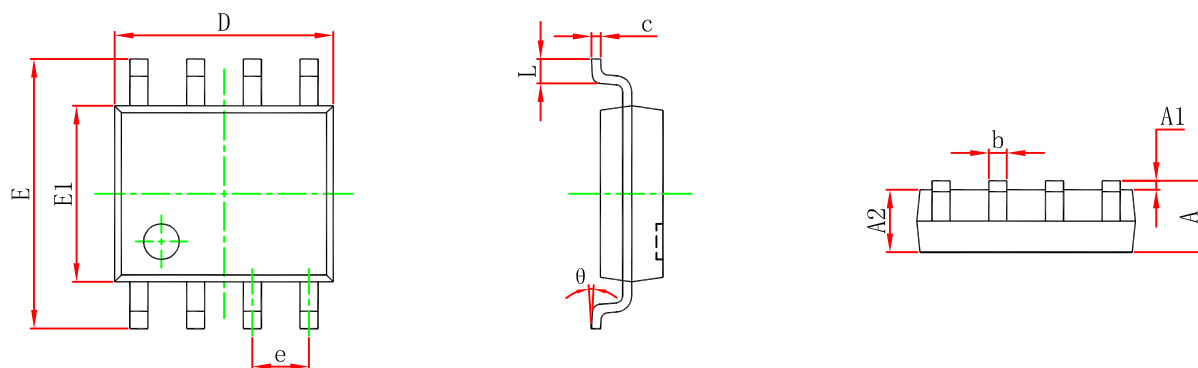


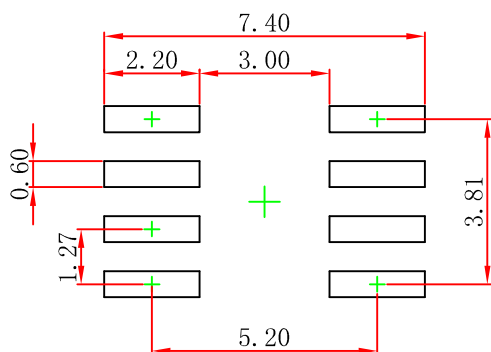
Fig.11 Gate Charge Waveform



SOP-8(SOIC-8) Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.800	5.000	0.189	0.197
e	1.270 (BSC)		0.050 (BSC)	
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°



Note:
1. Controlling dimension; in millimeters.
2. General tolerance: $\pm 0.05\text{mm}$.
3. The pad layout is for reference purposes only.



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