

OptiMOS™ -T2 Power-Transistor



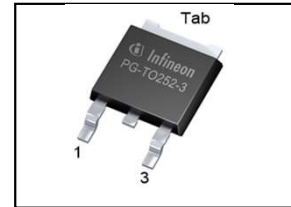
Features

- N-channel - Enhancement mode
- AEC Q101 qualified
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- RoHS compliant
- 100% Avalanche tested

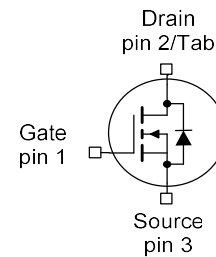
Product Summary

V_{DS}	80	V
$R_{DS(on),max}$	13.2	mΩ
I_D	50	A

PG-TO252-3-313



Type	Package	Marking
IPD50N08S4-13	PG-TO252-3-313	4N0813



Maximum ratings, at $T_j=25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current ¹⁾	I_D	$T_C=25\text{ °C}$, $V_{GS}=10\text{ V}$	50	A
		$T_C=100\text{ °C}$, $V_{GS}=10\text{ V}^{2)}$	50	
Pulsed drain current ²⁾	$I_{D,pulse}$	$T_C=25\text{ °C}$	200	
Avalanche energy, single pulse ²⁾	E_{AS}	$I_D=25\text{ A}$	76	mJ
Avalanche current, single pulse	I_{AS}	-	31	A
Gate source voltage	V_{GS}	-	±20	V
Power dissipation	P_{tot}	$T_C=25\text{ °C}$	72	W
Operating and storage temperature	T_j, T_{stg}	-	-55 ... +175	°C

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Thermal characteristics²⁾

Thermal resistance, junction - case	R_{thJC}	-	-	-	2.1	K/W
SMD version, device on PCB	R_{thJA}	minimal footprint	-	-	62	
		6 cm ² cooling area ³⁾	-	-	40	

Electrical characteristics, at $T_j=25^\circ\text{C}$, unless otherwise specified

Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=1mA$	80	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=33\mu A$	2.0	3.0	4.0	
Zero gate voltage drain current	I_{DSS}	$V_{DS}=80V, V_{GS}=0V, T_j=25^\circ\text{C}$	-	0.01	1	μA
		$V_{DS}=80V, V_{GS}=0V, T_j=125^\circ\text{C}^{2)}$	-	5	100	
Gate-source leakage current	I_{GSS}	$V_{GS}=20V, V_{DS}=0V$	-	-	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=50A$	-	11.2	13.2	m Ω

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Dynamic characteristics²⁾

Input capacitance	C_{iss}	$V_{GS}=0V, V_{DS}=25V,$ $f=1MHz$	-	1316	1711	pF
Output capacitance	C_{oss}		-	511	664	
Reverse transfer capacitance	C_{rss}		-	29	58	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=40V, V_{GS}=10V,$ $I_D=50A, R_G=3.5\Omega$	-	5.0	-	ns
Rise time	t_r		-	3.6	-	
Turn-off delay time	$t_{d(off)}$		-	6.4	-	
Fall time	t_f		-	11.8	-	

Gate Charge Characteristics²⁾

Gate to source charge	Q_{gs}	$V_{DD}=64V, I_D=50A,$ $V_{GS}=0 \text{ to } 10V$	-	6.9	9.0	nC
Gate to drain charge	Q_{gd}		-	4.5	9	
Gate charge total	Q_g		-	19	30	
Gate plateau voltage	$V_{plateau}$		-	5.0	-	V

Reverse Diode

Diode continuous forward current ²⁾	I_S	$T_C=25^\circ C$	-	-	50	A
Diode pulse current ²⁾	$I_{S,pulse}$		-	-	200	
Diode forward voltage	V_{SD}	$V_{GS}=0V, I_F=50A,$ $T_j=25^\circ C$	-	0.9	1.3	V
Reverse recovery time ²⁾	t_{rr}	$V_R=50V, I_F=I_S,$ $di_F/dt=100A/\mu s$	-	74	-	ns
Reverse recovery charge ²⁾	Q_{rr}		-	49	-	nC

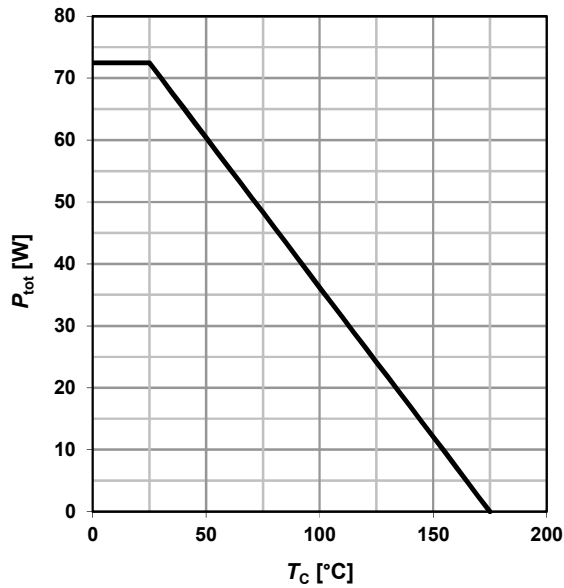
¹⁾ Current is limited by bondwire; with an $R_{thJC} = 2.1K/W$ the chip is able to carry 85A at 25°C.

²⁾ Specified by design. Not subject to production test.

³⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

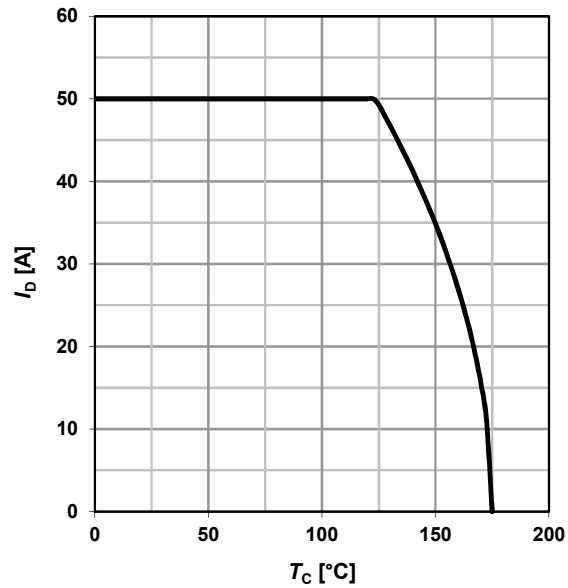
1 Power dissipation

$$P_{\text{tot}} = f(T_C); V_{\text{GS}} \geq 6 \text{ V}$$



2 Drain current

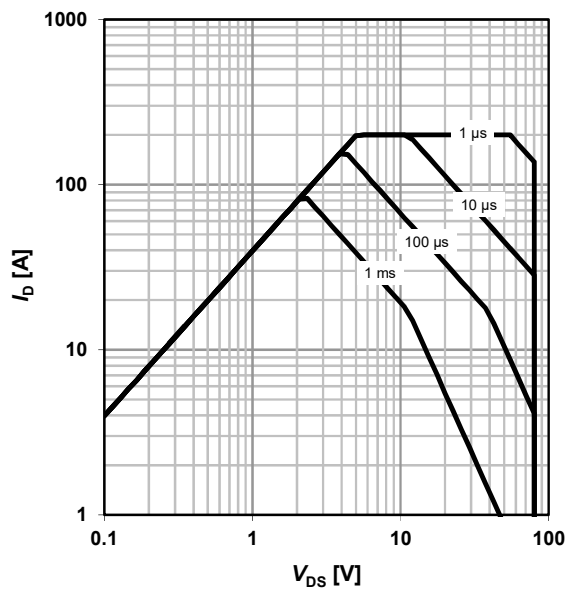
$$I_D = f(T_C); V_{\text{GS}} = 10 \text{ V}$$



3 Safe operating area

$$I_D = f(V_{\text{DS}}); T_C = 25^{\circ}\text{C}; D = 0$$

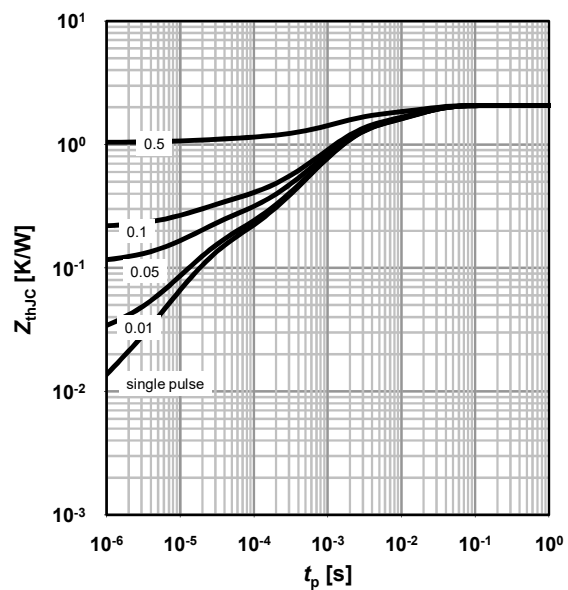
parameter: t_p



4 Max. transient thermal impedance

$$Z_{\text{thJC}} = f(t_p)$$

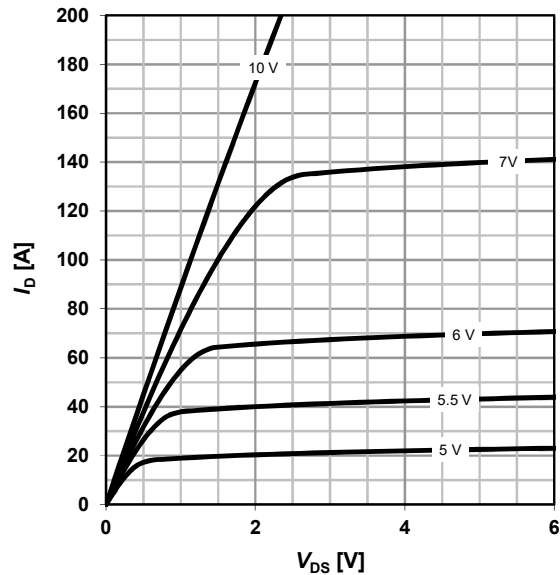
parameter: $D = t_p/T$



5 Typ. output characteristics

$$I_D = f(V_{DS}); T_J = 25^\circ\text{C}$$

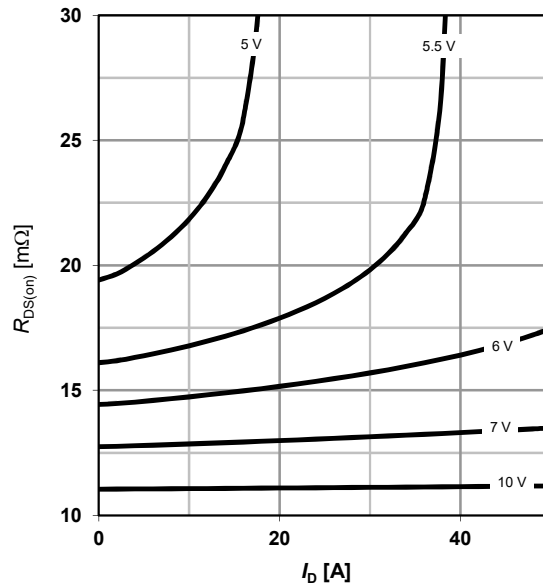
parameter: V_{GS}



6 Typ. drain-source on-state resistance

$$R_{DS(on)} = f(I_D); T_J = 25^\circ\text{C}$$

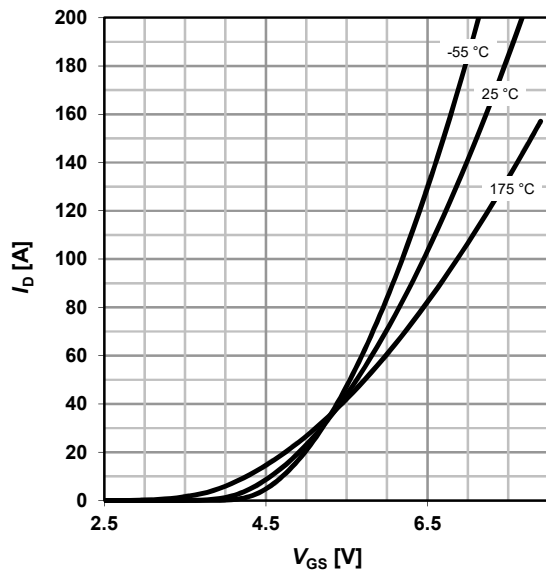
parameter: V_{GS}



7 Typ. transfer characteristics

$$I_D = f(V_{GS}); V_{DS} = 6\text{ V}$$

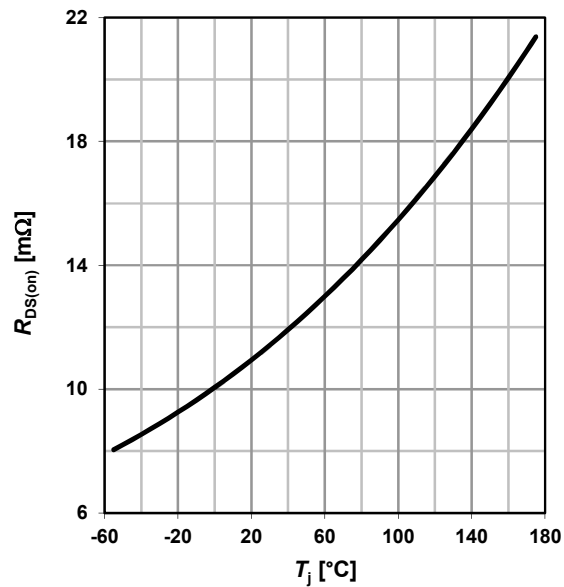
parameter: T_J



8 Typ. drain-source on-state resistance

$$R_{DS(on)} = f(T_J); I_D = 50\text{ A}; V_{GS} = 10\text{ V}$$

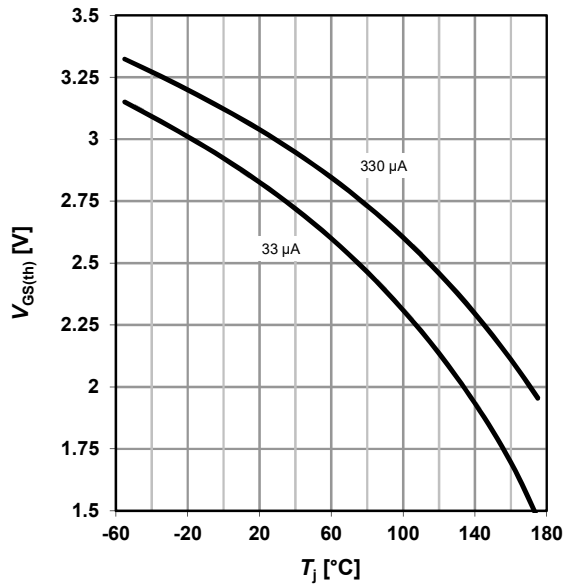
$\alpha = 0.4$



9 Typ. gate threshold voltage

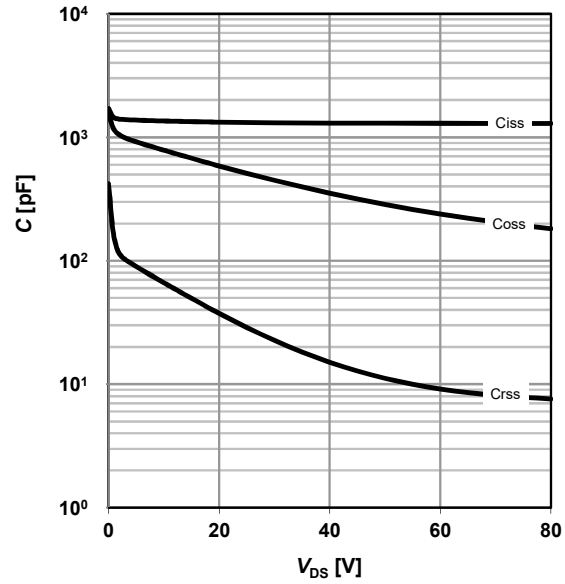
$$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$$

parameter: I_D



10 Typ. capacitances

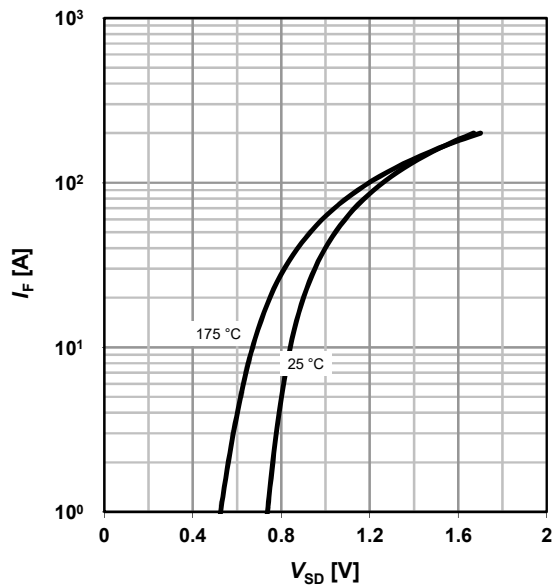
$$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$$



11 Typical forward diode characteristics

$$I_F = f(V_{SD})$$

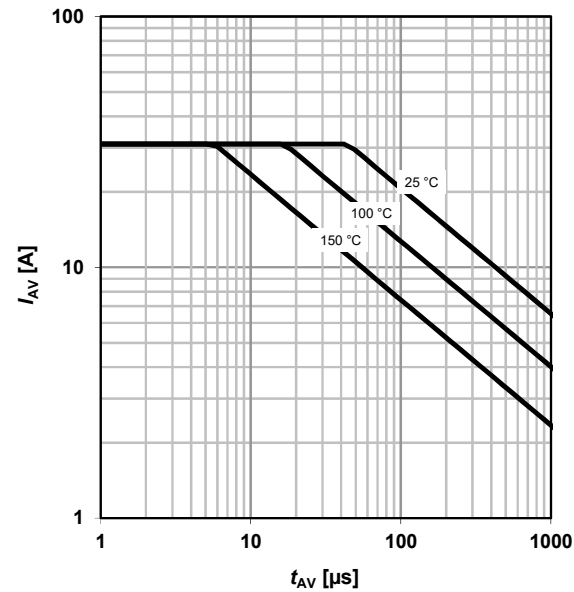
parameter: T_j



12 Avalanche characteristics

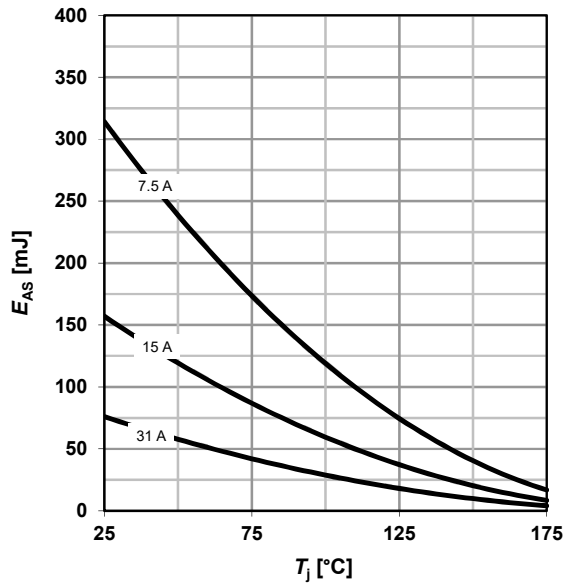
$$I_{AS} = f(t_{AV})$$

parameter: $T_{j(start)}$



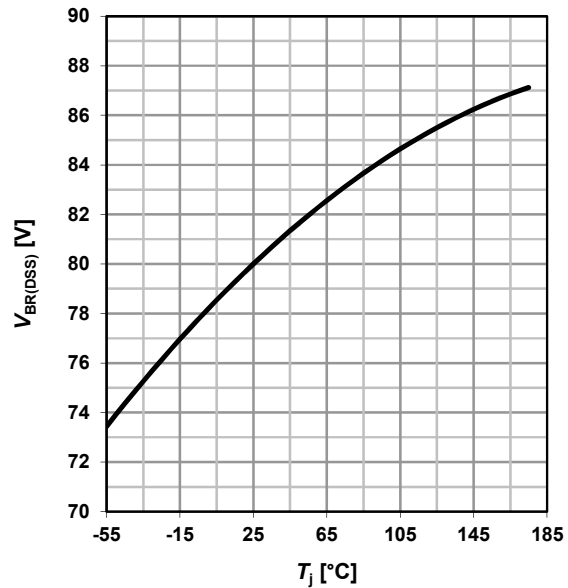
13 Avalanche energy

$$E_{AS} = f(T_j); I_D = 15 \text{ A}$$



14 Drain-source breakdown voltage

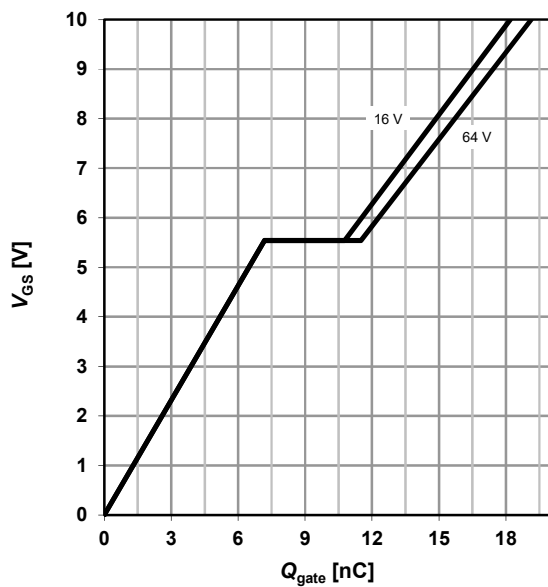
$$V_{BR(DSS)} = f(T_j); I_D = 1 \text{ mA}$$



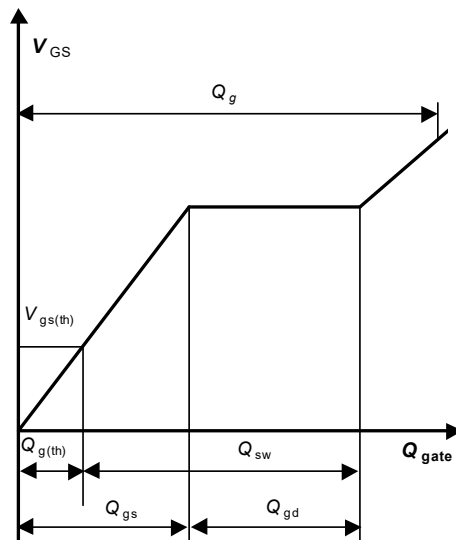
15 Typ. gate charge

$$V_{GS} = f(Q_{gate}); I_D = 50 \text{ A pulsed}$$

parameter: V_{DD}

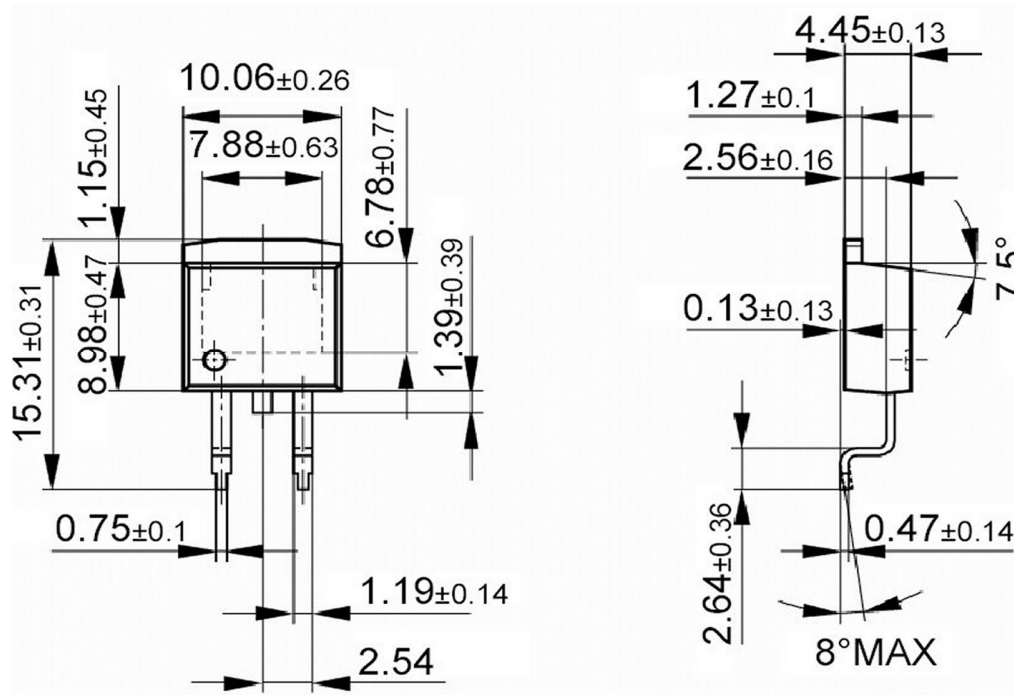


16 Gate charge waveforms

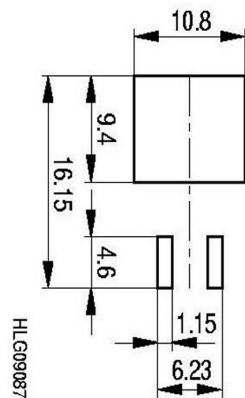


Package Outline

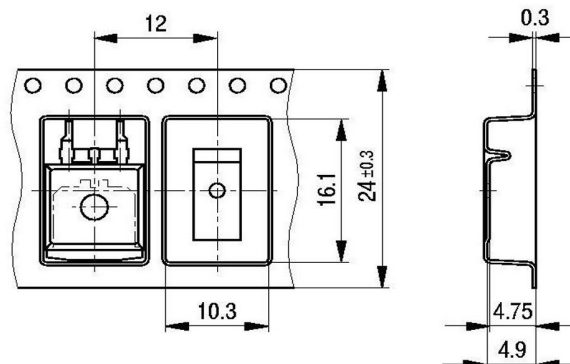
P-TO263-3-2: Outline



Footprint

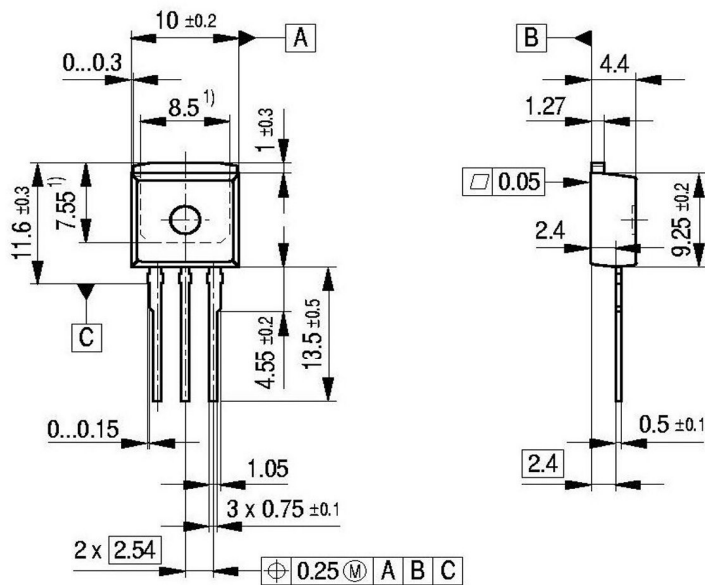


Packaging



Dimensions in mm

P-TO262-3-1: Outline

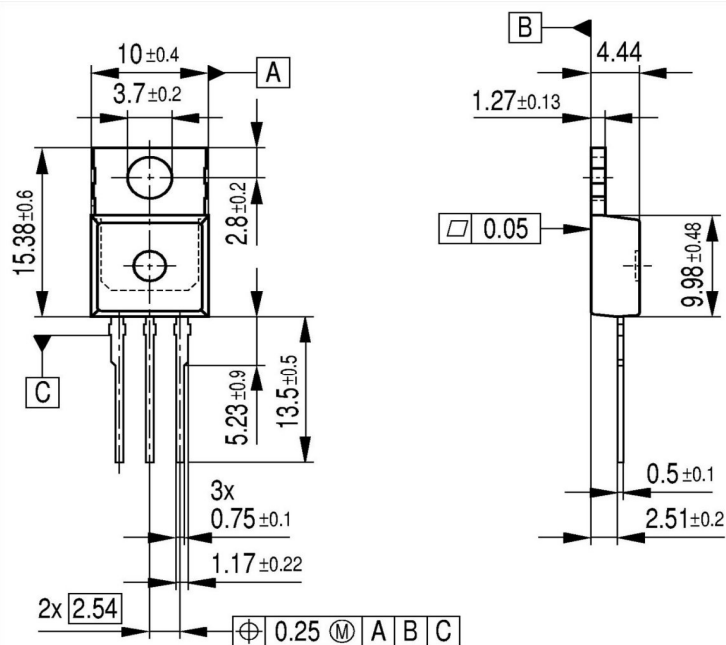


1) Typical

Metal surface min. $X = 7.25$, $Y = 6.9$

All metal surfaces tin plated, except area of cut.

P-TO220-3-1: Outline



All metal surfaces tin plated, except area of cut.

Metal surface min. $x=7.25$, $y=12.3$

Packaging



Dimensions in mm

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Revision History

Version	Date	Changes
Revision 1.0	2014-07-09	Final data sheet
Revision 1.1	2023-02-16	Diagram 8 Typ. drain-source on-state resistance: used α value clarified