

N- and P-Channel 40 V (D-S) MOSFET

PRODUCT SUMMARY

	V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A) ^a	Q _g (Typ.)
N-Channel	40	0.0175 at V _{GS} = 10 V	10	9.8
		0.020 at V _{GS} = 4.5 V	9.2	
P-Channel	- 40	0.021 at V _{GS} = - 10 V	- 9.2	21.7
		0.028 at V _{GS} = - 4.5 V	- 7.4	

FEATURES

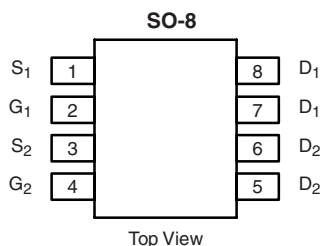
- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Power MOSFET
- 100 % R_g and UIS Tested
- Compliant to RoHS Directive 2002/95/EC



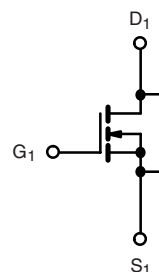
RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

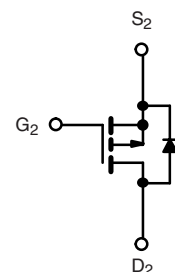
- Notebook PCs



Ordering Information: Si4564DY-T1-GE3 (Lead (Pb)-free and Halogen-free)



N-Channel MOSFET



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T_A = 25 °C, unless otherwise noted

Parameter	Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage	V _{DS}	40	- 40	V
Gate-Source Voltage	V _{GS}	± 16	± 20	
Continuous Drain Current (T _J = 150 °C)	I _D	T _C = 25 °C	10	A
		T _C = 70 °C	8	
		T _A = 25 °C	8.0 ^{b, c}	
		T _A = 70 °C	6.2 ^{b, c}	
Pulsed Drain Current (10 μs Pulse Width)	I _{DM}	40	- 40	
Source-Drain Current Diode Current	I _S	T _C = 25 °C	2.6	
		T _A = 25 °C	1.6 ^{b, c}	
Pulsed Source-Drain Current	I _{SM}	40	- 40	
Single Pulse Avalanche Current	I _{AS}	10	- 20	
Single Pulse Avalanche Energy	E _{AS}	5	20	mJ
Maximum Power Dissipation	P _D	T _C = 25 °C	3.1	W
		T _C = 70 °C	2	
		T _A = 25 °C	2 ^{b, c}	
		T _A = 70 °C	1.28 ^{b, c}	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150		°C

THERMAL RESISTANCE RATINGS

Parameter	Symbol	N-Channel		P-Channel		Unit
		Typ.	Max.	Typ.	Max.	
Maximum Junction-to-Ambient ^{b, d}	R _{thJA}	50	62.5	47	62.5	°C/W
Maximum Junction-to-Foot (Drain)	R _{thJF}	30	40	29	38	

Notes:

a. Based on T_C = 25 °C.

b. Surface Mounted on 1" x 1" FR4 board.

c. t = 10 s.

d. Maximum under Steady State conditions is 120 °C/W (N-Channel) and 110 °C/W (P-Channel).

SPECIFICATIONS $T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted

Parameter	Symbol	Test Conditions		Min.	Typ. ^a	Max.	Unit		
Static									
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	N-Ch	40			V		
		V _{GS} = 0 V, I _D = - 250 μA	P-Ch	- 40					
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	I _D = 250 μA	N-Ch		40		mV/°C		
		I _D = - 250 μA	P-Ch		- 34				
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)} /T _J	I _D = 250 μA	N-Ch		- 4.1				
		I _D = - 250 μA	P-Ch		5.0				
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	N-Ch	0.8		2.0	V		
		V _{DS} = V _{GS} , I _D = - 250 μA	P-Ch	- 1.2		- 2.5			
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 16 V	N-Ch			± 100	nA		
		V _{DS} = 0 V, V _{GS} = ± 20 V	P-Ch			± 100			
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 40 V, V _{GS} = 0 V	N-Ch			1	μA		
		V _{DS} = - 40 V, V _{GS} = 0 V	P-Ch			- 1			
		V _{DS} = 40 V, V _{GS} = 0 V, T _J = 55 °C	N-Ch			10			
		V _{DS} = - 40 V, V _{GS} = 0 V, T _J = 55 °C	P-Ch			- 10			
On-State Drain Current ^b	I _{D(on)}	V _{DS} = 5 V, V _{GS} = 10 V	N-Ch	20			A		
		V _{DS} = - 5 V, V _{GS} = - 10 V	P-Ch	- 20					
Drain-Source On-State Resistance ^b	R _{DS(on)}	V _{GS} = 10 V, I _D = 8 A	N-Ch		0.0145	0.0175	Ω		
		V _{GS} = - 10 V, I _D = - 8 A	P-Ch		0.0175	0.021			
		V _{GS} = 4.5 V, I _D = 5 A	N-Ch		0.017	0.020			
		V _{GS} = - 4.5 V, I _D = - 5 A	P-Ch		0.0232	0.028			
Forward Transconductance ^b	g _{fs}	V _{DS} = 15 V, I _D = 8 A	N-Ch		27		S		
		V _{DS} = - 15 V, I _D = - 8 A	P-Ch		25				
Dynamic ^a									
Input Capacitance	C _{iss}	N-Channel V _{DS} = 20 V, V _{GS} = 0 V, f = 1 MHz	N-Ch		855		pF		
			P-Ch		2000				
Output Capacitance	C _{oss}	P-Channel V _{DS} = - 20 V, V _{GS} = 0 V, f = 1 MHz	N-Ch		120				
			P-Ch		240				
Reverse Transfer Capacitance	C _{rss}		N-Ch		48				
			P-Ch		202				
Total Gate Charge	Q _g	V _{DS} = 20 V, V _{GS} = 10 V, I _D = 10 A	N-Ch		20.5	31	nC		
		V _{DS} = - 20 V, V _{GS} = - 10 V, I _D = - 10 A	P-Ch		41.5	63			
		N-Channel V _{DS} = 20 V, V _{GS} = 4.5 V, I _D = 10 A	N-Ch		9.8	15			
			P-Ch		21.7	33			
Gate-Source Charge	Q _{gs}	P-Channel V _{DS} = - 20 V, V _{GS} = - 4.5 V, I _D = - 10 A	N-Ch		2.6				
			P-Ch		5.6				
Gate-Drain Charge	Q _{gd}		N-Ch		2.6				
			P-Ch		9.8				
Gate Resistance	R _g	f = 1 MHz	N-Ch	0.3	1.5	3.0	Ω		
			P-Ch	1.3	6.4	12.8			



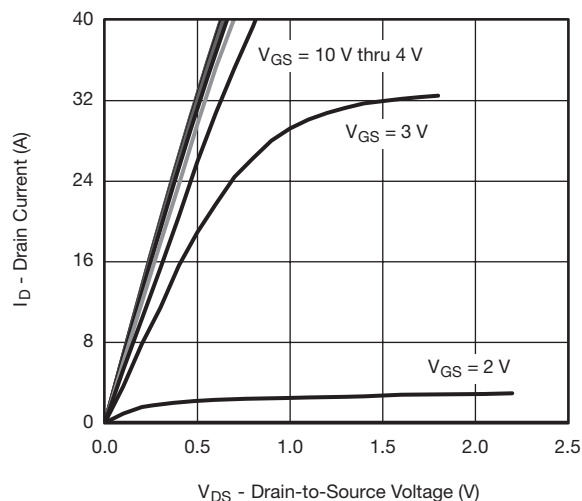
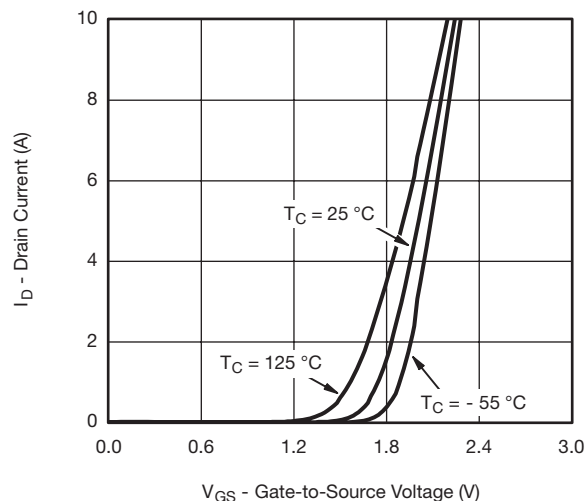
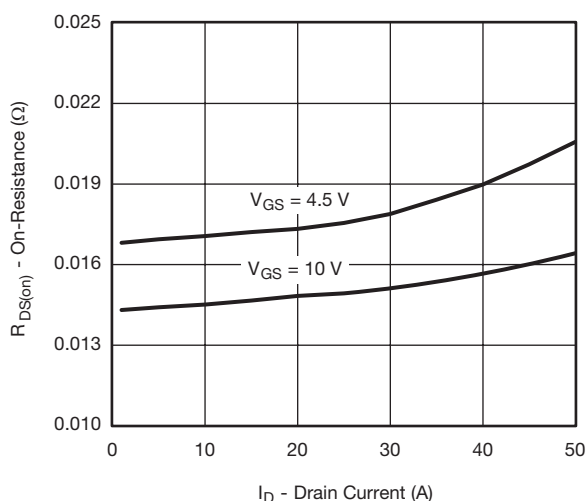
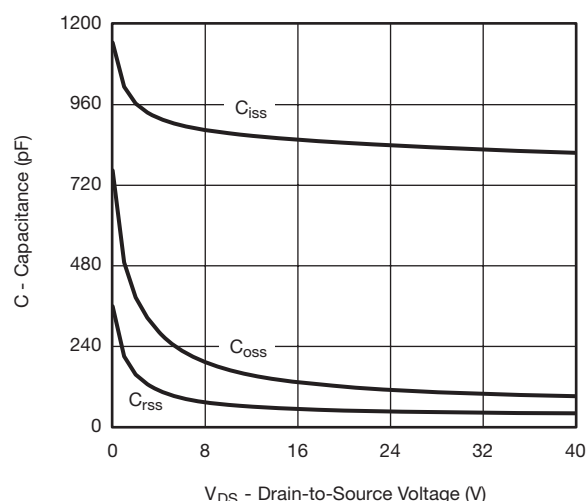
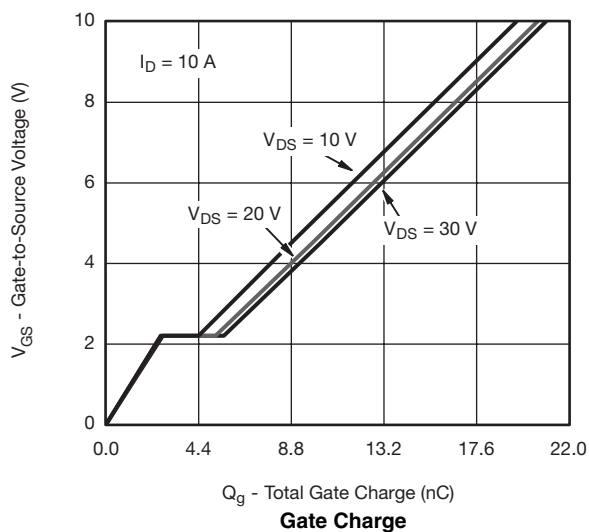
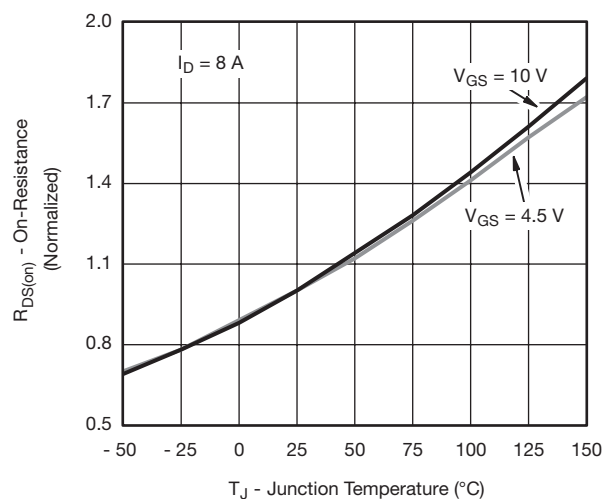
SPECIFICATIONS $T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted							
Parameter	Symbol	Test Conditions		Min.	Typ. ^a	Max.	Unit
Dynamic ^a							
Turn-On Delay Time	$t_{d(on)}$	N-Channel $V_{DD} = 20\text{ V}$, $R_L = 2\text{ }\Omega$ $I_D \cong 10\text{ A}$, $V_{GEN} = 10\text{ V}$, $R_g = 1\text{ }\Omega$	N-Ch		7	14	ns
			P-Ch		9	18	
Rise Time	t_r		N-Ch		10	20	
			P-Ch		9	18	
Turn-Off Delay Time	$t_{d(off)}$	P-Channel $V_{DD} = -20\text{ V}$, $R_L = 2\text{ }\Omega$ $I_D \cong -10\text{ A}$, $V_{GEN} = -10\text{ V}$, $R_g = 1\text{ }\Omega$	N-Ch		18	36	
			P-Ch		50	90	
Fall Time	t_f		N-Ch		9	18	
			P-Ch		14	28	
Turn-On Delay Time	$t_{d(on)}$	N-Channel $V_{DD} = 20\text{ V}$, $R_L = 2\text{ }\Omega$ $I_D \cong 10\text{ A}$, $V_{GEN} = 4.5\text{ V}$, $R_g = 1\text{ }\Omega$	N-Ch		11	22	
			P-Ch		42	75	
Rise Time	t_r		N-Ch		15	30	
			P-Ch		40	70	
Turn-Off Delay Time	$t_{d(off)}$	P-Channel $V_{DD} = -20\text{ V}$, $R_L = 2\text{ }\Omega$ $I_D \cong -10\text{ A}$, $V_{GEN} = -4.5\text{ V}$, $R_g = 1\text{ }\Omega$	N-Ch		23	46	
			P-Ch		40	70	
Fall Time	t_f		N-Ch		13	26	
			P-Ch		15	30	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^{\circ}\text{C}$	N-Ch			2.6	A
			P-Ch			- 2.6	
Pulse Diode Forward Current ^a	I_{SM}		N-Ch			40	
			P-Ch			- 40	
Body Diode Voltage	V_{SD}	$I_S = 2\text{ A}$	N-Ch		0.74	1.2	V
		$I_S = -2\text{ A}$	P-Ch		- 0.77	- 1.2	
Body Diode Reverse Recovery Time	t_{rr}	N-Channel $I_F = 5\text{ A}$, $dI/dt = 100\text{ A}/\mu\text{s}$, $T_J = 25\text{ }^{\circ}\text{C}$	N-Ch		17	34	ns
			P-Ch		30	60	
Body Diode Reverse Recovery Charge	Q_{rr}		N-Ch		10	20	nC
			P-Ch		26	52	
Reverse Recovery Fall Time	t_a	P-Channel $I_F = -5\text{ A}$, $dI/dt = -100\text{ A}/\mu\text{s}$, $T_J = 25\text{ }^{\circ}\text{C}$	N-Ch		10		ns
			P-Ch		15		
Reverse Recovery Rise Time	t_b		N-Ch		7		
			P-Ch		15		

Notes:

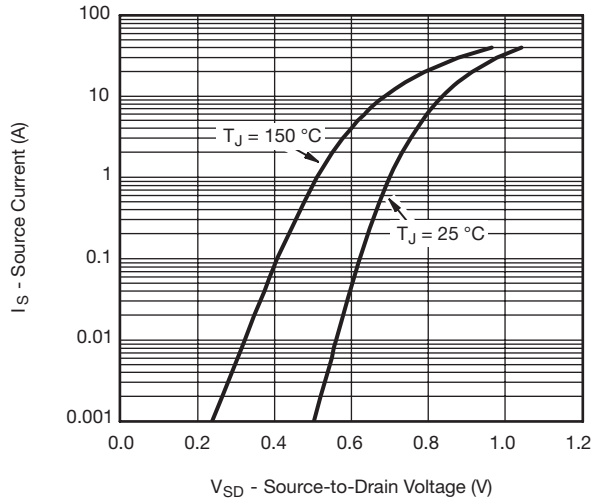
a. Guaranteed by design, not subject to production testing.

b. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

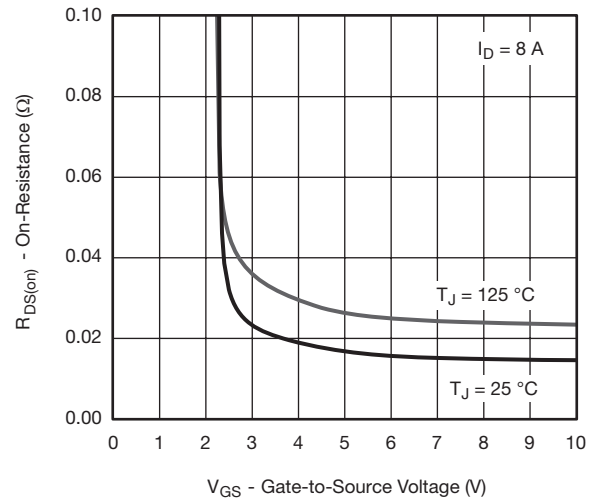
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted**Output Characteristics****Transfer Characteristics****On-Resistance vs. Drain Current and Gate Voltage****Capacitance****Gate Charge****On-Resistance vs. Junction Temperature**

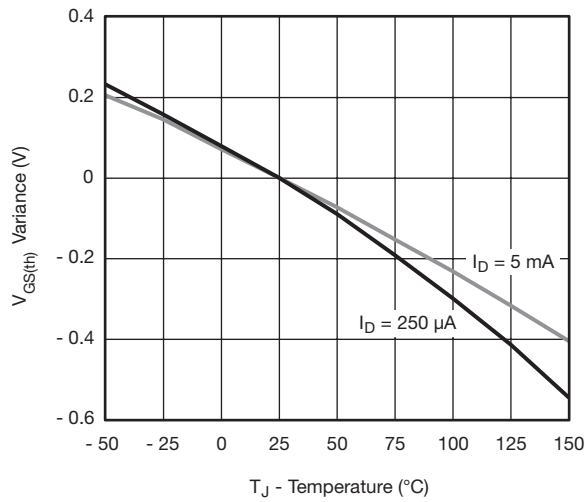
N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



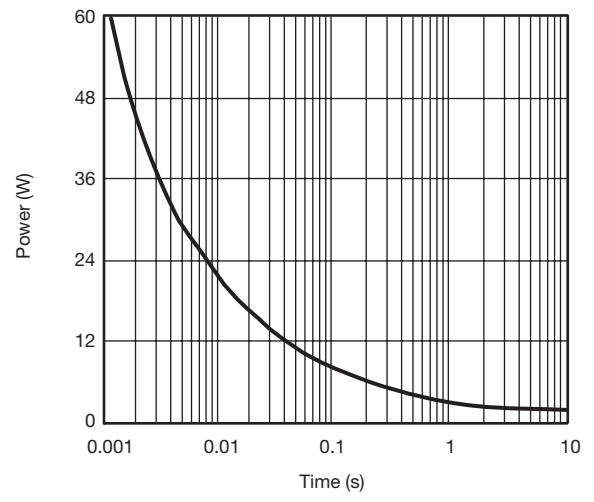
Source-Drain Diode Forward Voltage



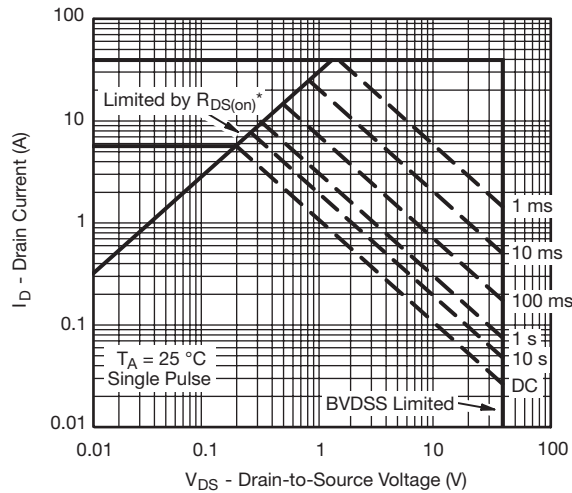
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

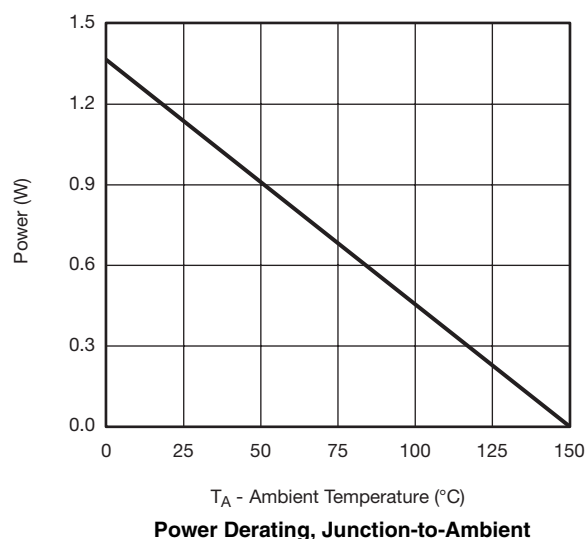
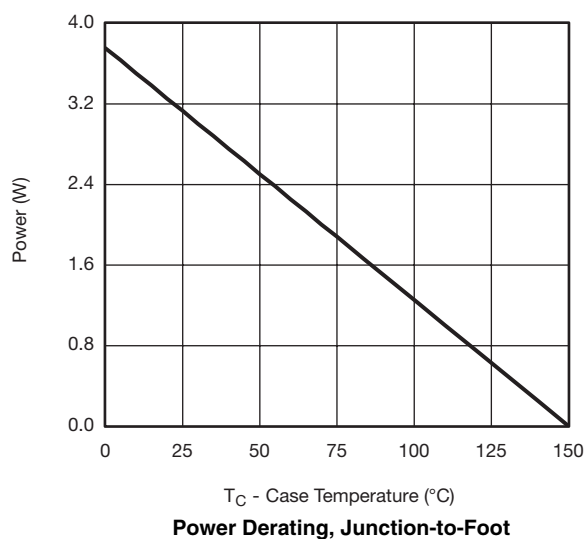
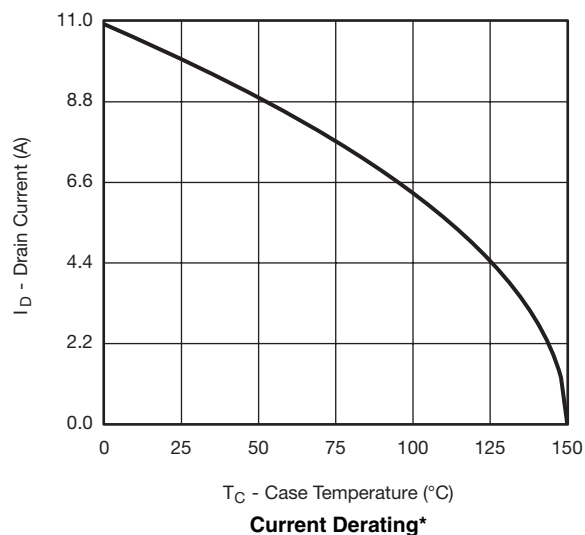


Single Pulse Power, Junction-to-Ambient



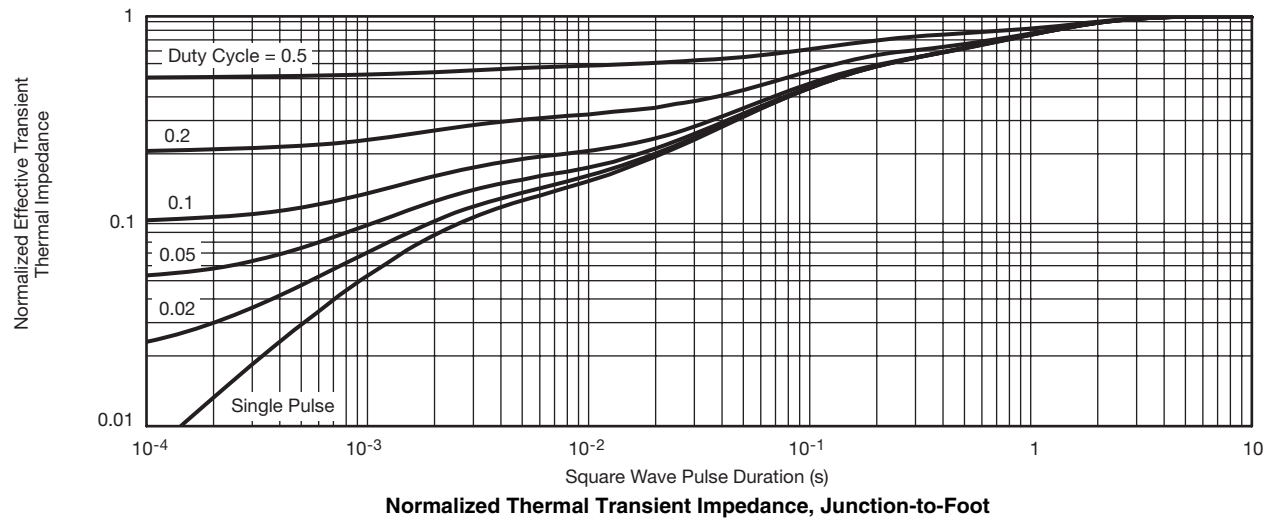
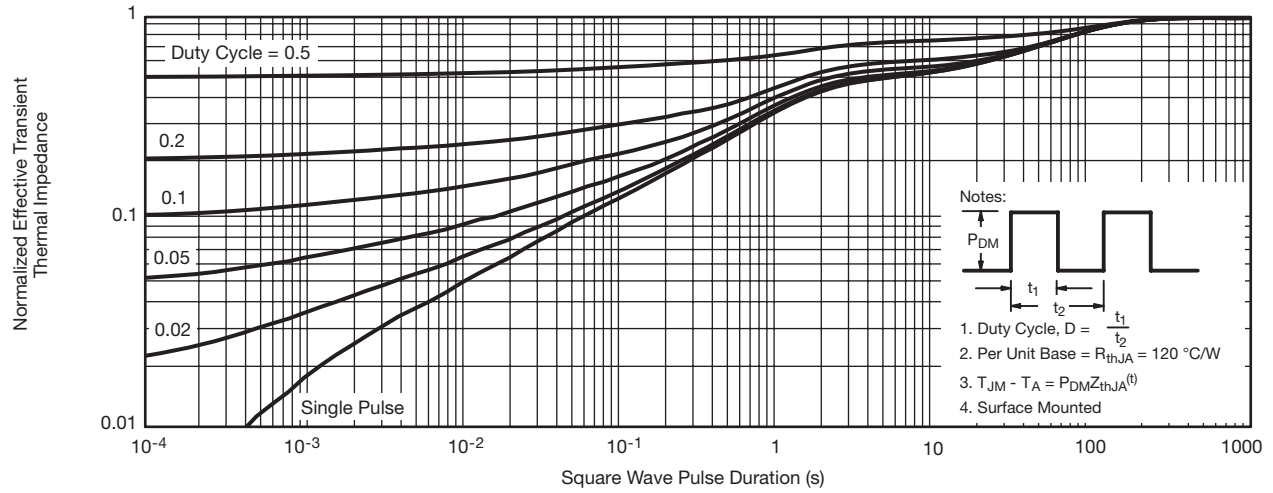
* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

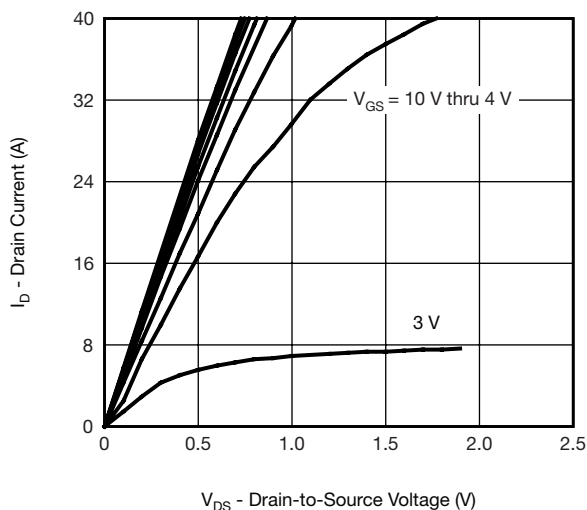
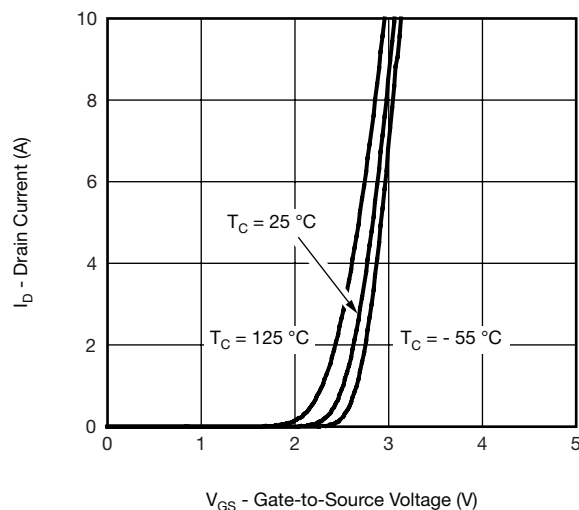
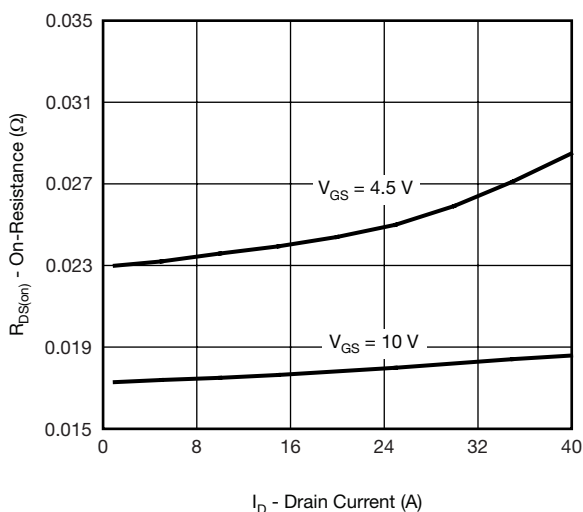
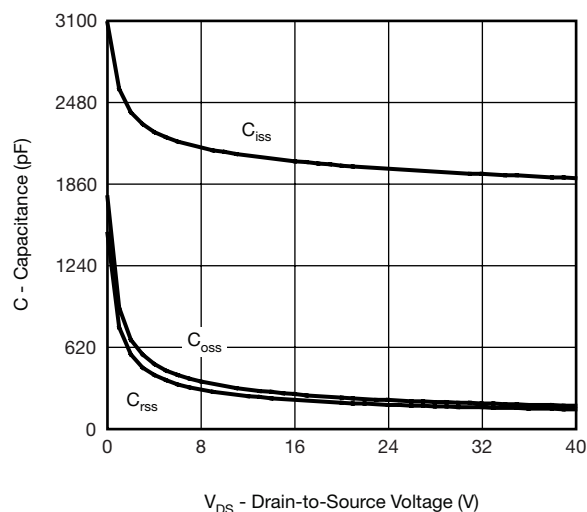
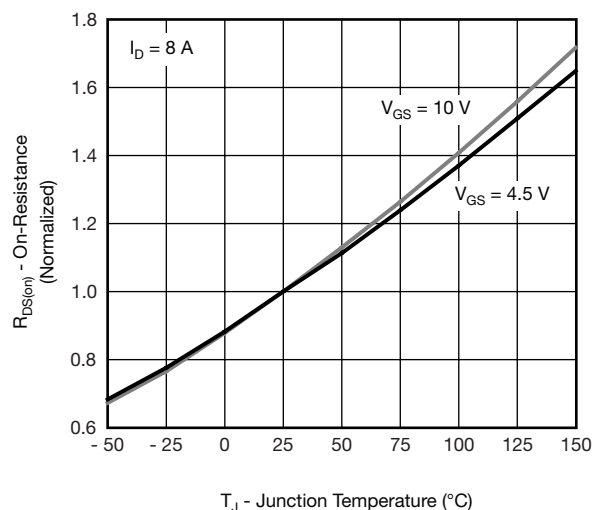
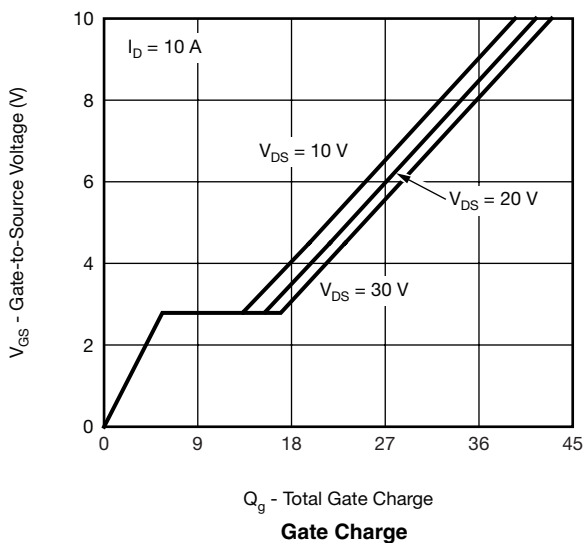
Safe Operating Area, Junction-to-Ambient

N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

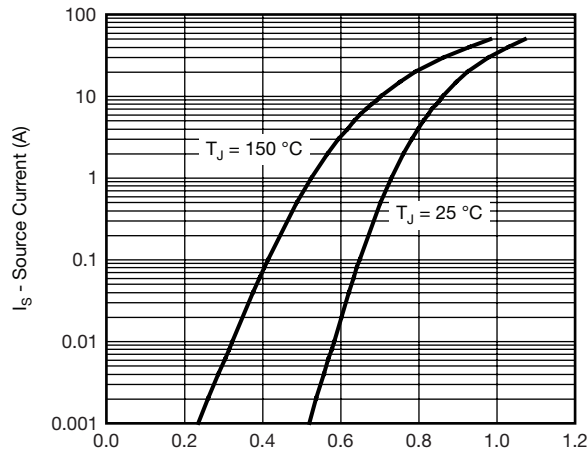
* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

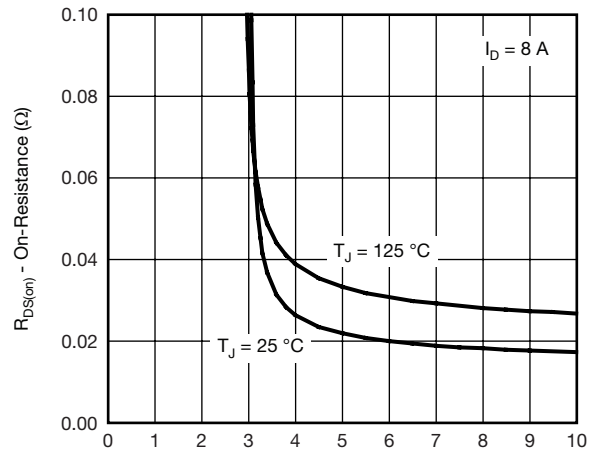


P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted**Output Characteristics****Transfer Characteristics****On-Resistance vs. Drain Current and Gate Voltage****Capacitance****On-Resistance vs. Junction Temperature**

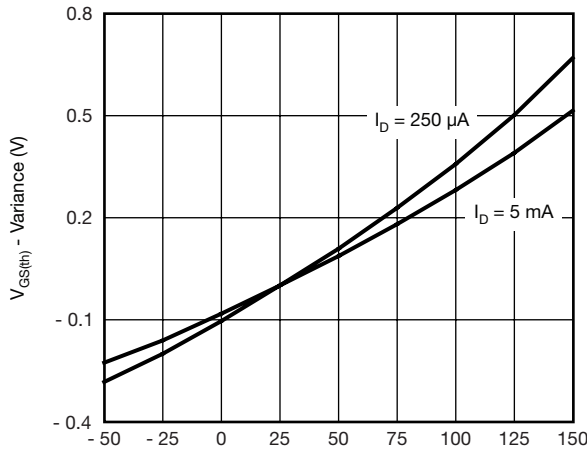
P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



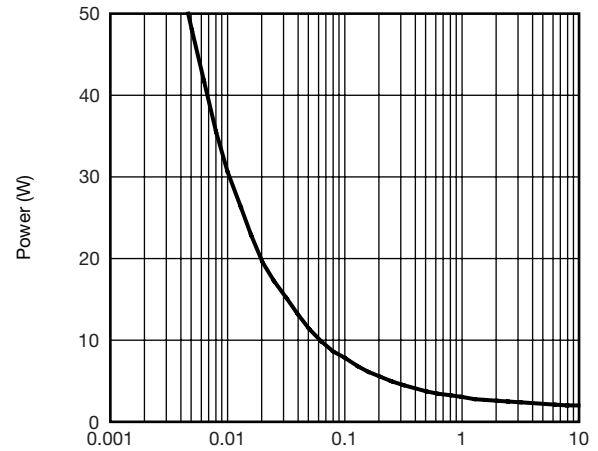
V_{SD} - Source-to-Drain Voltage (V)
Source-Drain Diode Forward Voltage



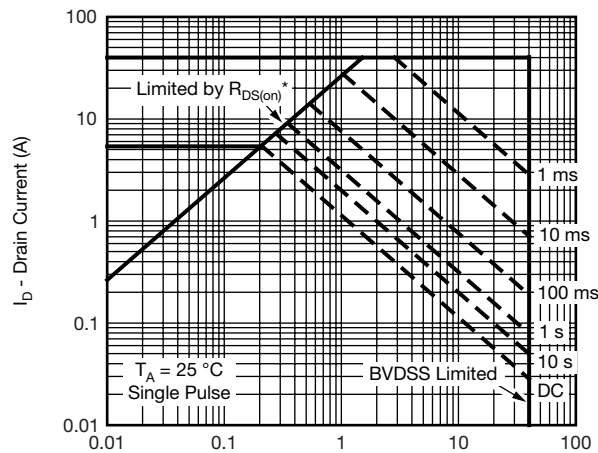
V_{GS} - Gate-to-Source Voltage (V)
On-Resistance vs. Gate-to-Source Voltage



T_J - Junction Temperature ($^\circ\text{C}$)
Threshold Voltage

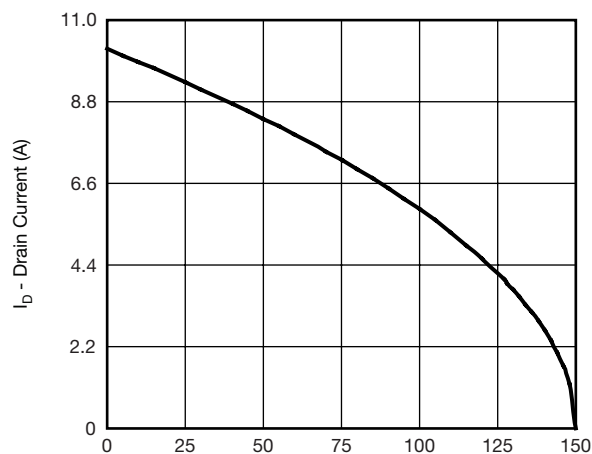
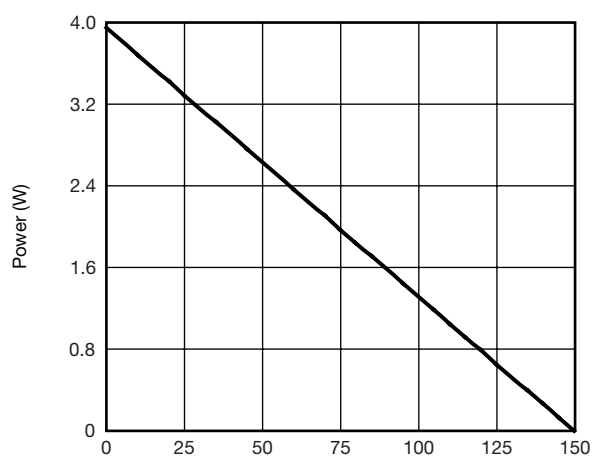
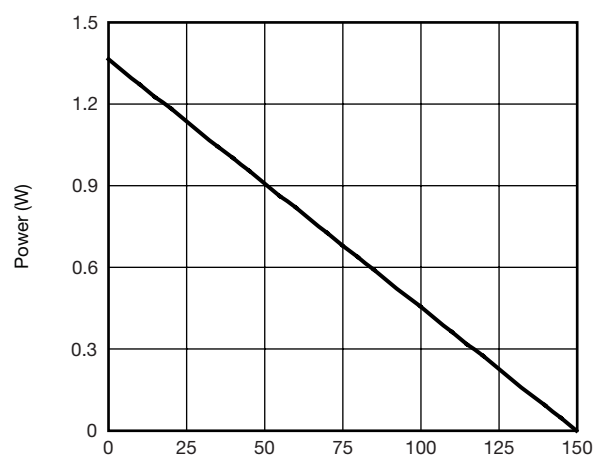


Single Pulse Power, Junction-to-Ambient



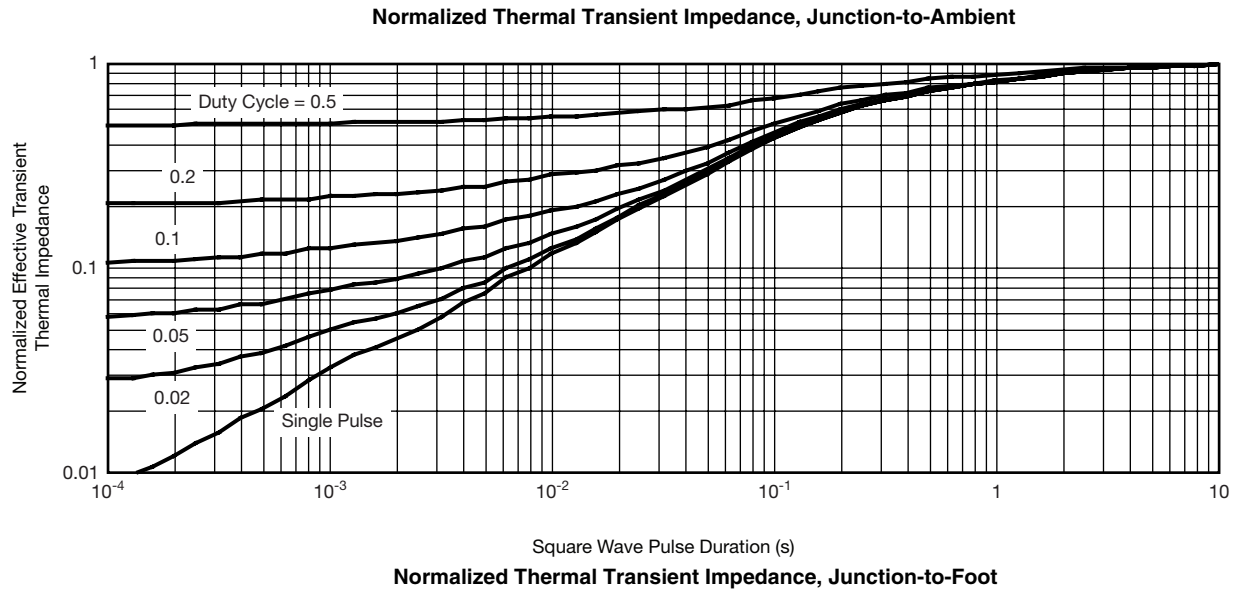
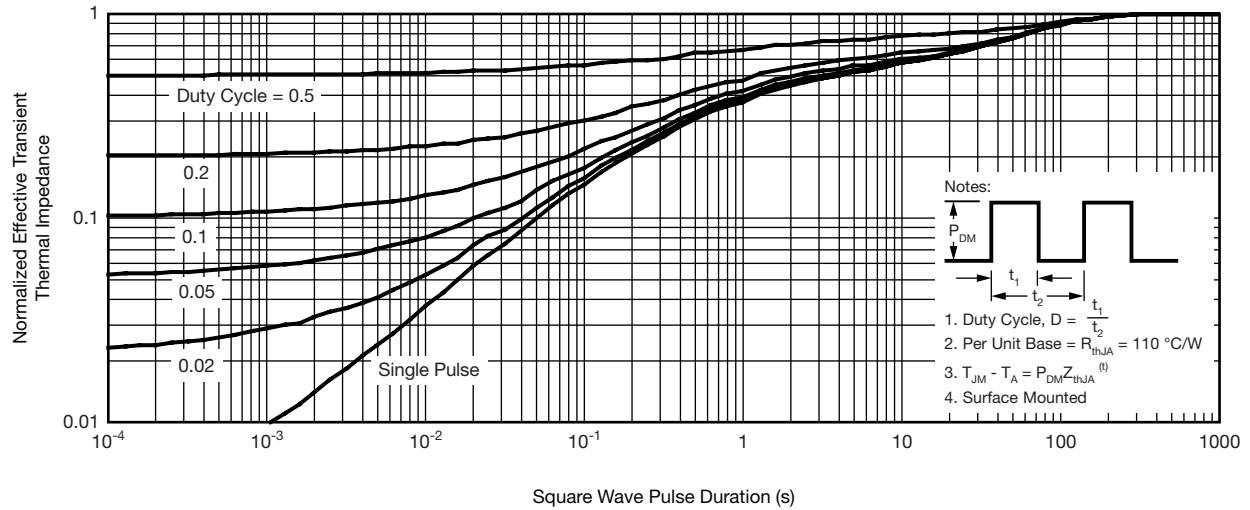
V_{DS} - Drain-to-Source Voltage (V)
* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient

P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted T_C - Case Temperature (°C)**Current Derating*** T_C - Case Temperature (°C)**Power Derating, Junction-to-Foot** T_A - Ambient Temperature (°C)**Power Derating, Junction-to-Ambient**

* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



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SOIC (NARROW): 8-LEAD

JEDEC Part Number: MS-012



DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A ₁	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026
ECN: C-06527-Rev. I, 11-Sep-06				
DWG: 5498				

RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads
Dimensions in Inches/(mm)

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