Features

- Meets the TIA/EIA- 422-B requirements
- High speed, up to 50Mbps data rate, and tPLH = tPHL = 17 ns typical
- Low pulse distortion, tsk(p) = 0.7 ns typical
- -7V ~ +12V Common-Mode Range With ±200mV sensitivity
- Input Hysteresis: 40 mV typical
- Wide power supply voltage 3.0V to 5.5V
- Bus-Pin Protection:
  - ±18 kV HBM protection
  - ±10 kV IEC-Contact ESD
  - ±15 kV IEC-Air Charge ESD
- Pb-Free
- Package: SOP16, TSSOP16

Applications

- Field Transmitters: Temperature Sensors and Pressure Sensors
- Motor Controller and Position Encoder Systems
- Factory Automation
- Industrial Control Networks
-

Description

3PEAK's TPT4032 is an enhanced RS422 device which meets standard TIA/EIA-422-B with strong ESD protection capability. The BUS-pin can pass ±18kV HBM-ESD, and ±15 kV IEC-Air Charge ESD protection. It works in wide power supply range: from 3.0V to 5.5V VCC, which design quad receiver for balanced communication. It also features the wide input common-mode voltage and higher data rate, the TPT4032 can accept -7V ~ +12V common-mode differential input with 100 Ω Load and 50Mbps data rate in 5.0V power supply, required by high speed field-bus applications.

The TPT4032's enable functions can control all four receivers and provide an active-high (G) or active-low (/G) enable input, and they provide the high-impedance state in the power-off condition, which only consume <1uA very low current.

The TPT4032 is available in an SOP16 and TSSOP16 package, and is characterized from –40°C to 125°C.

Typical Application Circuit

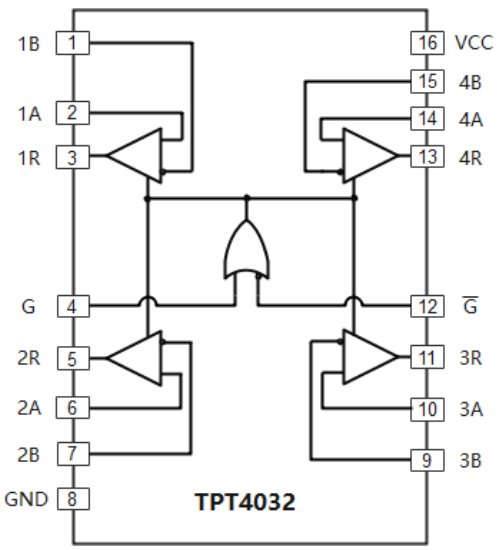
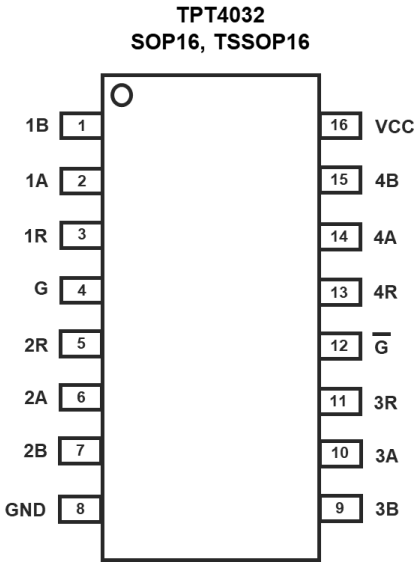


Table of Contents

Revision History

Date	Revision	Notes
2020/11/18	Rev. Pre.0	Definition Version Pre.0
2021/5/26	Rev. 0	Released version
2021/7/21	Rev. A	Updated the Unit of V_{IT+} , V_{IT-}
2022/4/26	Rev. A.1	Updated the order information
2023/7/21	Rev. A.2	Updated the type of V_{IH} V_{IL} test condition in page 7

Pin Configuration and Functions



Pin Functions

Pin		I/O	Description
1B	1	I	RS422/RS485 differential input (inverting)
1A	2	I	RS422/RS485 differential input (noninverting)
1R	3	O	Logic level output
G	4	I	Active-high select
2R	5	O	Logic level output
2A	6	I	RS422/RS485 differential input (noninverting)
2B	7	I	RS422/RS485 differential input (inverting)
GND	8	—	Ground
3B	9	I	RS422/RS485 differential input (inverting)
3A	10	I	RS422/RS485 differential input (noninverting)
3R	11	O	Logic level output
/G	12	I	Active-low select
4R	13	O	Logic level output
4A	14	I	RS422/RS485 differential input (noninverting)
4B	15	I	RS422/RS485 differential input (inverting)
VCC	16	—	Power pin

Absolute Maximum Ratings

Parameter	Description	Min	Max	Unit
VCC	Supply voltage	–0.5	7	V
V_I	Input voltage (G, /G)	–0.3	VCC + 0.3	V
V_{CM}	Common-mode input voltage	–10	+15	V
V_O	Output voltage	–0.5	VCC+0.5	V
I_{IK} I_{OK}	Input or output clamp current		±20	mA
I_O	Output current		±20	mA
I_{OS}	Short-circuit output current		200	mA
T_J	Operating virtual junction temperature		150	°C
Tstg	Storage temperature	–65	150	°C

*** Note:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

(1) This data was taken with the JEDEC low effective thermal conductivity test board.

(2) This data was taken with the JEDEC standard multilayer test boards.

Recommended Operating Conditions

Parameter	Description	Min	Max	Unit
VCC	Supply voltage	3.0	5.5	V
V_{IH}	High-level input voltage (receiver enable inputs)	2	VCC	V
V_{IL}	Low-level input voltage (receiver enable inputs)	0	0.8	V
V_{CM}	Common-mode input voltage	-7	+12	V
R_L	Differential load resistance	100		Ω
T_A	Operating ambient temperature	-40	125	°C

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
IEC	IEC Contact Discharge	IEC-61000-4-2, Bus Pin	±10	kV
	IEC Air-Gap Discharge	IEC-61000-4-2, Bus Pin	±15	kV
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001, Bus Pin	±18	kV
		ANSI/ESDA/JEDEC JS-001, All Pin	±7	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002, All Pin	±1.5	kV
LU	Latch up	LU, per JESD78, All Pin (3)	±500	mA

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
(3) Test at the temperature of 25℃~~C .temperature~~

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
16-Pin TSSOP	118	52	°C/W
16-Pin SOP	93	35	°C/W

Note:
(1) Parameter is provided from 1S0P PCB per JEDEC standard
(2) θ_{JA}, θ_{JC} data is only for reference by design simulation

Electrical Characteristics

Typical value is in VCC = 5.0V, TA = +25°C, RL = 100Ω to GND, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Input Electrical Specifications						
V_{IK}	Enable-input clamp voltage	I_O = 18 mA		-0.8	-1.5	V
V_{IH}	Logic Input High Voltage	G, /G	2.0			V
V_{IL}	Logic Input Low Voltage	G, /G			0.8	V
V_{OH}	High-level output voltage	I_{OH} = -6mA, V_{ID} = +200mV	3.8	4.89		V
V_{OL}	Low-level output voltage	I_{OL} = 6mA, V_{ID} = -200mV		0.11	0.4	V
V_{IT+}	Differential input high-threshold voltage, positive	VI = –7 V to 12 V			0.2	V
V_{IT-}	Differential input low-threshold voltage, negative	VI = –7 V to 12 V	-0.2			V
V_{HYS}	Hysteresis voltage (1)	$V_{IT+} – V_{IT-}$		40		mV
Rin	Input resistance	VI = -7V to12V, one input to ground	96	176		kΩ
$I_{I (A/B)}$	Line input current	VI=12V,Other input at -7V to 12V		48	150	uA
		VI=-7V,Other input at -7V to 12V		61	150	uA
$I_{H(G,/G)}$	High level enable current (2)	VI=VCC		3.2	10	uA
$I_{L(G,/G)}$	Low level enable current (2)	VI=GND	-10	-2.6		uA
I_{OZ}	OFF state(High-impedance-state) output current	Vo=0V or VCC	-1	0	1	uA
I_{OS}	Short-circuit output current	VCC=MAX,Vo=0V,VID>=0.2V	-180	-103		mA
I_{CC}	Quiescent supply current	G,/G=VCC or GND,100 ohm Line inputs resistor		6.5	10	mA
C_i	Input capacitance(1)			18		pF

(1). Test data based on bench test and design simulation

(2). Internal weak pull in/up resistor

AC Electrical Specifications

Typical value is in VCC = 5.0V, TA = +25°C, RL = 100Ω to GND

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
tPLH	Propagation delay time, low-to-high-level output	SW is open, see Figure 1 , CL=15pF		16	30	ns
tPHL	Propagation delay time, high-to-low-level output			19	30	ns
tsk(p)	Pulse skew time ($\|t_{PLH} – t_{PHL}\|$)	SW is open, see Figure 1		3	7	ns
t_r	Differential output rise times	SW is open, see Figure 1, CL=15pF		3.7	11	ns
t_f	Differential output fall times			2.2	11	ns
tPZH	Output enable time to high level	SW is closed, see Figure 3, CL=50pF		10	40	ns
tPZL	Output enable time to low level			13	40	ns

tPHZ	Output disable time from high level	SW is closed, see Figure 3, CL=50pF		27	40	ns
tPLZ	Output disable time from low level			24	40	ns
C_{pd}	Power dissipation capacitance (1)	SW is open, see Figure 2		34		pF

(1). Test data based on bench test and design simulation

Electrical Characteristics (Continue)

Typical value is in VCC = 3.3V, TA = +25°C, RL = 100Ω to GND, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Input Electrical Specifications						
VIK	Enable-input clamp voltage	I_O = 18 mA		-0.8	-1.5	V
VIH	Logic Input High Voltage	G, /G	2.0			V
VIL	Logic Input Low Voltage	G, /G			0.8	V
VOH	High-level output voltage	I_{OH} = -6mA, V_{ID} = +200mV	2.7	3.47		V
VOL	Low-level output voltage	I_{OL} = 6mA, V_{ID} = -200mV		0.16	0.4	V
V_{IT+}	Differential input high-threshold voltage	VI = –7 V to 12 V			0.2	mV
V_{IT-}	Differential input low-threshold voltage	VI = –7 V to 12 V	-0.2			mV
V_{HYS}	Hysteresis voltage (1)	$V_{IT+} – V_{IT-}$		40		mV
Rin	Input resistance	VI = -7V to12V, one input to ground	96	176		kΩ
$I_{I (A/B)}$	Line input current	VI=12V,Other input at -7V to 12V		50	150	uA
		VI=-7V,Other input at -7V to 12V		54	150	uA
$I_{H(G,/G)}$	High level enable current	VI=VCC		2.1	5.5	uA
$I_{L(G,/G)}$	Low level enable current	VI=GND		2.0	5.5	uA
I_{OZ}	OFF state(High-impedance-state) output current	Vo=0V or VCC	-1	0	1	uA
IOS	Short-circuit output current	VCC=MAX,Vo=0V,VID>=0.2V	-85	-58		mA
ICC	Quiescent supply current	G,/G=VCC or GND,100 ohm Line inputs resistor		6.2	8	mA
C_i	Input capacitance(1)			14		pF

(1). Test data based on bench test and design simulation

AC Electrical Specifications

Typical value is in VCC = 3.3V, TA = +25°C, RL = 100Ω to GND, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
tPLH	Propagation delay time, low-to-high-level output	SW is open, see Figure 1 , CL=15pF		22	30	ns
tPHL	Propagation delay time, high-to-low-level output			22	30	ns
tsk(p)	Pulse skew time ($\|t_{PLH} - t_{PHL}\|$)	SW is open, see Figure 1		1.3	6	ns
t_r	Differential output rise times	SW is open, see Figure 1, CL=15pF		3.3	11	ns
t_f	Differential output fall times			3.4	11	ns
tPZH	Output enable time to high level	SW is closed, see Figure 3, CL=50pF		14	40	ns
tPZL	Output enable time to low level			13	40	ns
tPHZ	Output disable time from high level	SW is closed, see Figure 3, CL=50pF		27	40	ns
tPLZ	Output disable time from low level			24	40	ns
C_{pd}	Power dissipation capacitance (1)	SW is open, see Figure 2		27		pF

(1). Test data based on bench test and design simulation

Test Circuits and Waveforms

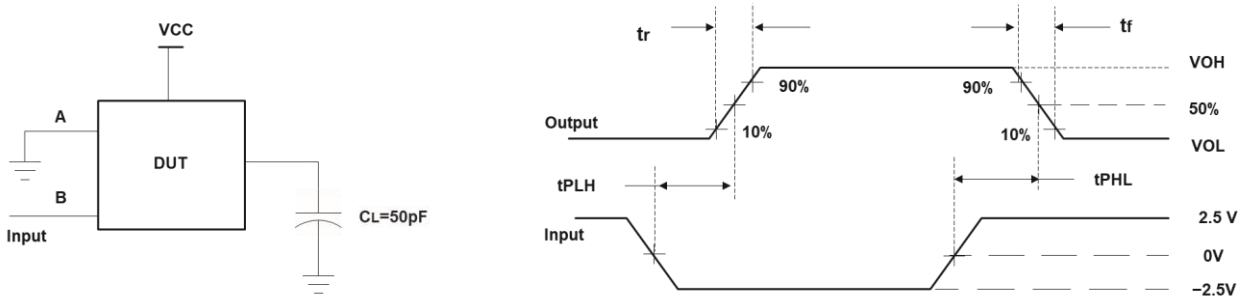


Figure 1. Receiver Propagation Delay and Output Transition Times Measurement

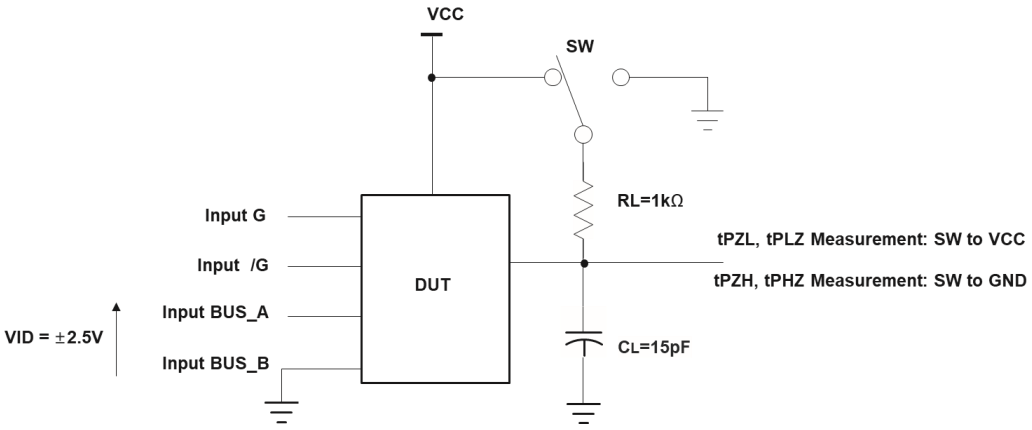


Figure 2. Receiver Propagation Delay and Differential Transition Times -- Test Circuit

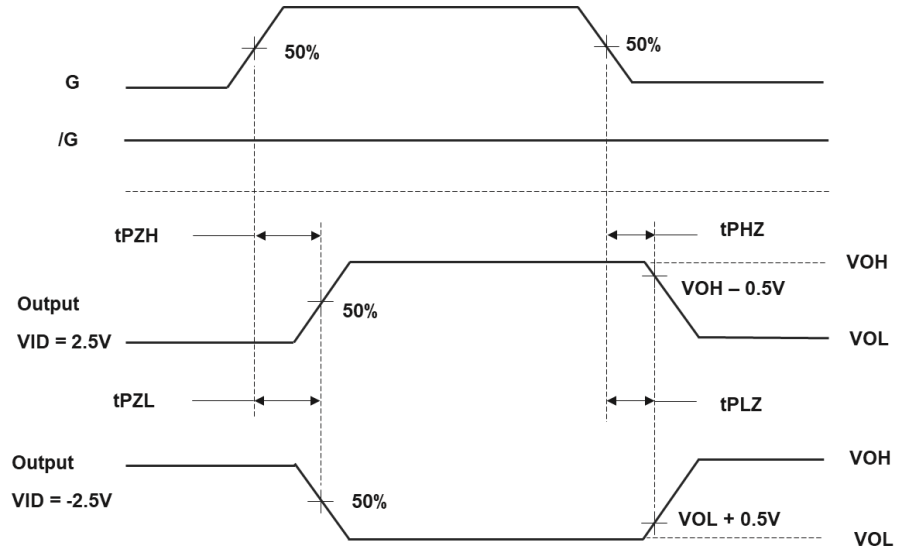


Figure 3A. Receiver Propagation Delay and Differential Transition Times

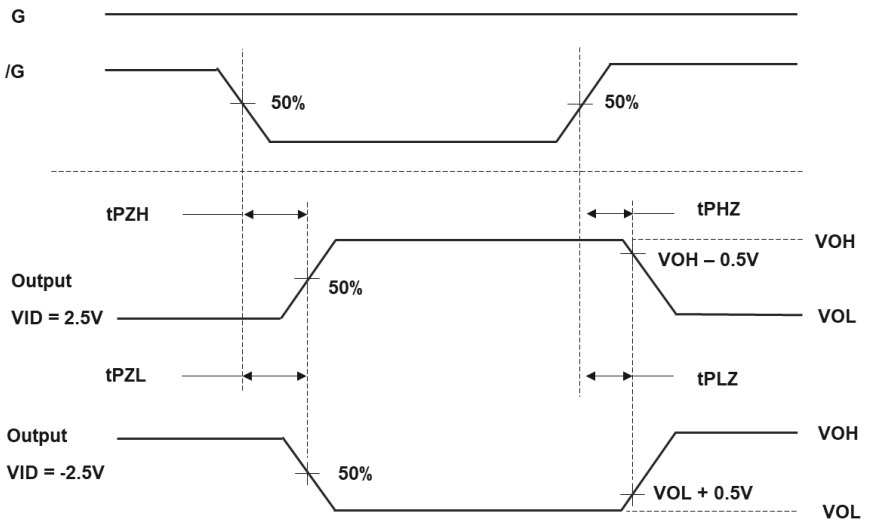


Figure 3B. Receiver Propagation Delay and Differential Transition Times

Theory of Operation

Overview

3PEAK's TPT4032 is an enhanced RS422 device which meets standard TIA/EIA-422-B with strong ESD protection capability. The BUS-pin can pass ±18kV HBM-ESD, and ±15 kV IEC-Air ESD protection. It works in wide power supply range: from 3.0V to 5.5V VCC, which design quad receiver for balanced communication. It also features the wide input common-mode voltage and higher data rate, the TPT4032 can accept -7V ~ +12V common-mode differential input with 100 Ω Load and 50Mbps data rate in 5.0V power supply, required by high speed field-bus applications. The TPT4032 only consume <1uA very low current in the power-off condition.

Function block diagram

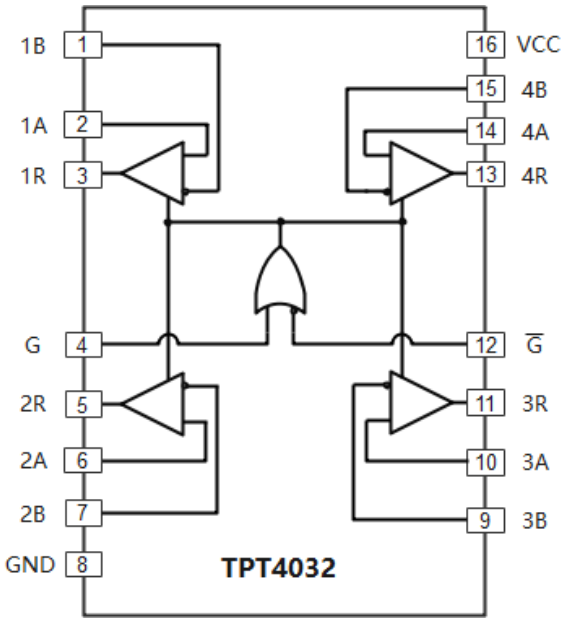


Figure 4. Function block diagram

Feature Description

-7V ~ +12V Common-Mode Range With ±200-mV Sensitivity

For a common-mode voltage range from -7V to +12V, the input voltage is acceptable in low ranges greater than 200 mV as a standard.

Input Fail-Safe function

RS-485 specifies that the receiver output state should be logic high for differential input voltages of VAB ≥ +200 mV and logic low for VAB ≤ –200 mV. For input voltages in between these limits, the receiver output state is not defined and can randomly be high or low. In some abnormal case, if the input signal is removed, the receiver output is defined as certain state (typically high) through internal biasing circuits.

A loss of input signal can be caused by an pen circuit caused by a wire break or the unintentional disconnection of a transceiver from the bus. The TPT4032 has an internal circuit that ensures functionality during an idle bus.

Active-High in G and Active-Low in /G

The G and /G logic inputs can configure the device to select receiver output status, and set a logic high on the G pin or a logic low on the /G pin to enable the device in normal operation mode, and it is easy to configure the logic from a controller or microprocessor.

Power supply

Both the logic and transmitters operate from a single power supply in wide range: 3.0 ~ 5.5V, making designs much more easily. The line quad drivers can operate off the same rail as the host controller or a similar low voltage supply, thus simplifying power structure. The 5.0V power supply is recommended to get better performance, especially in high data rate up-to 50Mbps.

Device Functional Modes

Differential Input A-B	Enables		Outputs
	G	/G	R
$V_{ID} \geq V_{IT+}$	H	X	H
	X	L	H
$V_{IT} < V_{ID} < V_{IT+}$	H	X	?
	X	L	?
$V_{ID} \leq V_{IT-}$	H	X	L
	X	L	L
X	L	H	Z

Note:

H = High level, L = Low level, X = Irrelevant, Z = High impedance (off)

Application and Implementation

Application Information

A typical system usually contain the drivers, receivers, and transceivers complied with RS-422, to reduce reflections in the transmission line, requires the proper cable termination for highly reliable applications. Only one driver on the bus is allowed per RS422 standard, as termination is used in circuit and it is usually placed at the end of the cable near the last receiver. In order to get the good performance and low cost of the application, and decide the type of termination. The different types of termination are unterminated lines, parallel termination, AC termination, and multipoint termination. For laboratory experiments, around 50 meter of 100-Ω, twisted-pair cable, a single driver and receiver, 3PEAK TPT4031 and TPT4032 were tested at room temperature with in 5.0V supply voltage.

Typical Application

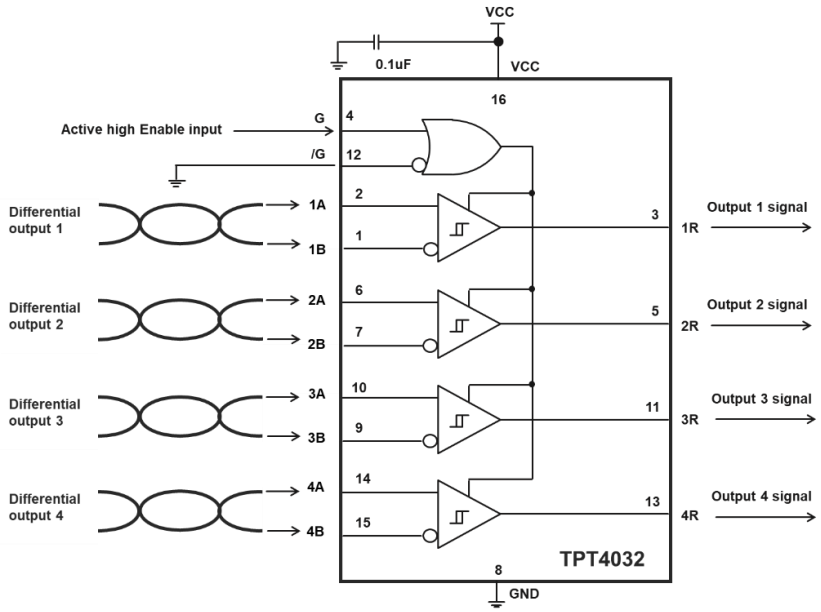


Figure 5. Typical application reference circuit

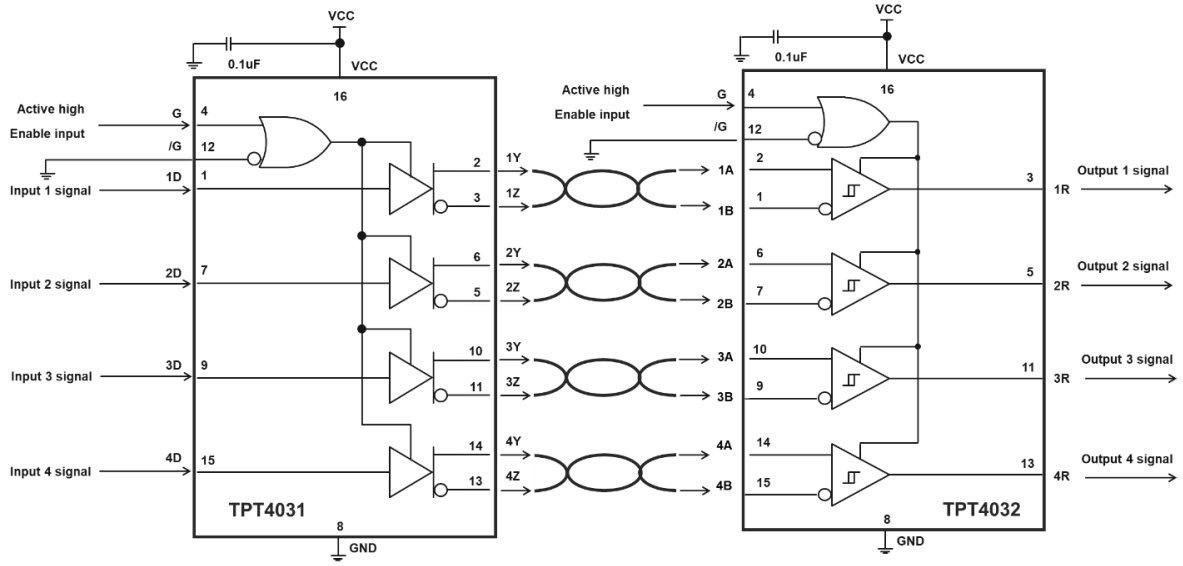
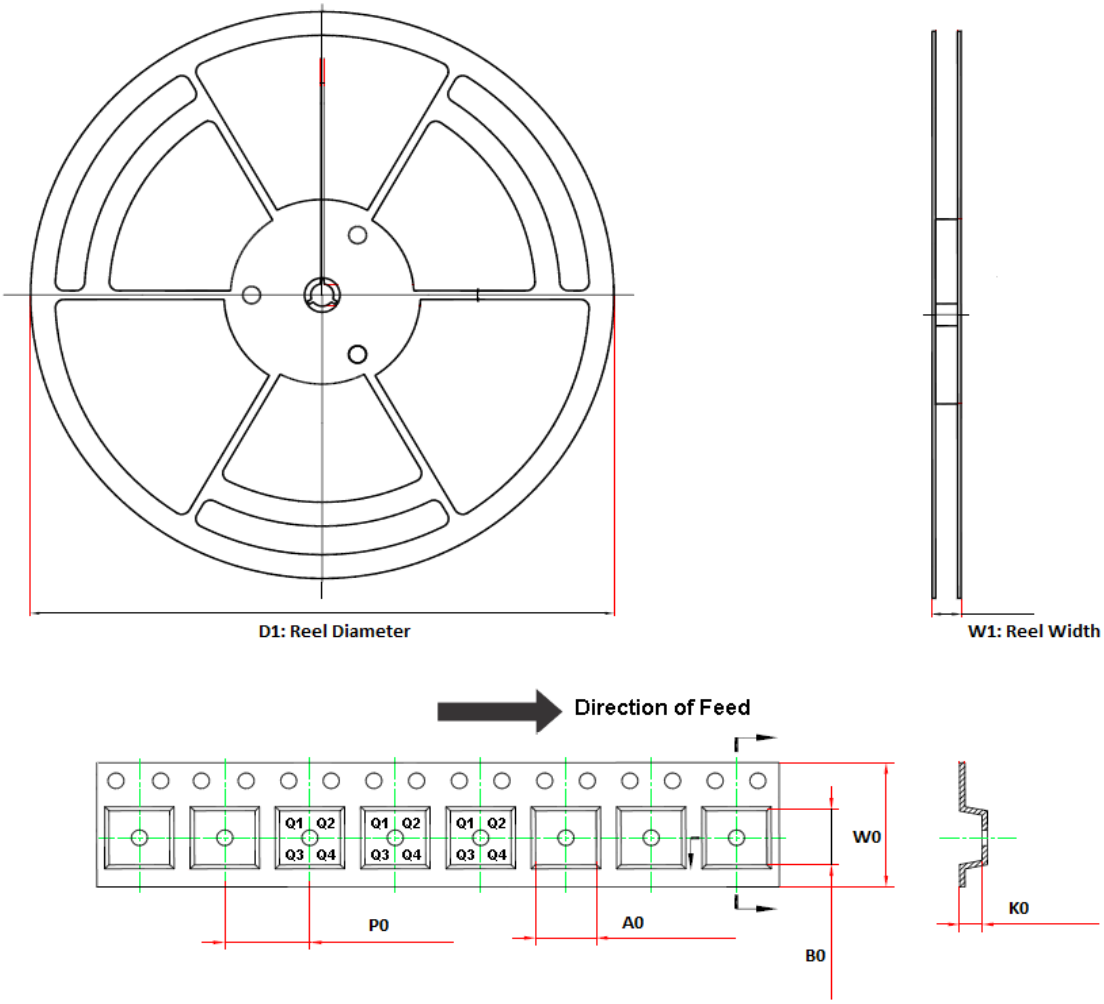


Figure 6. Typical application reference circuit

Resistor and capacitor termination values are shown for each lab experiment, but vary from different system. For example, the termination resistor, R_T, must be within 20% of the characteristic impedance, Zo, of the cable and can vary from about 80 Ω to 120 Ω.

Place 0.1μF bypass capacitors is required close to the power-supply pins to reduce errors coupling in from noisy or high impedance power supplies.

Tape and Reel Information

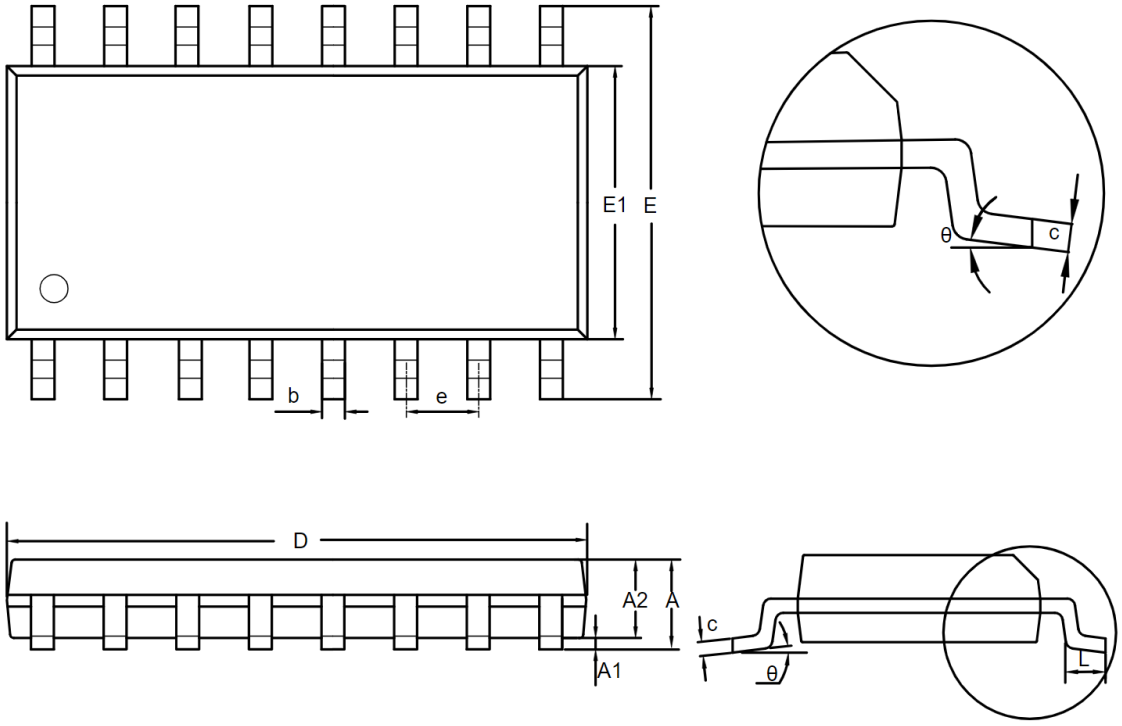


Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPT4032-SO3R	SOP16	330	21.6	6.7	10.4	2.1	8.0	16.0	Q1
TPT4032-TS3R	TSSOP16	330	17.6	6.8	5.4	1.7	8.0	12.0	Q1

Package Outline Dimensions

SO3R (SOP16)

Package Outline Dimensions SO3(SOP-16-A)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.350	1.750	0.053	0.069
A1	0.050	0.250	0.002	0.010
A2	1.300	1.600	0.051	0.063
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	9.800	10.000	0.386	0.394
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
e	1.270 BSC		0.050 BSC	
L	0.400	1.000	0.016	0.039
θ	0	8°	0	8°

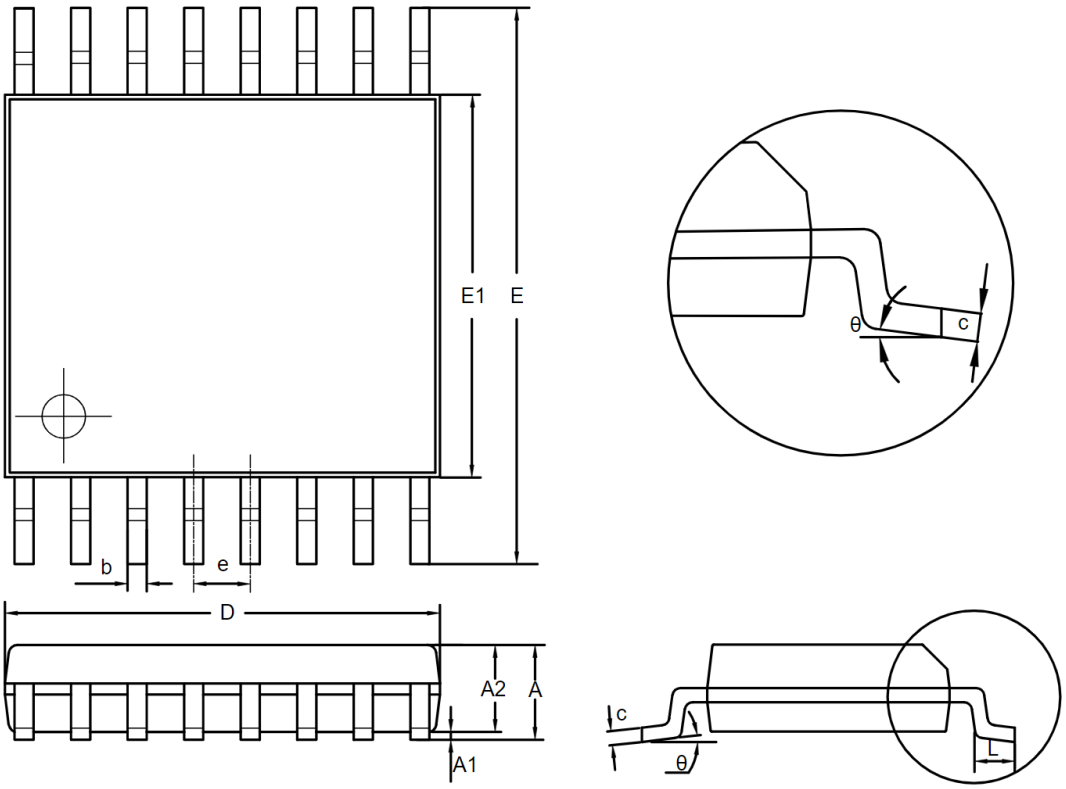
NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Package Outline Dimensions

TS3R (TSSOP16)

Package Outline Dimensions TS3(TSSOP-16-A)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.900	1.200	0.035	0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.050	0.031	0.041
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D	4.900	5.100	0.193	0.201
E	6.200	6.600	0.244	0.260
E1	4.300	4.500	0.169	0.177
e	0.650 BSC		0.026 BSC	
L	0.450	0.750	0.018	0.030
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPT4032-SO3R	-40 to 125°C	16-Pin SOP	T4032	3	Tape and Reel, 2500	Green
TPT4032-TS3R	-40 to 125°C	16-Pin TSSOP	T4032	3	Tape and Reel, 3000	Green

(1) Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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