OPAx387 Ultra-High Precision, Zero-Drift, Low-Input-Bias-Current Op Amps

1 Features

- Ultra-low offset voltage: ±2 μV (maximum, tested)
- Zero drift: ±0.003 μV/°C
- Low-input bias current: 150 pA (maximum, tested)
- Low noise: 8.5 $\text{nV}\sqrt{\text{Hz}}$ at 1 kHz
- No 1/f noise: 177 nV_{PP} (0.1 Hz to 10 Hz)
- Common-mode input range ±100 mV beyond supply rails
- Gain bandwidth: 5.7 MHz
- Quiescent current: 570 μA per amplifier
- Single supply: 1.7 V to 5.5 V
- Dual supply: ±0.85 V to ±2.75 V
- EMI and RFI filtered inputs

2 Applications

- Electronic thermometer
- Weigh scale
- Temperature transmitter
- Ventilators
- Data acquisition (DAQ)
- Semiconductor test
- Lab and field instrumentation
- Merchant network and server PSU
- Analog input module
- Pressure transmitter

3 Description

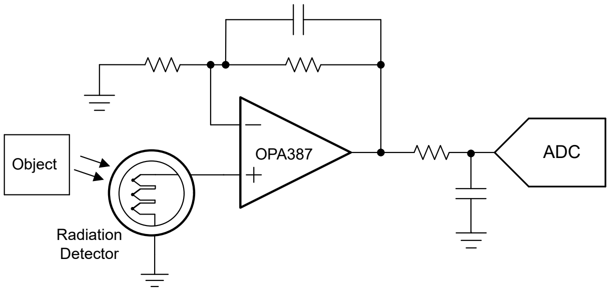
The OPA387, OPA2387, and OPA4387 (OPAx387) family of precision amplifiers offers state-of-the-art performance. With zero-drift technology, the OPAx387 offset voltage and offset drift provide unparalleled long-term stability. With a mere 570 μA of quiescent current, the OPAx387 are able to achieve 5.7 MHz of bandwidth, a broadband noise of 8.5 $\text{nV}/\sqrt{\text{Hz}}$, and a 1/f noise at 177 nV_{PP}. These specifications are crucial to achieve extremely-high precision and no degradation of linearity in 16-bit to 24-bit analog to digital converters (ADCs). The OPAx387 feature flat bias current over temperature; therefore, little to no calibration is needed in high input impedance applications over temperature.

All versions are specified over the industrial temperature range of –40°C to +125°C.

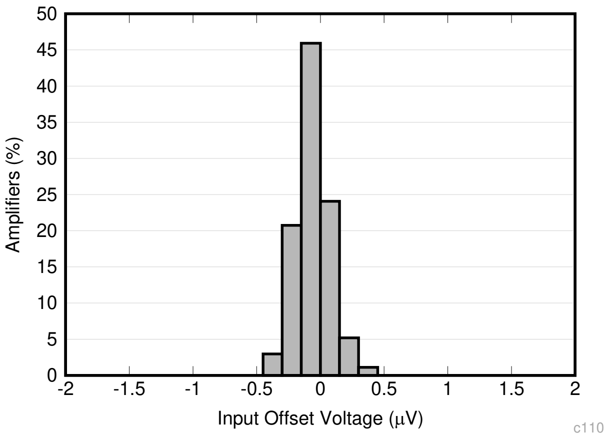
Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
OPA387	SOT-23 (5)	2.90 mm × 1.60 mm
	DFN (6)(3)	1.50 mm × 1.50 mm
OPA2387	SOIC (8)(3)	4.90 mm × 3.90 mm
	VSSOP (8)	3.00 mm × 3.00 mm
	DFN (8)(3)	2.00 mm × 2.00 mm
OPA4387 (2)	TSSOP (14)(3)	5.00 mm × 4.40 mm

(1) For all available packages, see the package option addendum at the end of the data sheet.
(2) Device is preview.
(3) Package is preview.



The OPA387 as an Ultra-Low Offset, Low-Noise ADC Driver



Ultra-Low Input Offset Voltage

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (October 2021) to Revision D (October 2021)	Page
• Added OPA4387 advanced information (preview) device and associated content	1
• Changed low-input bias current Features bullet from 135 pA to 150 pA	1
• Deleted input offset voltage MAX values for over temperature and common-mode voltage test conditions for clarity	7
• Added input offset voltage over temperature TYP value to represent performance shown in typical characteristics	7
• Changed maximum input bias current for OPA387 and OPA2387 from 135 pA to 150 pA	7
• Changed maximum input offset current for OPA387 and OPA2387 from 270 pA to 300 pA	7
• Changed maximum open-loop voltage gain for OPA387 and OPA2387 from 132 dB to 135 dB	7
• Changed settling time to 0.01% from 2.5 µs to 5.5 µs	7
• Changed high linearity output swing from rail for RL = 2 kΩ from 75 mV to 150 mV	7
• Changed short-circuit current for OPA387 at Vs = 1.7 V from ±25 mA to ±15 mA	7
• Added open-loop output impedance at 1 MHz	7
• Changed Figure 6-13, *PSRR and CMRR vs Frequency*, to fit to CMRR and PSRR specifications in the *Electrical Characteristic* table	9
• Changed Figure 6-24, *Phase Margin vs Capacitive Load*, to add test condition	9

Changes from Revision B (August 2021) to Revision C (October 2021)	Page
• Changed OPA387 from advanced information (preview) to production data (active)	1

Changes from Revision A (December 2020) to Revision B (August 2021)	Page
• Added OPA387 advanced information (preview) device and associated content	1

Changes from Revision * (November 2020) to Revision A (December 2020)	Page
• Changed OPA2387 from advanced information (preview) to production data (active)	1

5 Pin Configuration and Functions

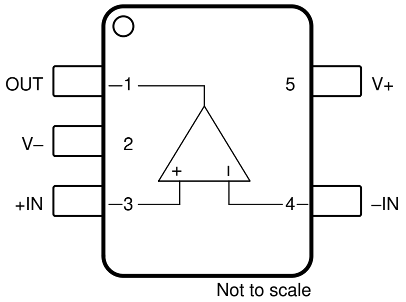


Figure 5-1. OPA387: DBV (5-Pin SOT-23) Package, Top View

Table 5-1. Pin Functions: OPA387

PIN		TYPE	DESCRIPTION
NAME	NO.		
–IN	4	Input	Inverting input
+IN	3	Input	Noninverting input
NC	—	—	No internal connection (can be left floating)
OUT	1	Output	Output
V–	2	Power	Negative (lowest) power supply
V+	5	Power	Positive (highest) power supply

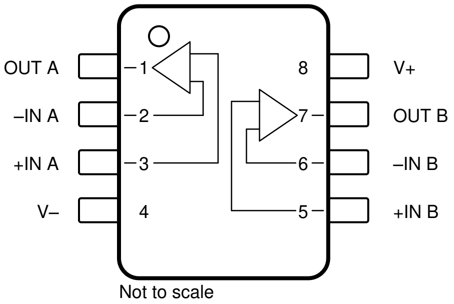
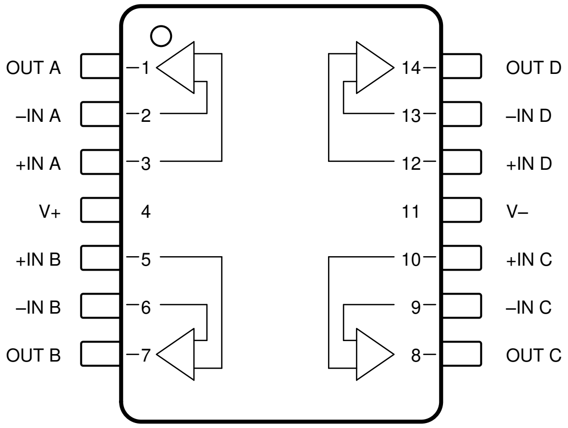


Figure 5-2. OPA2387: DGK (8-Pin VSSOP) Package, Top View

Table 5-2. Pin Functions: OPA2387

PIN		TYPE	DESCRIPTION
NAME	NO.		
–IN A	2	Input	Inverting input, channel A
–IN B	6	Input	Inverting input, channel B
+IN A	3	Input	Noninverting input, channel A
+IN B	5	Input	Noninverting input, channel B
OUT A	1	Output	Output, channel A
OUT B	7	Output	Output, channel B
V–	4	Power	Negative (lowest) power supply
V+	8	Power	Positive (highest) power supply



Not to scale

Figure 5-3. OPA4387: PW (Preview) Package, 14-Pin TSSOP, Top View

Table 5-3. Pin Functions: OPA4387

PIN		TYPE	DESCRIPTION
NAME	NO.		
–IN A	2	Input	Inverting input, channel A
–IN B	6	Input	Inverting input, channel B
–IN C	9	Input	Inverting input, channel C
–IN D	13	Input	Inverting input, channel D
+IN A	3	Input	Noninverting input, channel A
+IN B	5	Input	Noninverting input, channel B
+IN C	10	Input	Noninverting input, channel C
+IN D	12	Input	Noninverting input, channel D
EP	—	—	Connect Thermal Pad to V–
OUT A	1	Output	Output, channel A
OUT B	7	Output	Output, channel B
OUT C	8	Output	Output, channel C
OUT D	14	Output	Output, channel D
V–	11	Power	Negative (lowest) power supply
V+	4	Power	Positive (highest) power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_S	Supply Voltage, V_S = (V+) – (V–)	Single-supply		6	V
		Dual-supply		±3	
	Input voltage, all pins	Common-mode	(V–) – 0.5	(V+) + 0.5	V
		Differential		(V+) – (V–) + 0.2	
	Input current, all pins			±10	mA
	Output short circuit[2]		Continuous	Continuous	
T_A	Operating temperature		–55	150	°C
T_J	Junction temperature		–55	150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Short-circuit to ground, one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±3000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002[2]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_S	Supply voltage, V_S = (V+) – (V–)	Single-supply	1.7		5.5	V
		Dual-supply	±0.85		±2.75	
T_A	Specified temperature		–40		125	°C

6.4 Thermal Information: OPA387

THERMAL METRIC[1]		OPA387	UNIT
		DBV (SOT-23)	
		5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	187.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	107.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	57.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	33.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	57.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Thermal Information: OPA2387

THERMAL METRIC[1]		OPA2387	UNIT
		DGK (VSSOP)	
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	165	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	53	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	87	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	4.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	85	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

Thermal Information: OPA4387

THERMAL METRIC[1]		OPA4387	UNIT
		PW (TSSOP)	
		14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	109.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	27.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	56.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	54.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.6 Electrical Characteristics

at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_S = 1.7 V to 5.5 V, V_{CM} = V_S / 2, V_{OUT} = V_S / 2, and min and max specification established from manufacturing final test (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	V_S = 5.5 V			±0.25	±2	µV
		V_S = 1.7 V			±0.35	±2.5	
		T_A = –40°C to +125°C[1]			±0.4		
dV_{OS}/dT	Input offset voltage drift	T_A = –40°C to +125°C[1]	OPA387, OPA2387		±0.003	±0.012	µV/°C
			OPA4387			±0.018	
PSRR	Power supply rejection ratio	OPA387, OPA2387			±0.05	±0.35	µV/V
		OPA4387				±0.5	
		T_A = –40°C to +125°C[1]				±1	
INPUT BIAS CURRENT							
I_B	Input bias current	OPA387, OPA2387			±30	±150	pA
		OPA4387				±300	
		T_A = –40°C to +125°C[1]				±200	
I_{OS}	Input offset current	OPA387, OPA2387			±60	±300	pA
		OPA4387				±500	
		T_A = –40°C to +125°C[1]				±400	
NOISE							
	Input voltage noise	f = 0.1 Hz to 10 Hz			177		nV_{PP}
					27		nV_{RMS}
e_N	Input voltage noise density	f = 1 Hz			8.5		nV/√Hz
		f = 10 Hz			8.5		
		f = 100 Hz			8.5		
		f = 1 kHz			8.5		
i_N	Input current noise	f = 1 kHz			70		fA/√Hz
INPUT VOLTAGE							
V_{CM}	Common-mode voltage range	V_S = 1.7 V		(V–) – 0.1		(V+)	V
		V_S = 5.5 V		(V–) – 0.2		(V+) + 0.1	
CMRR	Common-mode rejection ratio	(V–) – 0.1 V < V_{CM} < (V+), V_S = 1.7 V		115	138		dB
		(V–) – 0.2 V < V_{CM} < (V+) + 0.1 V, V_S = 5.5 V	OPA387, OPA2387	140	150		
			OPA4387	130			
		(V–) – 0.1 V < V_{CM} < (V+), T_A = –40°C to +125°C[1]		110	132		
		(V–) – 0.2 V < V_{CM} < (V+) + 0.1, V_S = 5.5 V, T_A = –40°C to +125°C[1]		130			
INPUT CAPACITANCE							
Z_{ID}	Differential				100 || 3		MΩ || pF
Z_{ICM}	Common-mode				60 || 3		GΩ || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	(V–) + 100 mV < V_{OUT} < (V+) – 100 mV	OPA387, OPA2387	135	145		dB
			OPA4387	120			
			T_A = –40°C to +125°C[1]	125			
		(V–) + 150 mV < V_{OUT} < (V+) – 150 mV, R_L = 2 kΩ	OPA387, OPA2387	132	145		
			OPA4387	120			
			T_A = –40°C to +125°C[1]	125			

6.6 Electrical Characteristics (continued)

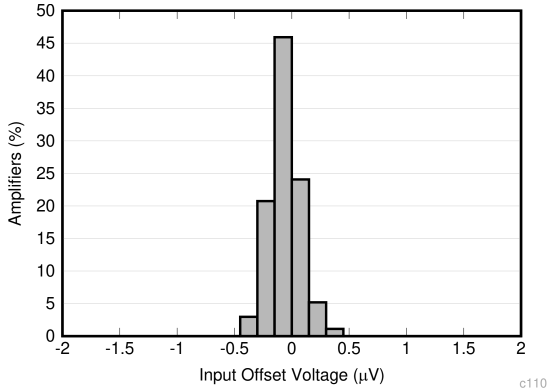
at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_S = 1.7 V to 5.5 V, V_{CM} = V_S / 2, V_{OUT} = V_S / 2, and min and max specification established from manufacturing final test (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product				5.7		MHz
SR	Slew rate	4-V step, G = +1			2.8		V/µs
t_S	Settling time	To 0.1%, 1-V step , G = +1			1.5		µs
		To 0.01%, 1-V step , G = +1			5.5		
	Overload recovery time	V_{IN} × G > V_S			500		ns
	Chopping clock frequency(1)			100	150		kHz
THD+N	Total harmonic distortion + noise	V_{OUT} = 1 V_{RMS}, G = +1, f = 1 kHz			0.002 %		
OUTPUT							
	Voltage output swing from rail	No load	OPA387, OPA2387		1	10	mV
		No load	OPA4387			20	
					5	30	
		R_L = 2 kΩ	OPA387, OPA2387		20	60	
		R_L = 2 kΩ	OPA4387			75	
		T_A = –40°C to +125°C(1)				30	
	High linearity output swing range(1)	A_{OL} > 120 dB		(V–) + 0.075		(V+) – 0.075	V
			R_L = 2 kΩ	(V–) + 0.150		(V+) – 0.150	
I_{SC}	Short-circuit current	V_S = 5.5 V			±55		mA
		V_S = 1.7 V	OPA2387		±25		
			OPA387, OPA4387		±15		
	Phase margin	C_L = 100 pF, G = +1			40		degrees
R_O	Open-loop output impedance	f = 1 MHz			250		Ω
POWER SUPPLY							
I_Q	Quiescent current per amplifier	I_O = 0 mA			570	675	µA
			T_A = –40°C to 125°C(1)			700	
	Turn-on time	At V_S = 5.5 V, V_S ramp rate > 0.3 V/µs, settle to 1%			25	100	µs

(1) Specification established from device population bench system measurements across multiple lots.

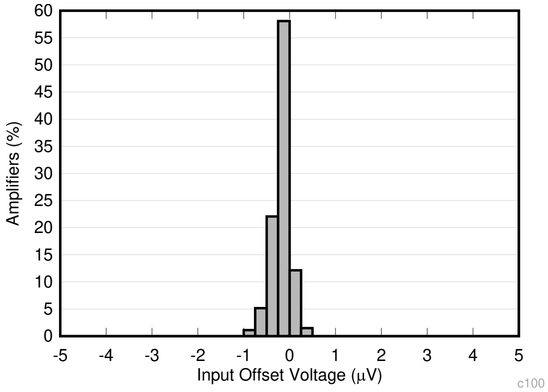
6.7 Typical Characteristics

at T_A = 25°C, V_S = ±2.75 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 50 pF (unless otherwise noted)



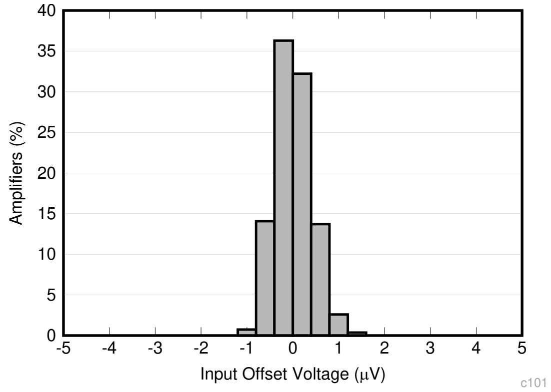
V_S = 5.5 V, T_A = 25°C

Figure 6-1. Offset Voltage Distribution



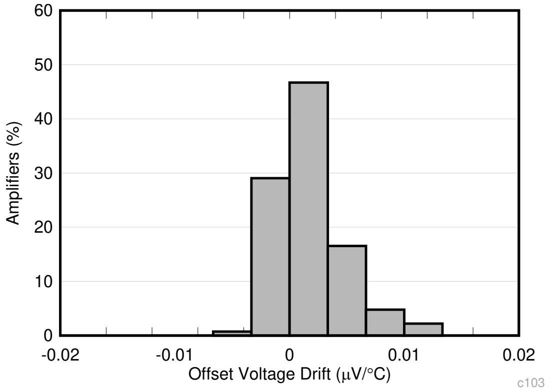
V_S = 5.5 V, T_A = –40°C

Figure 6-2. Offset Voltage Distribution



V_S = 5.5 V, T_A = 125°C

Figure 6-3. Offset Voltage Distribution



V_S = 5.5 V

Figure 6-4. Offset Voltage Drift Distribution

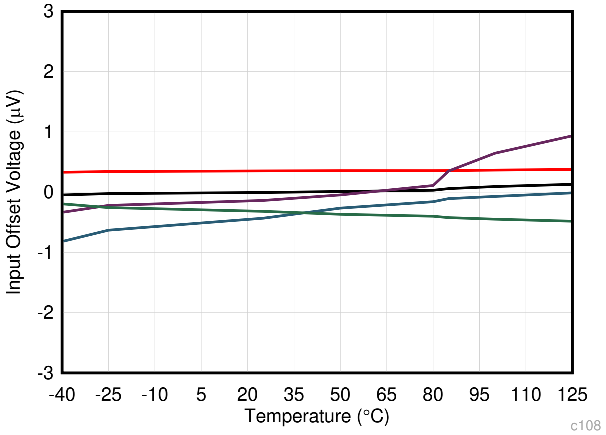


Figure 6-5. Offset Voltage vs Temperature

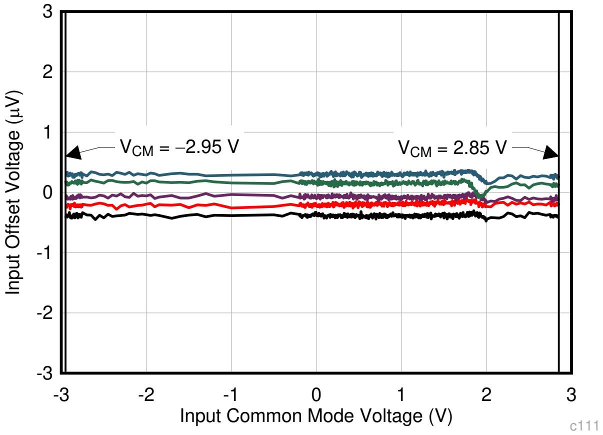


Figure 6-6. Offset Voltage vs Common-Mode Voltage

6.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±2.75 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 50 pF (unless otherwise noted)

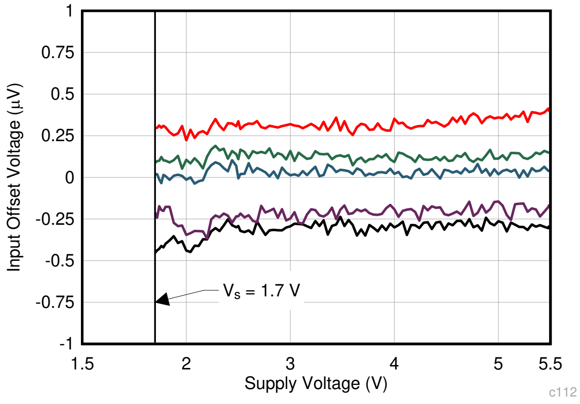


Figure 6-7. Offset Voltage vs Supply Voltage

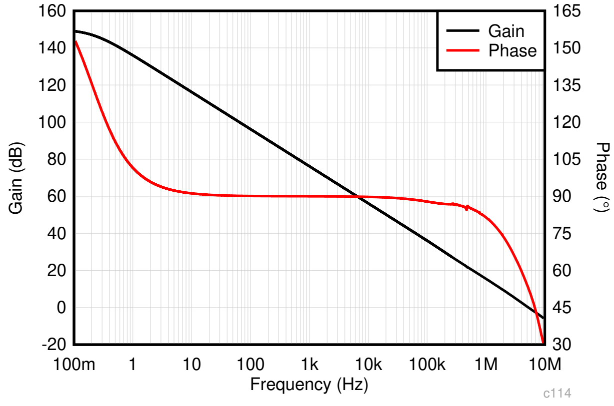


Figure 6-8. Open-Loop Gain and Phase vs Frequency

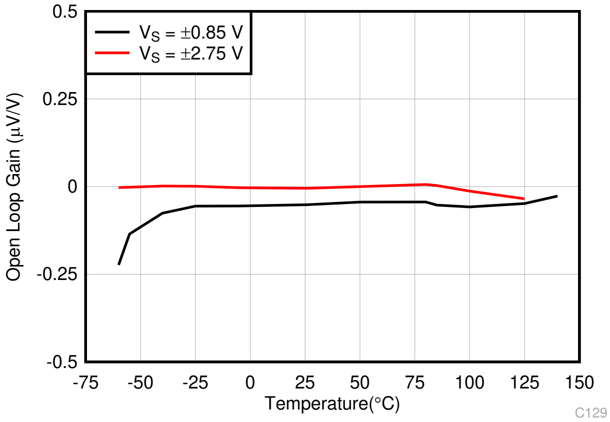


Figure 6-9. Open-Loop Gain vs Temperature

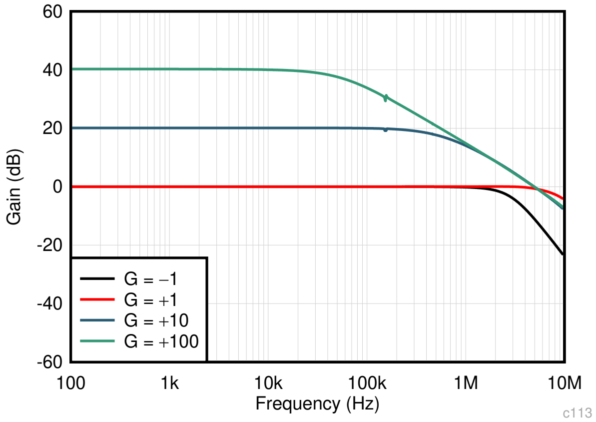


Figure 6-10. Closed-Loop Gain vs Frequency

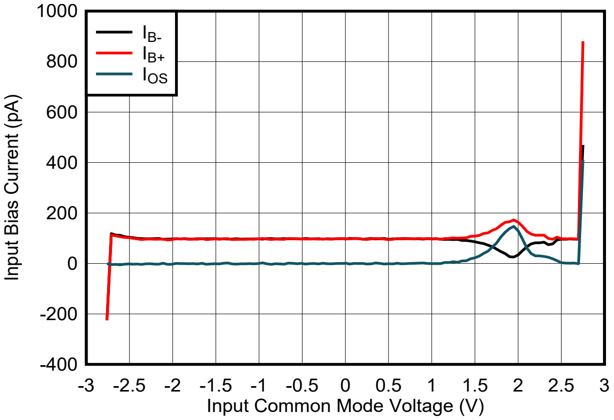


Figure 6-11. Input Bias Current vs Common-Mode Voltage

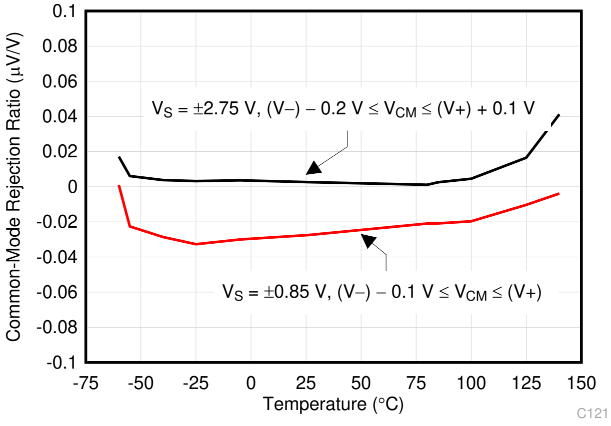


Figure 6-12. CMRR vs Temperature

6.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±2.75 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 50 pF (unless otherwise noted)

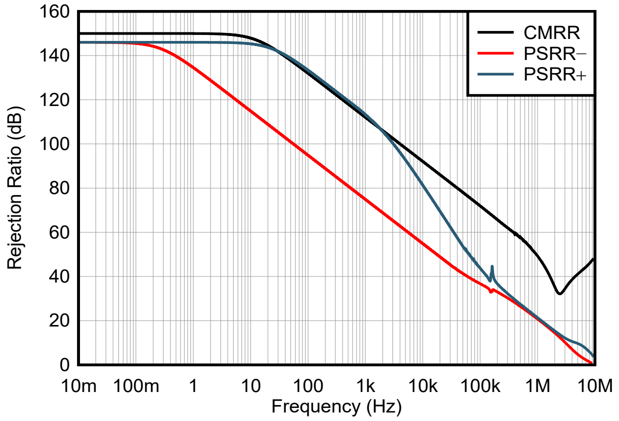


Figure 6-13. PSRR and CMRR vs Frequency

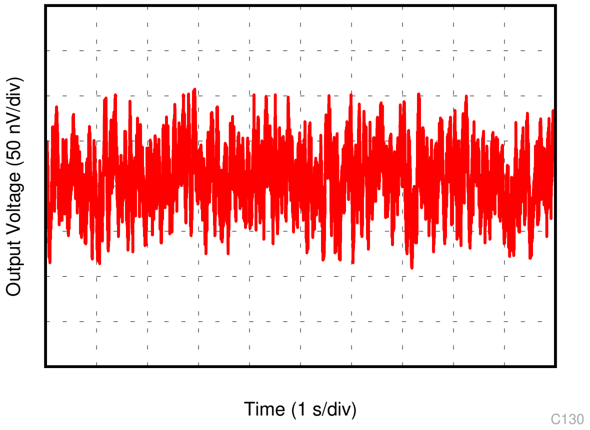


Figure 6-14. 0.1-Hz to 10-Hz Noise

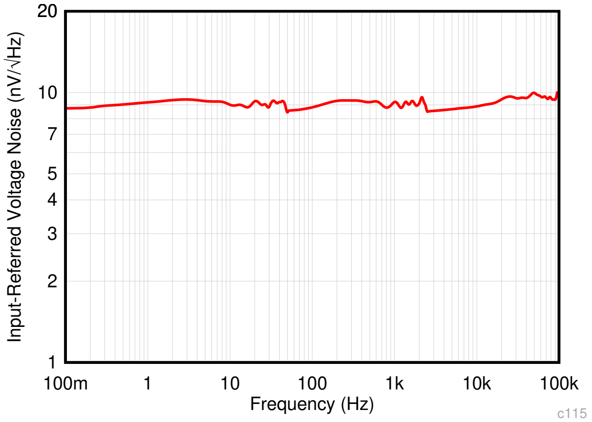


Figure 6-15. Input Voltage Noise Spectral Density vs Frequency

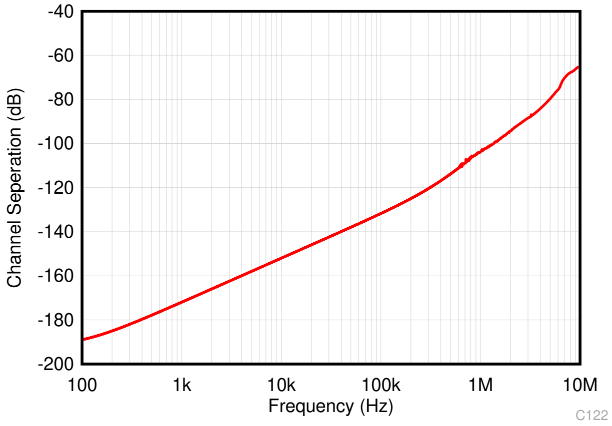
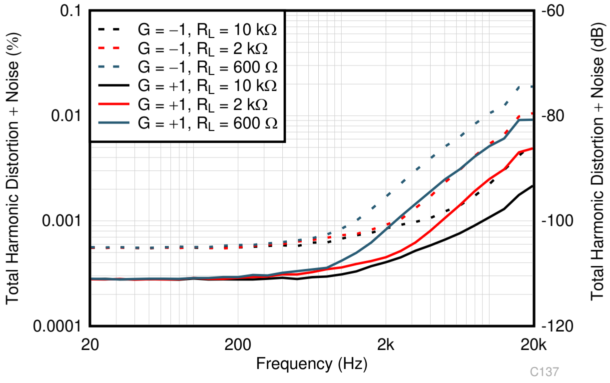
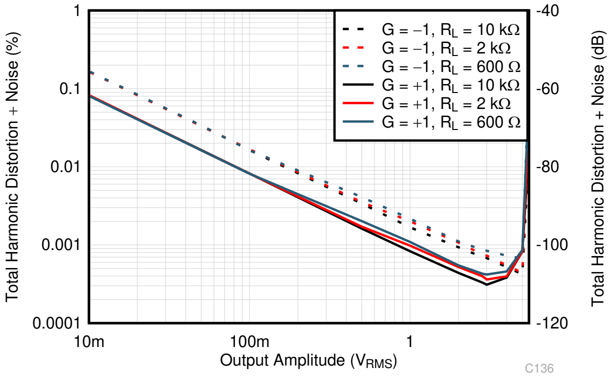


Figure 6-16. Channel-to-Channel Crosstalk



V_S = 5.5 V, V_{OUT} = 3 V_{RMS}, BW = 80 kHz

Figure 6-17. THD+N Ratio vs Frequency



V_S = 5.5 V, f = 1 kHz, BW = 80 kHz

Figure 6-18. THD+N vs Output Amplitude

6.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±2.75 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 50 pF (unless otherwise noted)

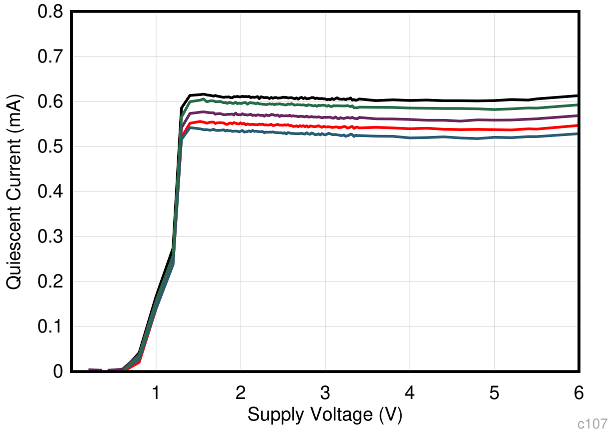


Figure 6-19. Quiescent Current vs Supply Voltage

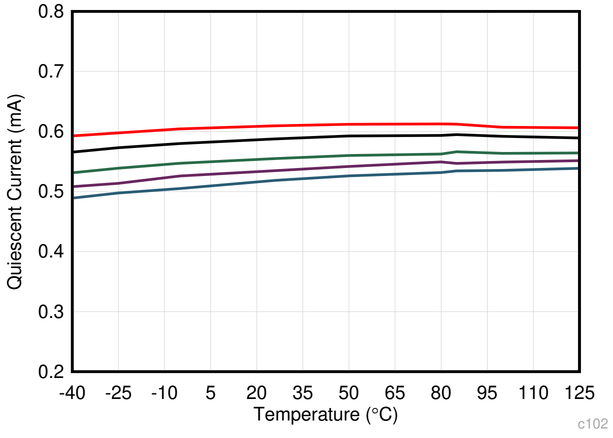


Figure 6-20. Quiescent Current vs Temperature

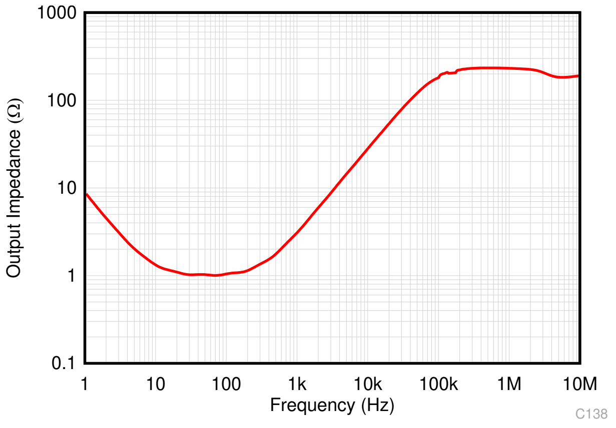
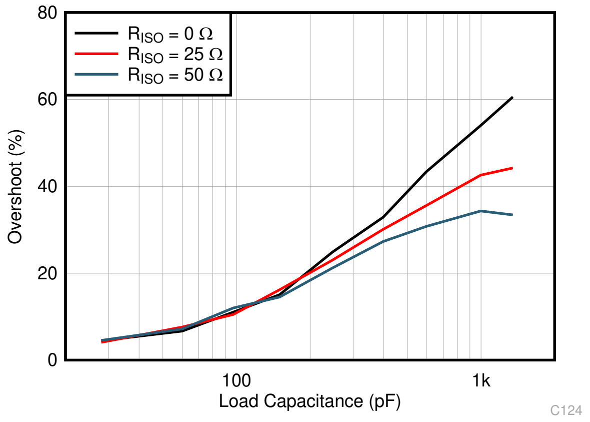
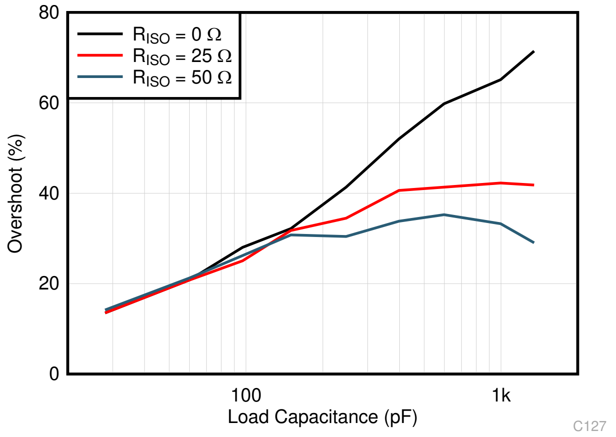


Figure 6-21. Open-Loop Output Impedance vs Frequency



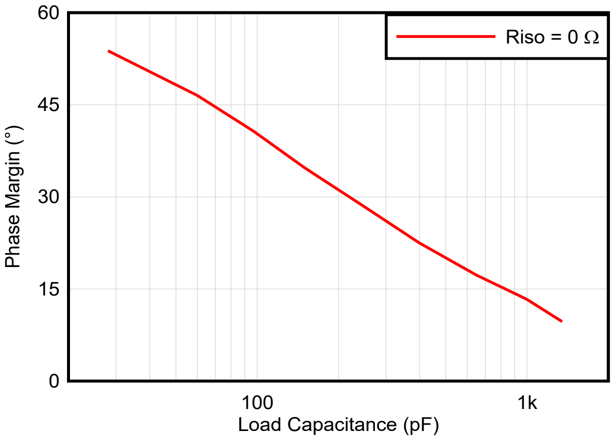
G = –1, 10 mV step

Figure 6-22. Small-Signal Overshoot vs Capacitive Load



G = +1, 10 mV step

Figure 6-23. Small-Signal Overshoot vs Capacitive Load



G = +1

Figure 6-24. Phase Margin vs Capacitive Load

6.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±2.75 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 50 pF (unless otherwise noted)

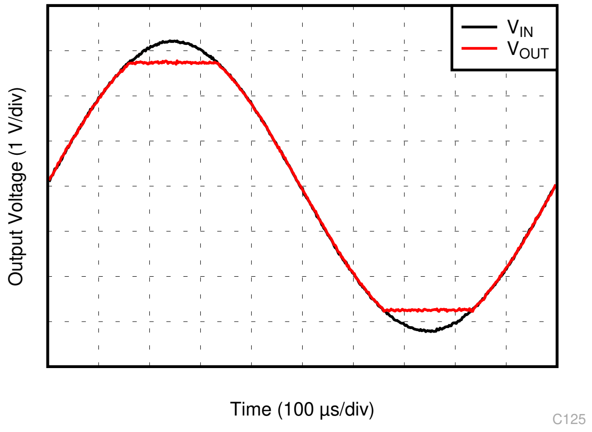
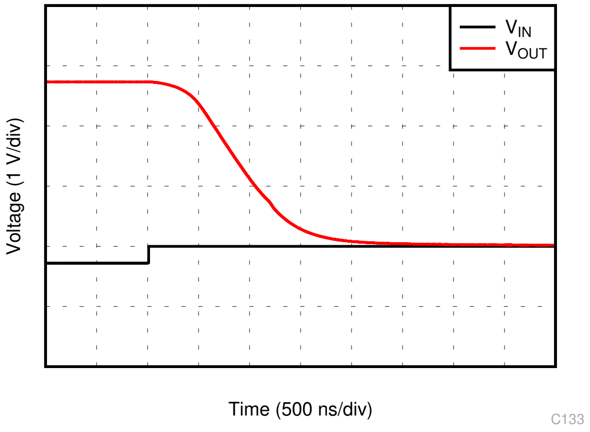
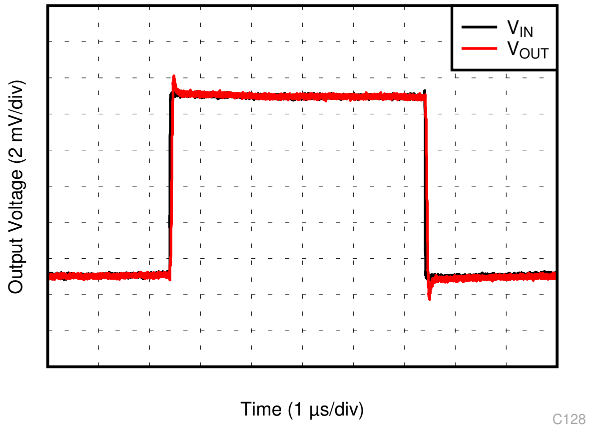


Figure 6-25. No Phase Reversal



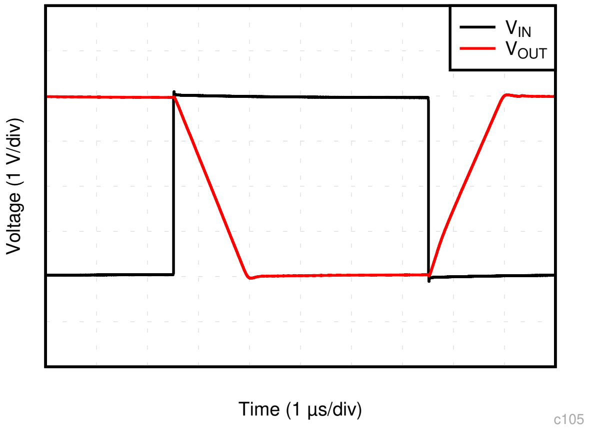
G = –1

Figure 6-26. Overload Recovery



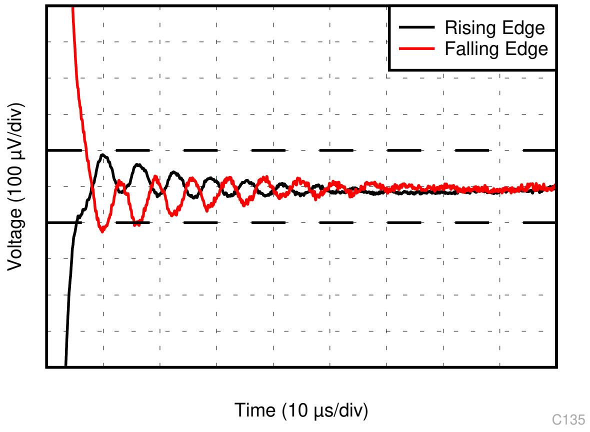
G = +1

Figure 6-27. Small-Signal Step Response



4-V step

Figure 6-28. Large-Signal Step Response



0.01% settling = ±100 µV

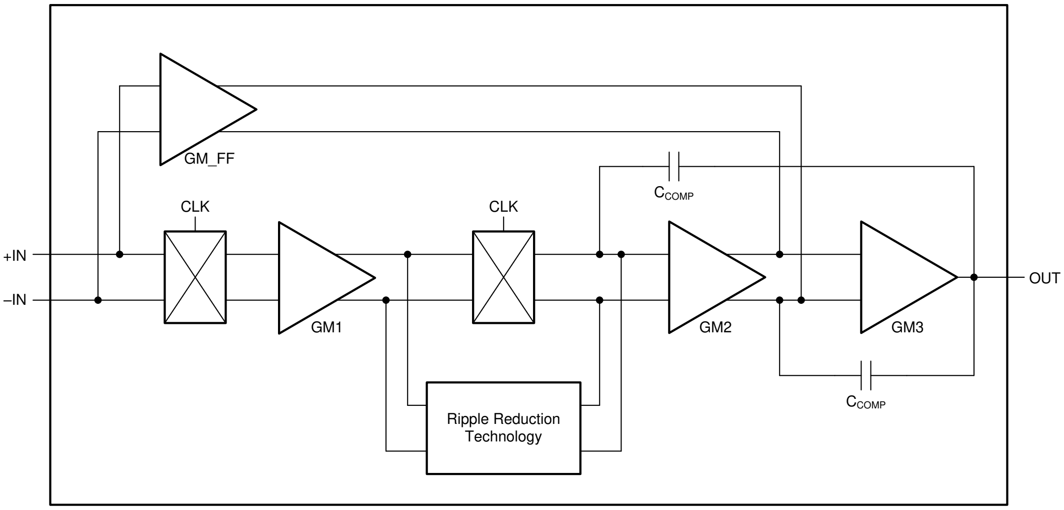
Figure 6-29. Settling Time

7 Detailed Description

7.1 Overview

The OPAx387 family of zero-drift amplifiers is engineered with state-of-the-art, proprietary, precision zero-drift technology. These amplifiers offer ultra-low input offset voltage and drift, and achieve excellent input and output dynamic linearity. The OPAx387 operate from 1.7 V to 5.5 V, are unity-gain stable, and are designed for a wide range of general-purpose and precision applications. The OPAx387 strengths also include a 5.7-MHz bandwidth, 8.5-nV/√Hz noise spectral density, and no 1/f noise, making the OPAx387 an excellent choice for interfacing with sensor modules, and buffering high-fidelity, digital-to-analog converters (DACs).

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Input Bias Current

During normal operation, the typical input bias current of the OPAx387 is 30 pA. The device exhibits low drift over the full temperature range of –40°C to +125°C. There are no antiparallel diodes between the input pins (+IN and –IN); therefore, the differential input maximum voltage is limited only by diodes connected to the supply voltage pins. However, use caution in cases where the input differential voltage exceeds the nominal operating input differential voltage. When inputs are separated, the switching offset-cancellation path internal to the amplifier exceeds normal operating conditions, and can potentially create long settling behavior upon return to normal operation. The equivalent input circuit of OPAx387 is shown in Figure 7-1.

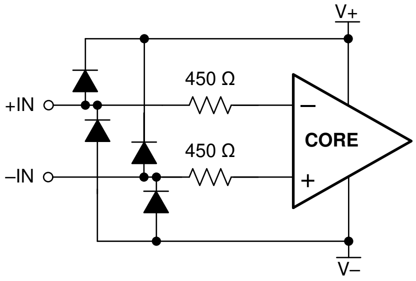


Figure 7-1. Equivalent Input Circuit

7.3.2 EMI Susceptibility and Input Filtering

Operational amplifiers can exhibit sensitivity to electromagnetic interference (EMI). Typically, conducted EMI (that is, EMI that enters the device through conduction) is more commonly observed than radiated EMI (that is, EMI that enters the device through radiation). When conducted EMI enters the operational amplifier, the dc offset at the amplifier output can shift from the nominal value. This shift is a result of signal rectification associated with the internal semiconductor junctions. Although all operational amplifier pin functions can be affected by EMI, the input pins are likely to be the most susceptible. The OPAx387 operational amplifier family incorporates an internal input low-pass filter that reduces the amplifier response to EMI. Both common-mode and differential-mode filtering are provided by the input filter. The conducted EMI rejection of the OPAx387 is seen in Figure 7-2.

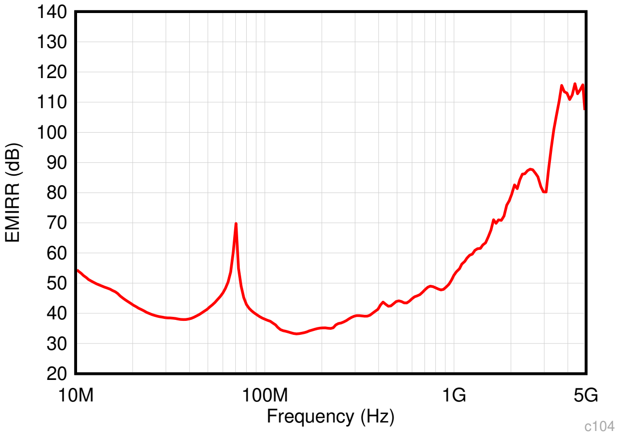


Figure 7-2. EMI Rejection Ratio

7.4 Device Functional Modes

The OPAx387 have a single functional mode and are operational when the power-supply voltage is greater than 1.7 V (±0.85 V). The maximum specified power-supply voltage for the OPAx387 is 5.5 V (±2.75 V).

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The OPAx387 are unity-gain stable, precision, operational amplifiers featuring state-of-the-art, zero-drift technology. The use of proprietary zero-drift circuitry gives the benefit of low input offset voltage over time and temperature, as well as lower 1/f noise component. As a result of the high PSRR, the devices work well in applications that run directly from battery power without regulation. The OPAx387 family is optimized for full rail-to-rail input, allowing for low-voltage, single-supply operation or split-supply use. These miniature, high-precision, low-noise amplifiers offer high-impedance inputs that have a common-mode range 100 mV beyond the supplies without input crossover distortion, and a rail-to-rail output that swings within 5 mV of the supplies under normal test conditions. The OPAx387 precision amplifiers are designed for upstream analog signal-chain applications in low or high gains, as well as downstream signal-chain functions, such as DAC buffering.

8.1.1 Zero-Drift Clocking

The OPAx387 use an advanced zero-drift architecture to achieve ultra-low offset and offset drift. This architecture uses a clock and switches internally to create a dc error-correction path. The clocking is filtered internally, and typically not observable for most configurations. Take the following precautions to minimize clock noise in the signal chain. The clocking creates a small charge-injection pulse at the input of the amplifier; therefore, do not use high-value resistors (> 100 kΩ) in series with the inputs to avoid higher clock voltage noise at the output. The charge injection pulses are minimized when the impedance to the input pins is matched. If higher value resistors are used, then use matching impedances on both amplifier input pins.

8.2 Typical Applications

8.2.1 Bidirectional Current Sensing

This single-supply, low-side, bidirectional current-sensing design example detects load currents from –1 A to +1 A. The single-ended output spans from 110 mV to 3.19 V. This design uses the OPAx387 because of the device low offset voltage and rail-to-rail input and output. One of the amplifiers is configured as a difference amplifier and the other amplifier provides the reference voltage. Figure 8-1 shows the design example schematic.

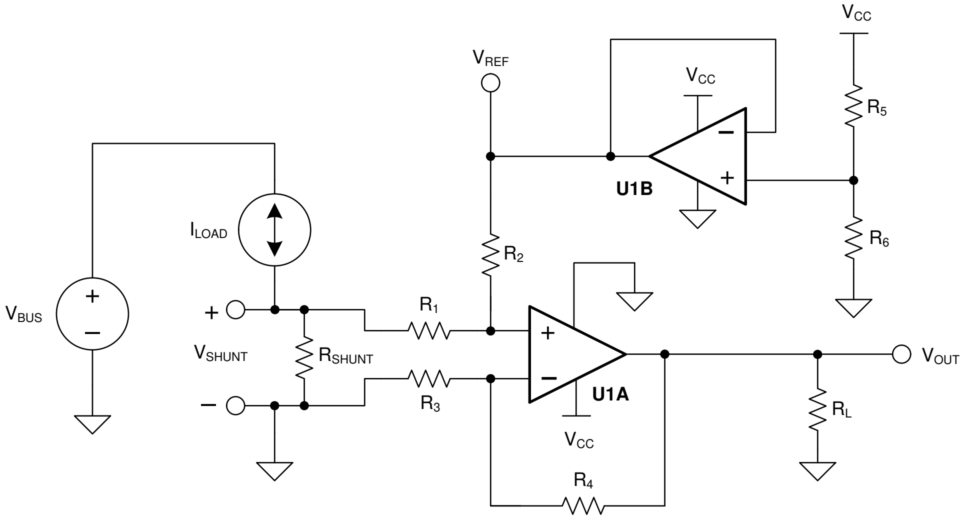


Figure 8-1. Bidirectional Current-Sensing Schematic

8.2.1.1 Design Requirements

This solution has the following requirements:

- Supply voltage: 3.3 V
- Input: –1 A to +1 A
- Output: 1.65 V ±1.54 V (110 mV to 3.19 V)

8.2.1.2 Detailed Design Procedure

The load current, I_{LOAD}, flows through the shunt resistor, R_{SHUNT}, to develop the shunt voltage, V_{SHUNT}. The shunt voltage is then amplified by the difference amplifier consisting of U1A and R_1 through R_4. The gain of the difference amplifier is set by the ratio of R_4 to R_3. To minimize errors, set $R_2 = R_4$ and $R_1 = R_3$. The reference voltage, V_{REF}, is supplied by buffering a resistor divider using U1B. The transfer function is given by Equation 1.

$$V_{OUT} = V_{SHUNT} \times Gain_{Diff\_Amp} + V_{REF} \tag{1}$$

where

- $V_{SHUNT} = I_{LOAD} \times R_{SHUNT}$
- $Gain_{Diff\_Amp} = \frac{R_4}{R_3}$
- $V_{REF} = V_{CC} \times \left(\frac{R_6}{R_5 + R_6}\right)$

There are two types of errors in this design: gain and offset. Gain errors are introduced by the tolerance of the shunt resistor and the ratios of R_4 to R_3 and, similarly, R_2 to R_1. Offset errors are introduced by the voltage divider (R_5 and R_6) and how closely the ratio of R_4 / R_3 matches R_2 / R_1. The latter value affects the CMRR of the difference amplifier, ultimately translating to an offset error.

The value of V_{SHUNT} is the ground potential for the system load because V_{SHUNT} is a low-side measurement. Therefore, a maximum value must be placed on V_{SHUNT}. In this design, the maximum value for V_{SHUNT} is set to 100 mV. Equation 2 calculates the maximum value of the shunt resistor given a maximum shunt voltage of 100 mV and maximum load current of 1 A.

$$R_{SHUNT(Max)} = \frac{V_{SHUNT(Max)}}{I_{LOAD(Max)}} = \frac{100\ \text{mV}}{1\ \text{A}} = 100\ \text{m}\Omega \tag{2}$$

The tolerance of R_{SHUNT} is directly proportional to cost. For this design, a shunt resistor with a tolerance of 0.5% was selected. If greater accuracy is required, select a 0.1% resistor or better.

The load current is bidirectional; therefore, the shunt voltage range is –100 mV to +100 mV. This voltage is divided down by R_1 and R_2 before reaching the operational amplifier, U1A. Make sure that the voltage present at the noninverting node of U1A is within the common-mode range of the device. Use an operational amplifier, such as the OPAx387, that has a common-mode range that extends below the negative supply voltage. The offset error is minimal because the OPAx387 has a typical offset voltage of merely ±0.25 μV (±5 μV, maximum).

Given a symmetric load current of –1 A to +1 A, the voltage divider resistors, R_5 and R_6, must be equal. To be consistent with the shunt resistor, a tolerance of 0.5% is selected. To minimize power consumption, 10-kΩ resistors are used.

To set the gain of the difference amplifier, the common-mode range and output swing of the OPAx387 must be considered. Equation 3 and Equation 4 depict the typical common-mode range and maximum output swing, respectively, of the OPAx387 given a 3.3-V supply.

$$-100\ \text{mV} < V_{CM} < 3.4\ \text{V} \tag{3}$$

$$100\ \text{mV} < V_{OUT} < 3.2\ \text{V} \tag{4}$$

The gain of the difference amplifier can now be calculated as shown in Equation 5.

$$\text{Gain}_{\text{Diff\_Amp}} = \frac{V_{\text{OUT\_Max}} - V_{\text{OUT\_Min}}}{R_{\text{SHUNT}} \times (I_{\text{MAX}} - I_{\text{MIN}})} = \frac{3.2\ \text{V} - 100\ \text{mV}}{100\ \text{m}\Omega \times [1\ \text{A} - (-\ 1\text{A})]} = 15.5\ \frac{\text{V}}{\text{V}} \tag{5}$$

The resistor value selected for R_1 and R_3 was 1 kΩ. 15.4 kΩ was selected for R_2 and R_4 because this number is the nearest standard value. Therefore, the ideal gain of the difference amplifier is 15.4 V/V.

The gain error of the circuit primarily depends on R_1 through R_4. As a result of this dependence, 0.1% resistors were selected. This configuration reduces the likelihood that the design requires a two-point calibration. A simple one-point calibration, if desired, removes the offset errors introduced by the 0.5% resistors.

8.2.1.3 Application Curve

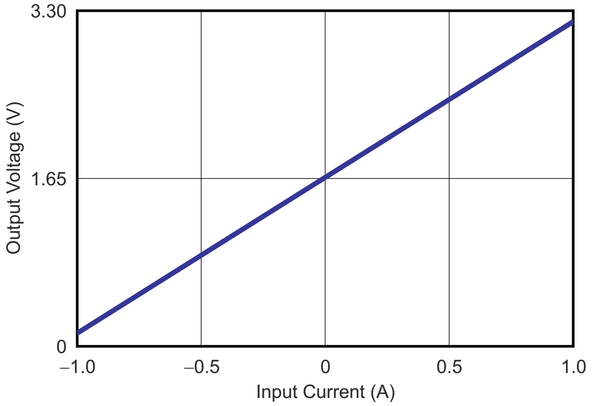


Figure 8-2. Bidirectional Current-Sensing Circuit Performance: Output Voltage vs Input Current

8.2.2 Load Cell Measurement

Figure 8-3 shows the OPAx387 in a high-CMRR dual-op amp instrumentation amplifier with a trim resistor and six-wire load cell for precision measurement.

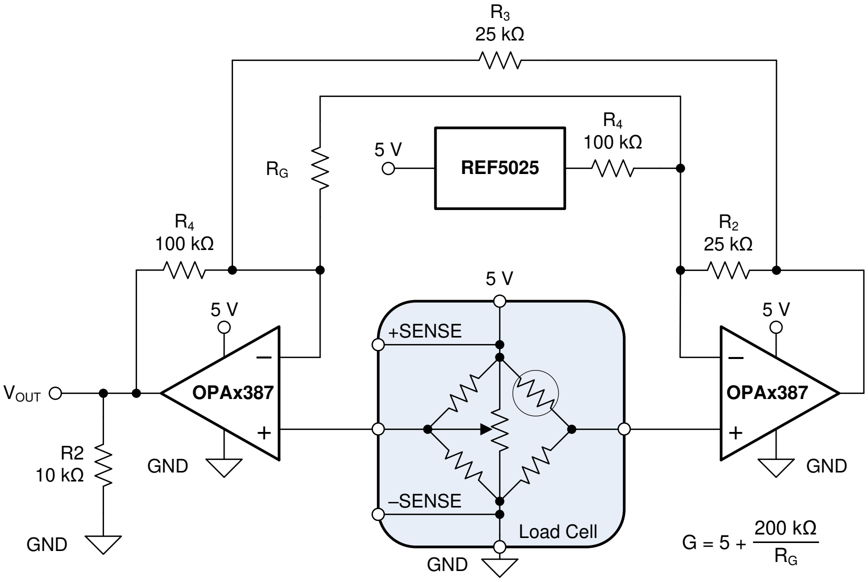


Figure 8-3. Load Cell Measurement Schematic

9 Power Supply Recommendations

The OPAx387 family of devices is specified for operation from 1.7 V to 5.5 V for single supplies, and ±0.85 V to ±2.75 V for dual supplies. Key parameters that can exhibit significant variance with regard to operating voltage are presented in Section 6.7.

CAUTION

Supply voltages greater than 6 V can permanently damage the device (see Section 6.1).

10 Layout

10.1 Layout Guidelines

Pay attention to good layout practice. Keep traces short and, when possible, use a printed-circuit board (PCB) ground plane with surface-mount components placed as close to the device pins as possible. Place a 0.1-µF capacitor close to the supply pins. These guidelines must be applied throughout the analog circuit to improve performance, and provide benefits such as reducing the electromagnetic interference (EMI) susceptibility.

For lowest offset voltage and precision performance, optimize circuit layout and mechanical conditions. Avoid temperature gradients that create thermoelectric (Seebeck) effects in the thermocouple junctions formed from connecting dissimilar conductors. Cancel these thermally-generated potentials by making sure that the potentials are equal on both input terminals. Other layout and design considerations include:

- Use low thermoelectric-coefficient conditions (avoid dissimilar metals).
- Thermally isolate components from power supplies or other heat sources.
- Shield operational amplifier and input circuitry from air currents, such as cooling fans.

Follow these guidelines to reduce the likelihood of junctions being at different temperatures, which can cause thermoelectric voltage drift of 0.1 µV/°C or higher depending on materials used.

10.2 Layout Example

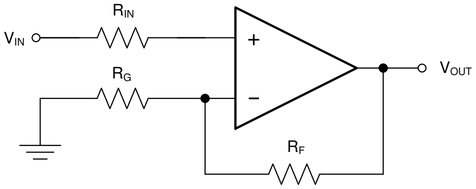


Figure 10-1. Schematic Representation

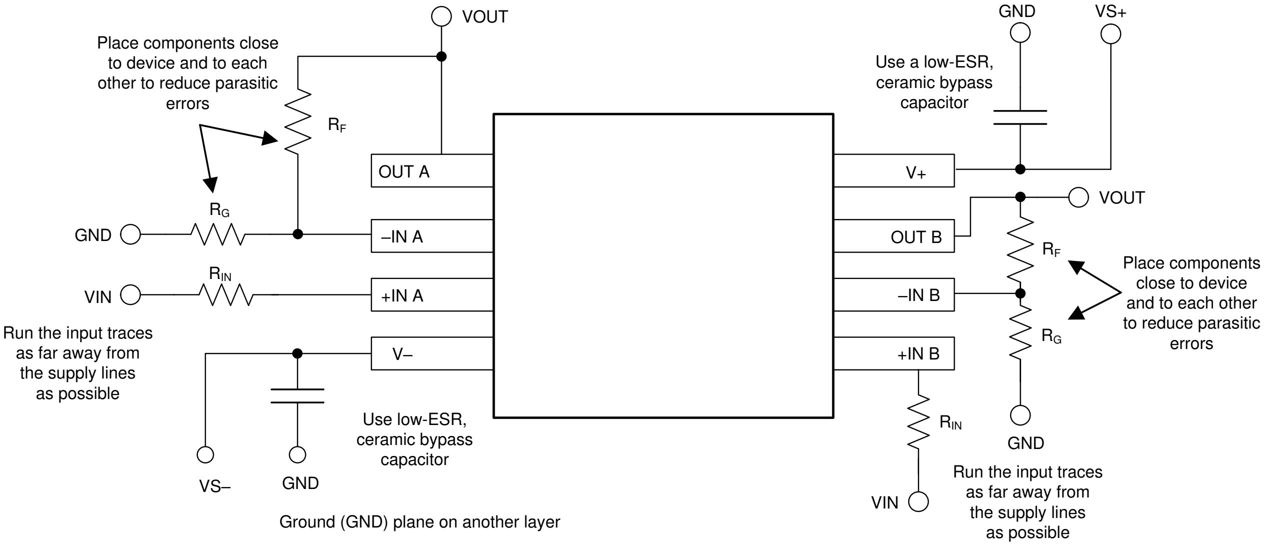


Figure 10-2. Layout Example

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 TINA-TI™ Simulation Software (Free Download)

TINA-TI™ simulation software is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI simulation software is a free, fully-functional version of the TINA™ software, preloaded with a library of macromodels, in addition to a range of both passive and active models. TINA-TI simulation software provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Analog eLab Design Center, TINA-TI simulation software offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

Note

These files require that either the TINA software or TINA-TI software be installed. Download the free TINA-TI simulation software from the TINA-TI™ software folder.

11.1.1.2 PSpice® for TI

PSpice® for TI is a design and simulation environment that helps evaluate performance of analog circuits. Create subsystem designs and prototype solutions before committing to layout and fabrication, reducing development cost and time to market.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following: Texas Instruments, *Circuit board layout techniques*

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.5 Trademarks

TINA-TI™ and TI E2E™ are trademarks of Texas Instruments.
TINA™ is a trademark of DesignSoft, Inc.
PSpice® is a registered trademark of Cadence Design Systems, Inc.
All trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2387DGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	2B2T	Samples
OPA2387DGKT	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	2B2T	Samples
OPA387DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	2IMT	Samples
OPA387DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	2IMT	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

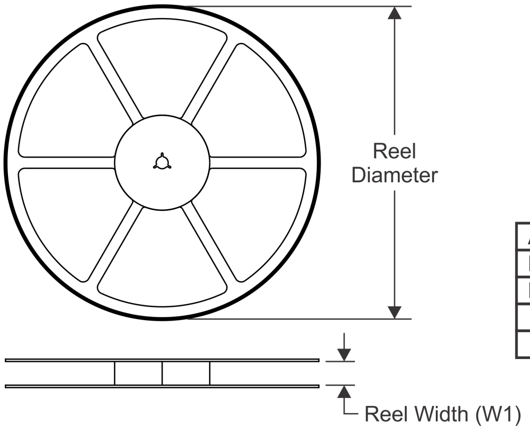
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

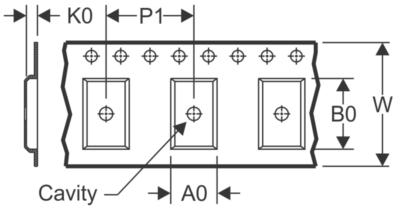
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

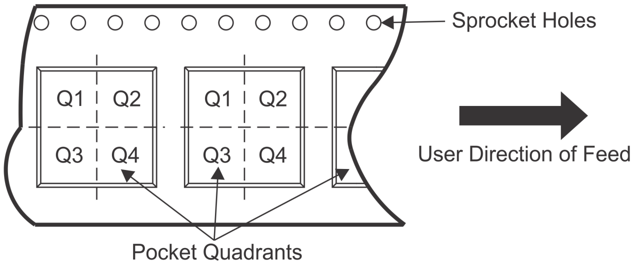


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

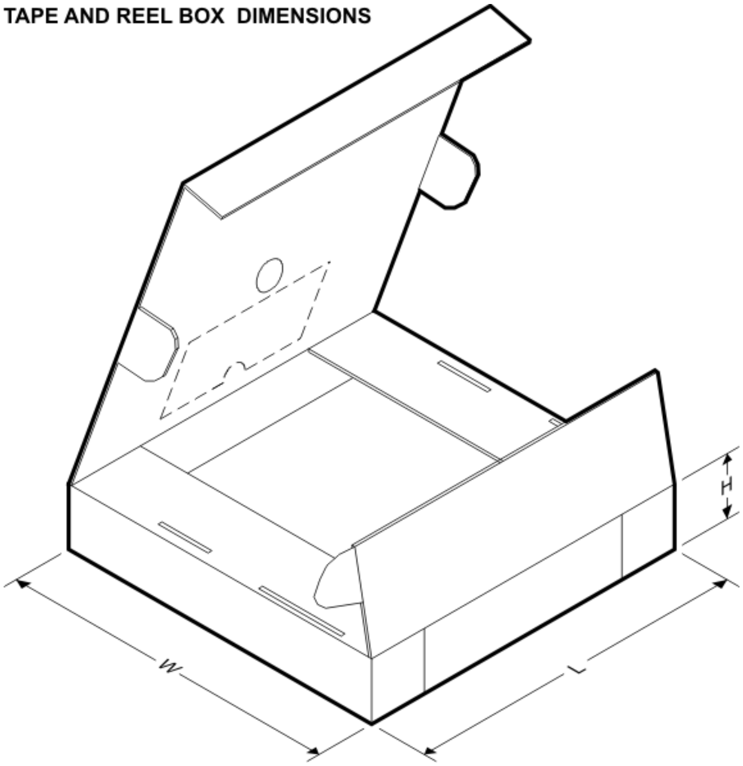
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

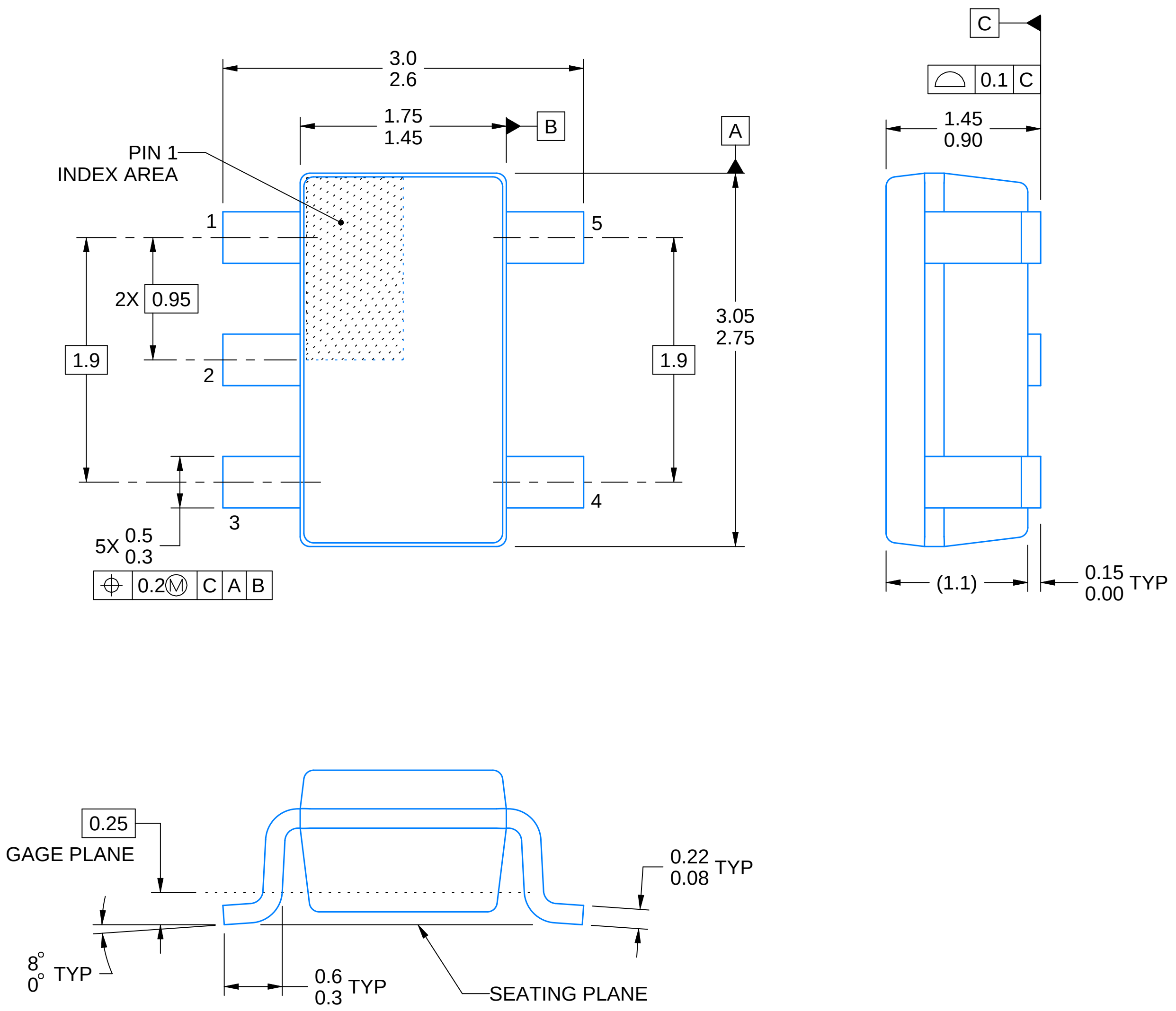
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2387DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2387DGKT	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA387DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
OPA387DBVT	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

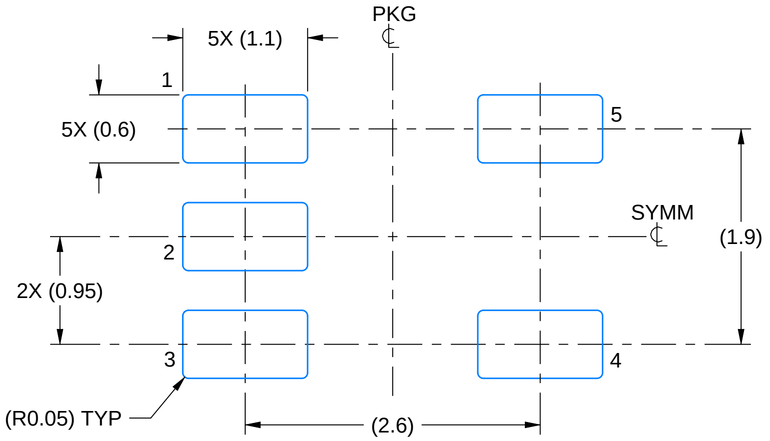
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2387DGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
OPA2387DGKT	VSSOP	DGK	8	250	366.0	364.0	50.0
OPA387DBVR	SOT-23	DBV	5	3000	190.0	190.0	30.0
OPA387DBVT	SOT-23	DBV	5	250	190.0	190.0	30.0



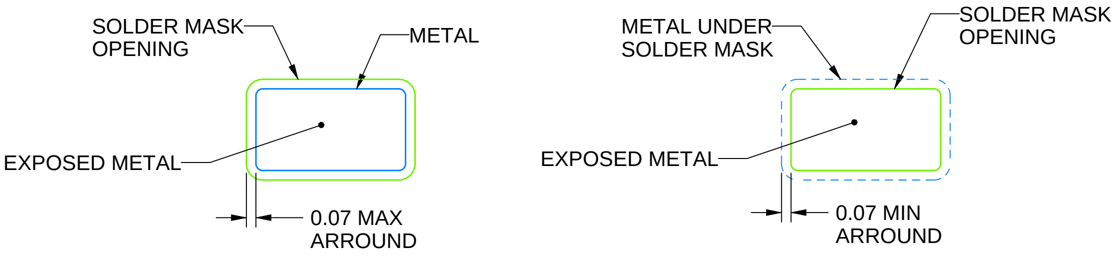
4214839/F 06/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



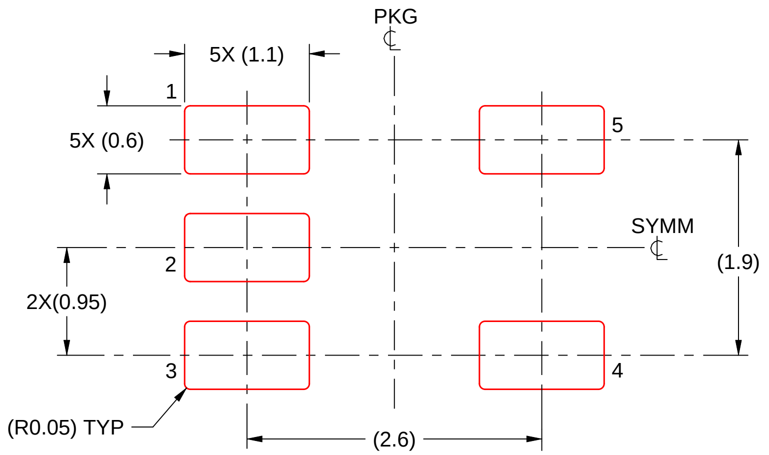
NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

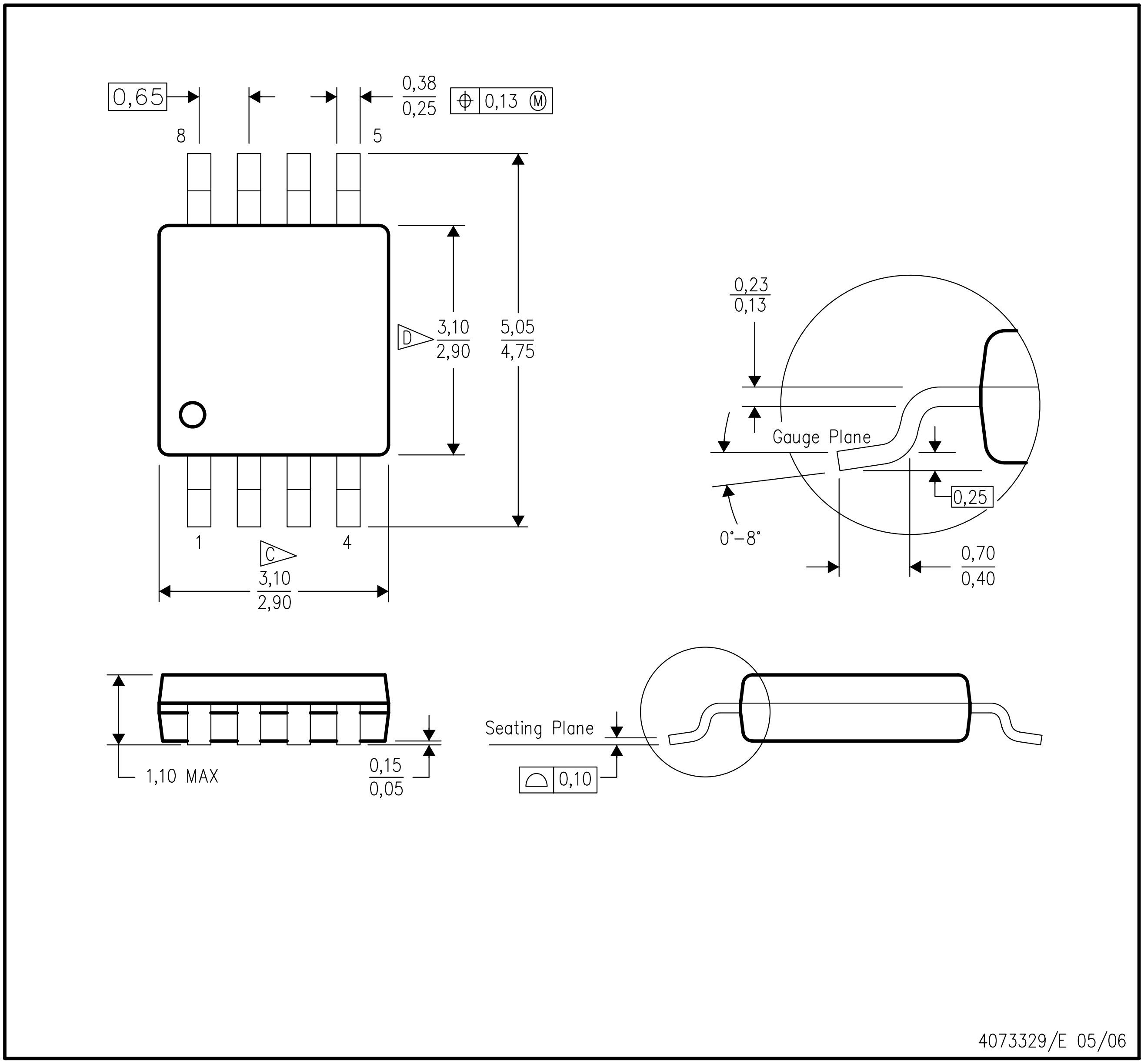


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

NOTES: (continued)

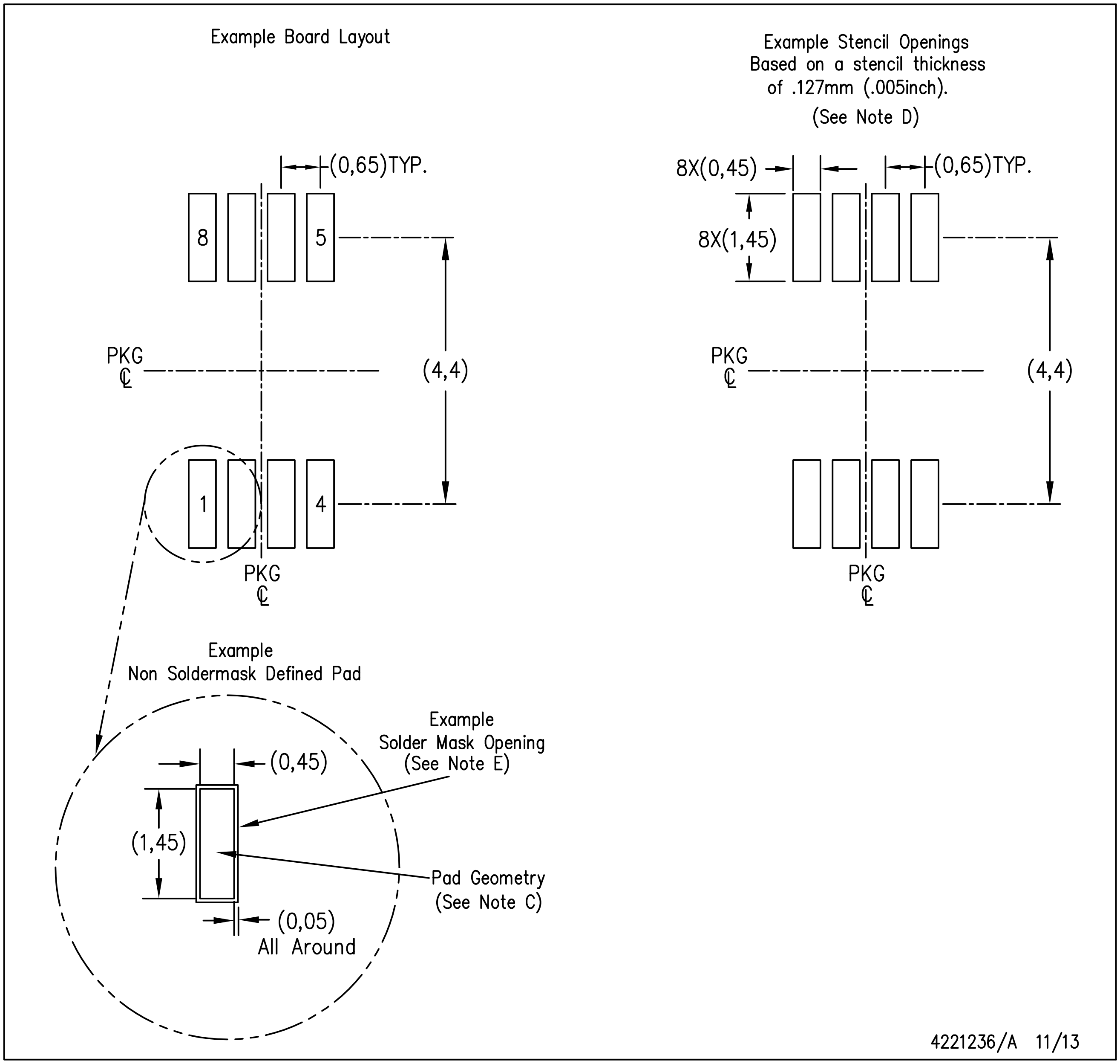
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DGK (S-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C▷ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D▷ Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO-187 variation AA, except interlead flash.

DGK (S-PDSO-G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2021, Texas Instruments Incorporated