SN74LVC1G32

General Description

This single 2-input positive- OR gate is designed for 1.65-V to 5.5-V V_{CC} operation.

The SN74LVC1G32 performs the Boolean function. Y=A+B or $Y=\overline{A}\cdot\overline{B}$ .in positive logic. The CMOS device has high output drive while maintaining low static power dissipation over a broad V_{CC} operating range.The SN74LVC1G32 device is available in a variety of packages.

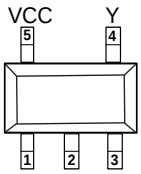
Features

- Operate from1.65V to 5.5V
- Supports 5-V VCC operation
- Specified from-40°C to 85°C
- Provides down translation to V_{CC}
- Max t_{pd} of 3.8 ns at 3.3V
- ±24-mA output drive at 3.3V

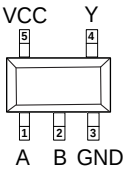
Applications

- Personal navigation device(GPS)
- AV receiver
- High-speed data acquisition and generation
- SSD:internal and external
- Digital picture frame(DPF)
- TV:LCD/digital and high-definition(HDTV)

Reference News

Pinning and Package	Marking
	

SOT-23-5

Pinning and Package	Marking
	

SC70-5

Pin Functions

Pin		Type	Description
Name	SOT23-5/SC70-5		
A	1	I	Data Input
B	2	I	Data Input
GND	3	-	Ground
Y	4	O	Data Output
V_{CC}	5	-	Supply Voltage

Order information

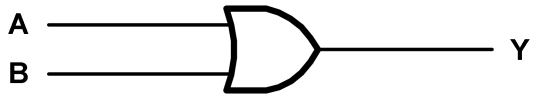
Orderable Device	Package	Packing Option
SN74LVC1G32DBVR	SOT23-5	3000PCS
SN74LVC1G32DCKR	SC70-5	3000PCS

Absolute Maximum Ratings

Parameters			Min	Max.	Unit
V_{CC}	Supply voltage range		-0.5	6.5	V
V_I	Input voltage range		-0.5	6.5	V
V_O	Voltage range applied to any output in the high-impedance or power-off state		-0.5	6.5	V
V_O	Voltage range applied to any output in the high or low state		-0.5	V_{CC}+0.5	V
I_{IK}	Input clamp current	V_I<0		-50	mA
I_{OK}	Output clamp current	V_O<0		-50	mA
I_O	Continuous output current			±50	mA
Continuous current through V_{CC} or GND				±100	mA
T_J	Junction temperature under bias		-40	85	℃
T_{stg}	Storage temperature range		-55	150	℃

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

Functional Block Diagram



ESD Ratings

ESD			Value	Unit
V(ESD)	Electrostatic Discharge	Human-Body Model (HBM)(1)	8 K	V
		Charged-Device Model (CDM)(2)	1.5K	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
SOT23-5	250	81	°C/W
SC70-5	400	150	°C/W

Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating	1.65	5.5	V
V_{IH}	High-Level Input Voltage	V_{CC}=1.65V to 1.95V	0.65×V_{CC}		V
		V_{CC}=2.3V to 2.7V	1.7		
		V_{CC}=3V to 3.6V	2		
		V_{CC}=4.5V to 5.5V	0.7×V_{CC}		
V_{IL}	Low-Level Input Voltage	V_{CC}=1.65V to 1.95V		0.35×V_{CC}	V
		V_{CC}=2.3V to 2.7V		0.7	
		V_{CC}=3V to 3.6V		0.8	
		V_{CC}=4.5V to 5.5V		0.3×V_{CC}	
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage		0	V_{CC}	V
I_{OH}	High-Level Output Current	V_{CC}=1.65V		-4	mA
		V_{CC}=2.3V		-8	
		V_{CC}=3V		-16	
				-24	
		V_{CC}=4.5V		-32	
I_{OL}	Low-Level Output Current	V_{CC}=1.65V		4	mA
		V_{CC}=2.3V		8	
		V_{CC}=3V		16	
				24	
		V_{CC}=4.5V		32	
Δt/Δv	Input Transition Rise or Fall Rate	V_{CC}=1.8V±0.15V, 2.5V±0.2V		20	ns/V
		V_{CC}=3.3V±0.3V		10	
		V_{CC}=5V±0.5V		5	
TA	Operating Free-air Temperature	All Other Packages	-40	85	°C

(1) All unused digital inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

Electrical Characteristics

V_{CC}=1.65V to 5.5V, FULL=–40°C to +85°C. Typical values are at TA=+25°C (unless otherwise noted)

Parameter	Symbol	Test Conditions	Vcc	TA	Min	Typ	Max	Units
Output								
Output High Voltage	V_{OH}	I_{OH}=–100μA	1.65V to 5.5V	FULL	V_{CC}-0.1			V
		I_{OH}=–4mA	1.65V	FULL	1.2			V
		I_{OH}=–8mA	2.3V	FULL	1.9			V
		I_{OH}=–16mA	3V	FULL	2.4			V
		I_{OH}=–24mA		FULL	2.3			V
		I_{OH}=–32mA	4.5V	FULL	3.8			V
Output Low Voltage	V_{OL}	I_{OL}=100μA	1.65V to 5.5V	FULL			0.1	V
		I_{OL}=4mA	1.65V	FULL			0.45	V
		I_{OL}=8mA	2.3V	FULL			0.3	V
		I_{OL}=16mA	3V	FULL			0.4	V
		I_{OL}=24mA		FULL			0.65	V
		I_{OL}=32mA	4.5V	FULL			0.65	V
Off-State Current	I_{off}	V_I or V_O=5.5V	0V	FULL			±25	μA
Input								
Input Leakage Current	I_I	V_I=5.5V or GND	0V to 5.5V	FULL			±5	μA
Input Capacitance	C_I	V_I=V_{CC} or GND	3.3V	FULL		4		pF
Power Supply								
Power Supply Range	V_{CC}		1.65V to 5.5V	FULL	1.65		5.5	V
Power Supply Current	I_{CC}	V_I=V_{CC} or GND, I_O=0	5.5V	FULL			10	μA
Delta Power Current	ΔI_{CC}	One Input at V_{CC} – 0.6V, Other Inputs at V_{CC} or GND	3V to 5.5V	FULL			500	μA

1) All unused digital inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

Switching Characteristics

Over recommended operating free-air temperature range,C_L=30pF or 50 pF (unless otherwise noted)

Parameter	From(Input)	To(Output)	–40°C to +85°C								Units
			V_{CC}=1.8V±0.15V		V_{CC}=2.5V±0.2V		V_{CC}=3.3V±0.3V		V_{CC}=5V±0.5V		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{pd}	A or B	Y	1	9	1	3.8	1	3.8	1	3.3	ns

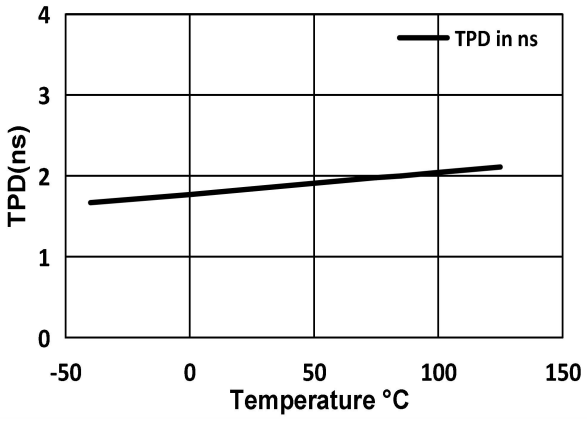
Operating Characteristics

TA=- 40°C to +85°C

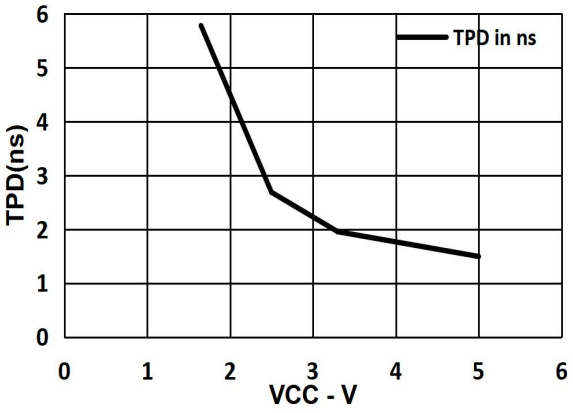
Parameter		Test Conditions	Vcc=1.8V	Vcc=2.5V	Vcc=3.3V	Vcc=5V	Units
			Typ	Typ	Typ	Typ	
C_{pd}	Power Dissipation Capacitance	f=10Mhz	23	23	23	29	pF

Typical Characteristics

V_{CC}=1.65V or 5.5V, FULL=–40°C to +85°C. Typical values are at TA=+25°C (unless otherwise noted)

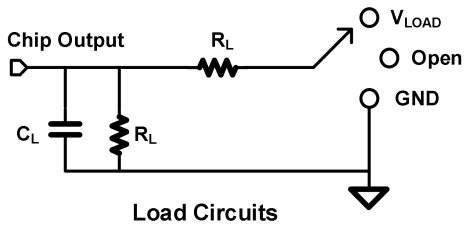


TPD Across Temperature at 3.3V V_{CC}



TPD Across V_{CC} at 25℃

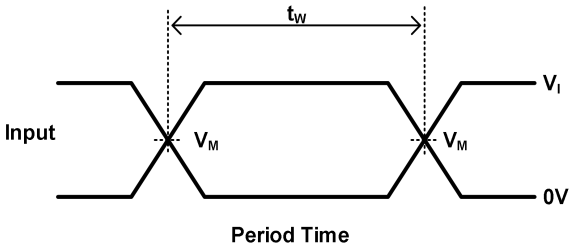
Parameter Measurement Information



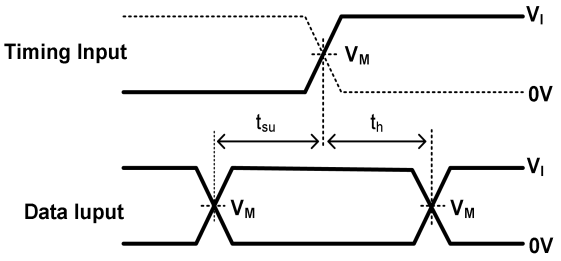
TEST	S1
T_{PHL}/T_{PLH}	OPEN
T_{PLZ}/T_{PZL}	V_{LOAD}
T_{PHZ}/T_{PZH}	GND

Vcc	INPUTS		VM	VLOAD	CL	RL	V△
	VI	Tr/Tf					
1.8V±0.15V	Vcc	≤2ns	Vcc/2	2×Vcc	30pF	500Ω	0.15V
2.5V±0.15V	Vcc	≤2ns	Vcc/2	2×Vcc	30pF	500Ω	0.15V
3.3V±0.15V	3V	≤2.5ns	1.5V	6V	50pF	500Ω	0.3V
5V±0.15V	Vcc	≤2.5ns	Vcc/2	2×Vcc	50pF	500Ω	0.3V

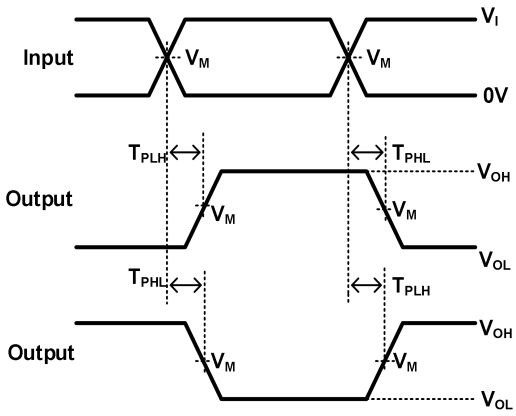
Parameter Measurement Information(Continued)



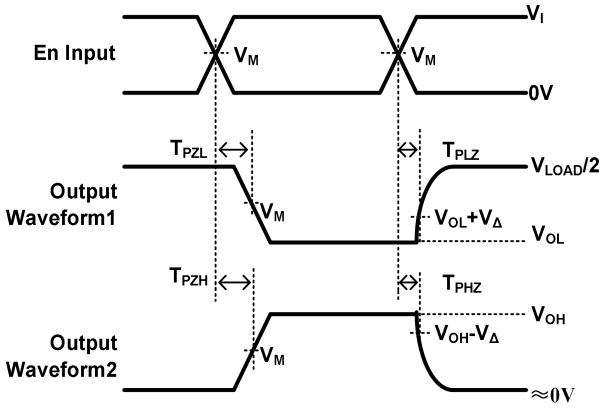
Period Time



Setup and Hold Times



Propagation Delay
for Output and Inverted Output



Enable and Disable Times
Low-And High-Level Enabling

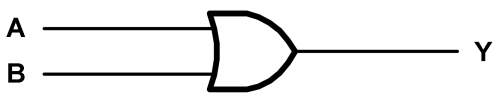
Notes: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR 10 MHz, Z =50.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all device.

Detailed Description

Overview

The SN74LVC1G32 device contains one 2-input positive OR gate device and performs the Boolean function $Y = A + B$ or $Y = \overline{\overline{A} \cdot \overline{B}}$. This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitrydisables the outputs, preventing damaging current backflow through the device when it is powered down. The I_{off} feature allows voltages on the inputs and outputs, when V_{CC} is 0 V.

Functional Block Diagram



Feature Description

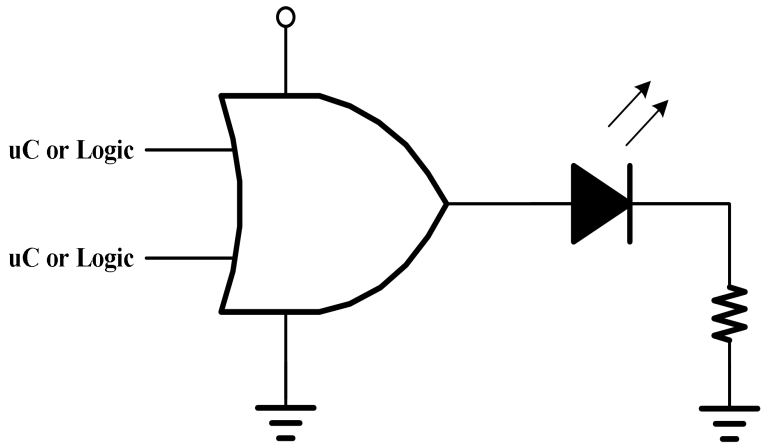
- Wide operating voltage range.
- Operates from 1.65 V to 5.5 V.
- Allows down voltage translation.
- Inputs accept voltages to 5.5 V.
- I_{off} feature allows voltages on the inputs and outputs, when V_{CC} is 0 V.

Device Functional Modes

Inputs		Output
A	**B**	**Y**
H	X	L
X	H	L
L	L	H

Application Note

The SN74LVC1G32 is a high drive CMOS device that can be used for implement OR logic with a high output drive, such as an LED application. It can produce 24-mA of drive current at 3.3V making it Ideal for driving multiple outputs and good for high speed applications up to 100Mhz The inputs are 5 5-V tolerant allowing translation down to V_{CC}



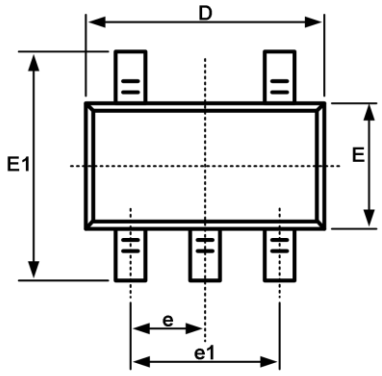
Basic LED Driver

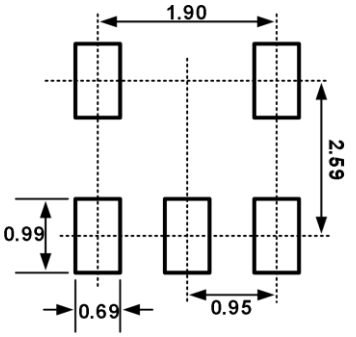
This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads, so routing and load conditions should be considered to prevent ringing.

Each VCC pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1-μF capacitor is recommended. If there are multiple VCC pins, then a 0.01-μF or 0.022-μF capacitor is recommended for each power pin. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. A 0.1-μF and 1-μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

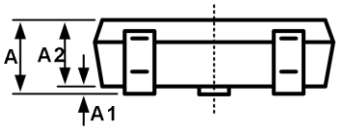
Package Outline

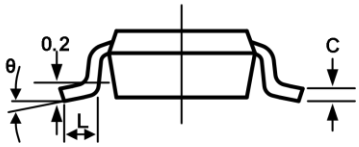
SOT23-5





Recommended Land Pattern (Unit: mm)

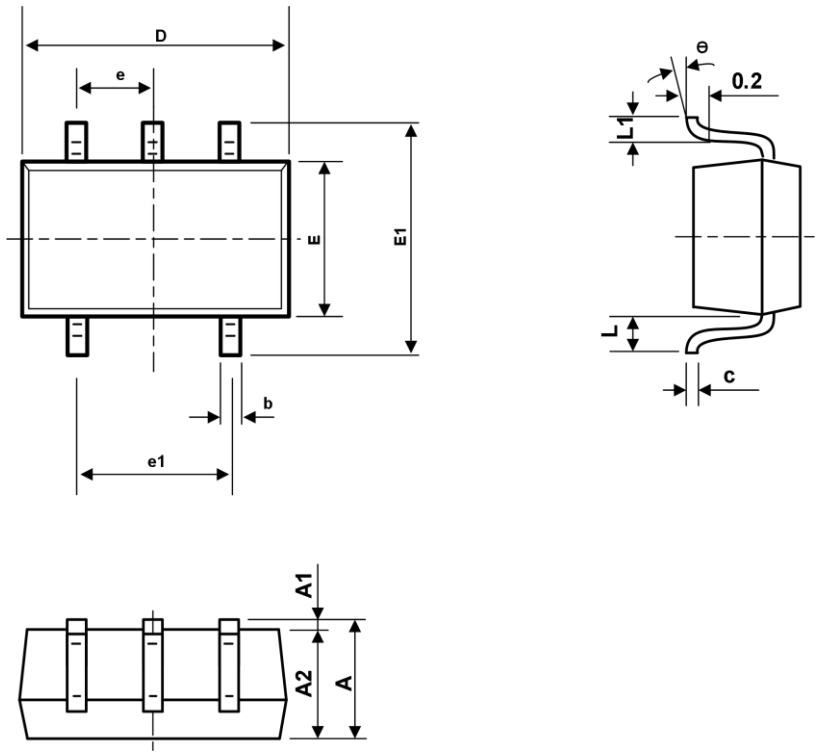




Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950BSC		0.037BSC	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
L1	0.600REF		0.024REF	
θ	0°	8°	0°	8°

Package Outline

SC70-5



symbol	Dimension In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.900	1.100	0.035	0.043
A1	0.000	0.100	0.000	0.004
A2	0.900	1.000	0.035	0.039
b	0.150	0.350	0.006	0.014
c	0.110	0.175	0.004	0.007
D	2.000	2.200	0.079	0.087
E	1.150	1.350	0.045	0.053
E1	2.150	2.450	0.085	0.096
e	0.650TYP		0.026TYP	
e1	1.200	1.400	0.047	0.055
L	0.525REF		0.021REF	
L1	0.260	0.460	0.010	0.018
θ	0°	8°	0°	8°