TP6815ND6

High Efficiency 1.2MHz, 1.5A Synchronous Step Down Regulator

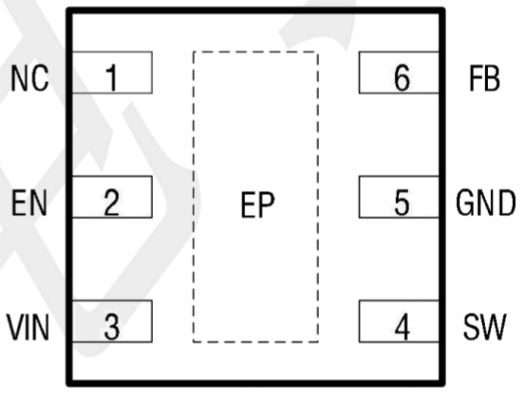
Features

- Supply Voltage Range: 2.3V to 6.0V
- Guaranteed 1.5A continuous load current
- 2% 0.6V reference
- Cycle-by-cycle peak current limitation
- PFM Mode for High Efficiency in Light Load
- 100% Duty Cycle in Dropout Operation
- Low RDS(ON) for internal switches (top/bottom):300/300 mΩ
- Fixed 1.2MHz Switching Frequency
- Efficiency Up to 96%
- Slope Compensated Current Mode Control for Excellent Line and Load Transient Response
- <1μA Shutdown Current
- RoHS and Halogen free compliance
- Compact package: DFN-6(2X2)

Applications

- Networking
- IP CAM
- LCD TV
- DSL Modem
- Access Point Router
- Digital TV
- Set Top Box

Pinout (top view)



DFN-6(2X2)

Pin Configurations

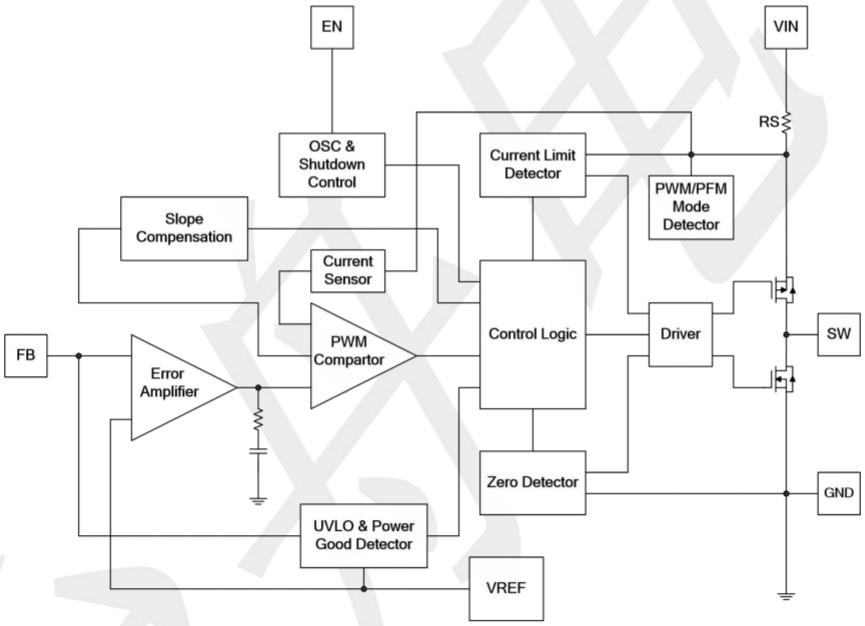
Pin Number	Pin Name	Pin Function
1	NC	No Internal Connection
2	EN	Chip Enable Pin. Drive EN above 1.5V to turn on the part. Drive EN below 0.3V to turn it off. Do not leave EN floating.
3	VIN	Power Supply Input.Must be closely decoupled to GND with a 10μF or greater ceramic capacitor.
4	SW	Power Switch Output. It is the switch node connection to Inductor. This pin connects to the drains of the internal P-ch and N-ch MOSFET switches.
5	GND	Analog ground pin.
6	FB	Output Voltage Feedback Pin. An internal resistive divider divides the output voltage down for comparison to the internal reference voltage.

Absolute Maximum Ratings

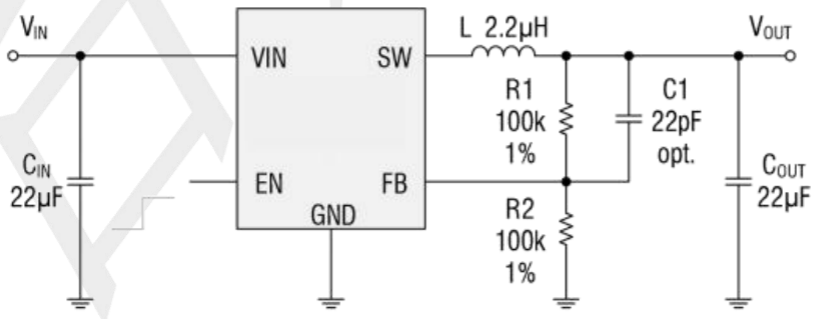
over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
VIN	Continuous input voltage range	-0.3	6.5	V
SW	SW voltage range	-0.3	VIN+0.3V	
EN	EN pin voltage range	-0.3	6.5	
FB	FB, pin voltage range	-0.3	6.5	
PD	PD @ TA = 25°C	0.8		W
LT	Lead Temperature (Soldering, 10 sec.)	260		℃
Temperature	Junction Temperature , TJ	-40	125	
	Storage, Tstg	-65	150	
θJA	Thermal Resistance from Junction to ambient	115		°C/W

BLOCK DIAGRAM



Typical Application Circuit



Electrical Characteristics

(V_{IN}=V_{EN}=3.6V, V_{OUT}=1.8V, T_A = 25°C, unless otherwise noted.)

PARAMETER	SYMBOL	TEST Conditions	MIN	TYP	MAX	UNIT
Supply Voltage	V_{IN}		2.3	--	6.0	V
UVLO Threshold	UVLO		1.7	1.9	2.1	V
OVP	OVP		--	6.5	--	V
Quiescent Current	I_Q	V_{EN}=3.0V	--	25	50	uA
Shutdown Current	I_{SHDN}	V_{EN}=0, V_{IN}=4.2V	--	0.1	1.0	uA
Feedback Reference Voltage	V_{FB}	T_A = 25°C	0.588	0.6	0.612	V
Top FET RON	$R_{DS(ON)1}$	V_{IN}= 5V,I_{SW}=100mA	--	300	450	mΩ
Bottom FET RON	$R_{DS(ON)2}$	V_{IN}= 5V,I_{SW}=-100mA	--	300	450	mΩ
TOP FET Peak Current Limit	$I_{LIM,TOP}$	V_{IN}= 3V, V_{OUT}=90%	--	2.2	--	A
Bottom FET Valley Current Limit	$I_{LIM,BOTTOM}$	V_{IN}= 3V, V_{OUT}=90%	--	2.2	--	A
EN Threshold	V_{IL}	Low Voltage	--	--	0.4	V
	V_{IH}	High Voltage	1.5	--	--	V
EN Input Current	I_{SINK}	VEN From 0V to 2V	--	1	--	uA
Switching Frequency	F_{SW}	IOUT =100%	--	1.2	--	MHz
		IOUT =0	--	300	--	KHz
SW Leakage Current		VEN=0V,VIN=VSW=5.5V	--	±0.01	±1	uA
Soft-start Time	t_{SS}		--	1.0	--	mS
Operating Temperature Range	TA		-40	--	85	℃

Note 1. Stresses beyond “Absolute Maximum Ratings” may cause permanent damage to the evice.These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

2. The device is not guaranteed to function outside its operating conditions.

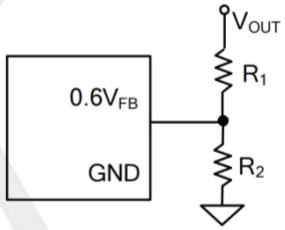
Function Description

Because of the high integration in the IC,the application circuit based on this regulator IC is rather simple. Only input capacitor CIN, output capacitor COUT, output inductor L and feedback resistors (R1 and R2) need to be selected for the targeted applications specifications.

Feedback resistor dividers R1 and R2

Choose R1 and R2 to program the proper output voltage. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both R1 and R2. A value of between 10kΩ and 1MΩ is highly recommended for both resistors. If Vout is 3.3V, R1=100k is chosen, then using following equation, R2 can be calculated to be 22.1k:

$$R_2 = \frac{0.6V}{V_{OUT} - 0.6V} R_1 .$$



Input capacitor CIN

The ripple current through input capacitor is calculated as: $I_{CIN\_RMS} = I_{OUT} \cdot \sqrt{D(1-D)} \cdot$

To minimize the potential noise problem, place a typical X5R or better grade ceramic capacitor really close to the IN and GND pins. Care should be taken to minimize the loop area formed by CIN, and IN/GND pins. In this case, a 10uF low ESR ceramic capacitor is recommended.

Output capacitor COUT

The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. For the best performance, it is recommended to use X5R or better grade ceramic capacitor greater than 10uF capacitance.

Output inductor L

There are several considerations in choosing this inductor.
1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the maximum output current. The inductance is calculated as:

$$L = \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{F_{SW} \times I_{OUT,MAX} \times 40\%}$$

where Fsw is the switching frequency and IOUT,MAX is the maximum load current.The regulator IC is quite tolerant of different ripple current amplitude. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

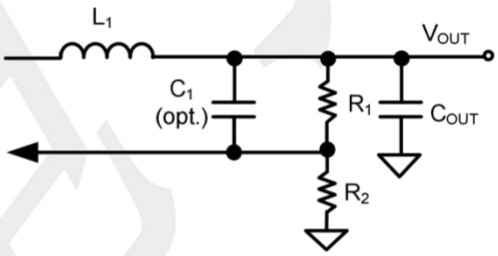
2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

$$I_{SAT,MIN} > I_{OUT,MAX} + \frac{V_{OUT}(1-V_{OUT}/V_{IN,MAX})}{2 \cdot F_{SW} \cdot L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with DCR<50mΩ to achieve a good overall efficiency.

Load Transient Considerations

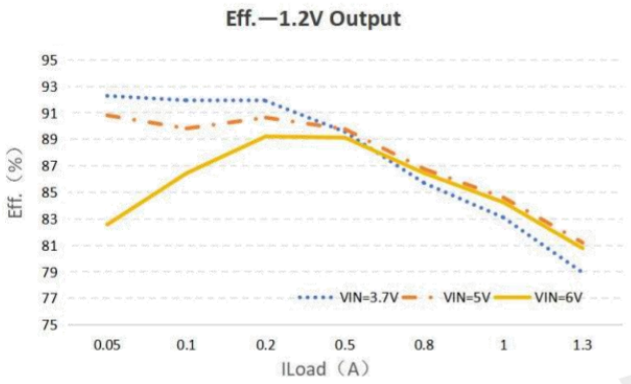
The regulator IC integrates the compensation components to achieve good stability and fast transient responses. In some applications, adding a 22pF ceramic cap in parallel with R1 may further speed up the load transient responses and is thus recommended for applications with large load transient step requirements.

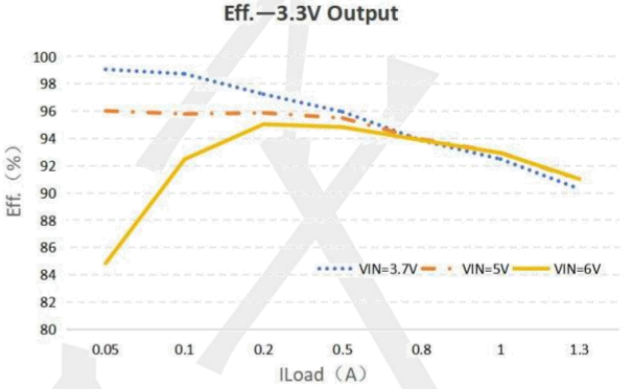


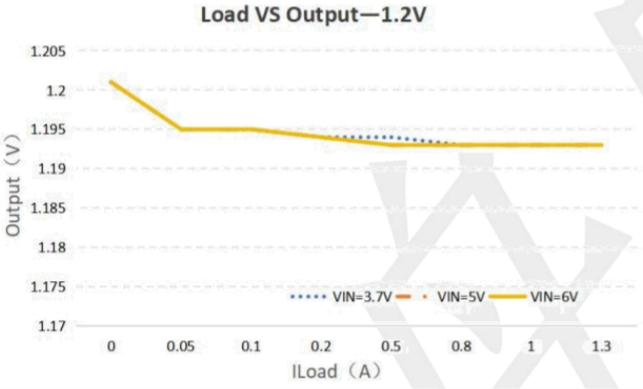
Layout Design

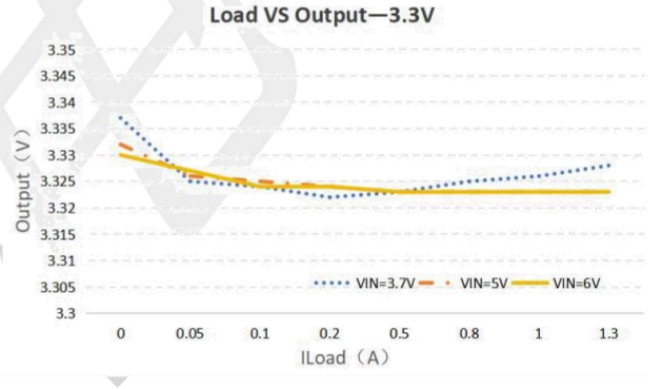
The layout design of regulator is relatively simple. For the best efficiency and minimum noise promblem, we should place the following components close to the IC: CIN, L, R1 and R2.
1) It is desirable to maximize the PCB copper area connecting to GND pin to achieve the best thermal and noise performance. If the board space allowed, a ground plane is highly desirable.
2) CIN must be close to Pins IN and GND. The loop area formed by CIN and GND must be minimized.
3) The PCB copper area associated with LX pin must be minimized to avoid the potential noise problem.
4) The components R1 and R2, and the trace connecting to the FB pin must NOT be adjacent to the LX net on the PCB layout to avoid the noise problem.
5) If the system chip interfacing with the EN pin has a high impedance state at shutdown mode and the IN pin is connected directly to a power source such as a Li-Ion battery, it is desirable to add a pull down 1Mohm resistor between the EN and GND pins to prevent the noise from falsely turning on the regulator at shutdown mode.

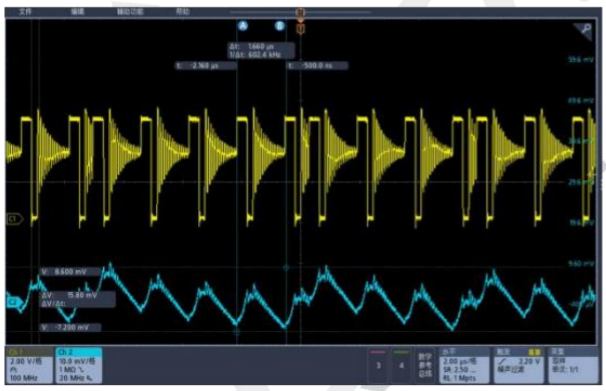
Typical Operating Characteristics









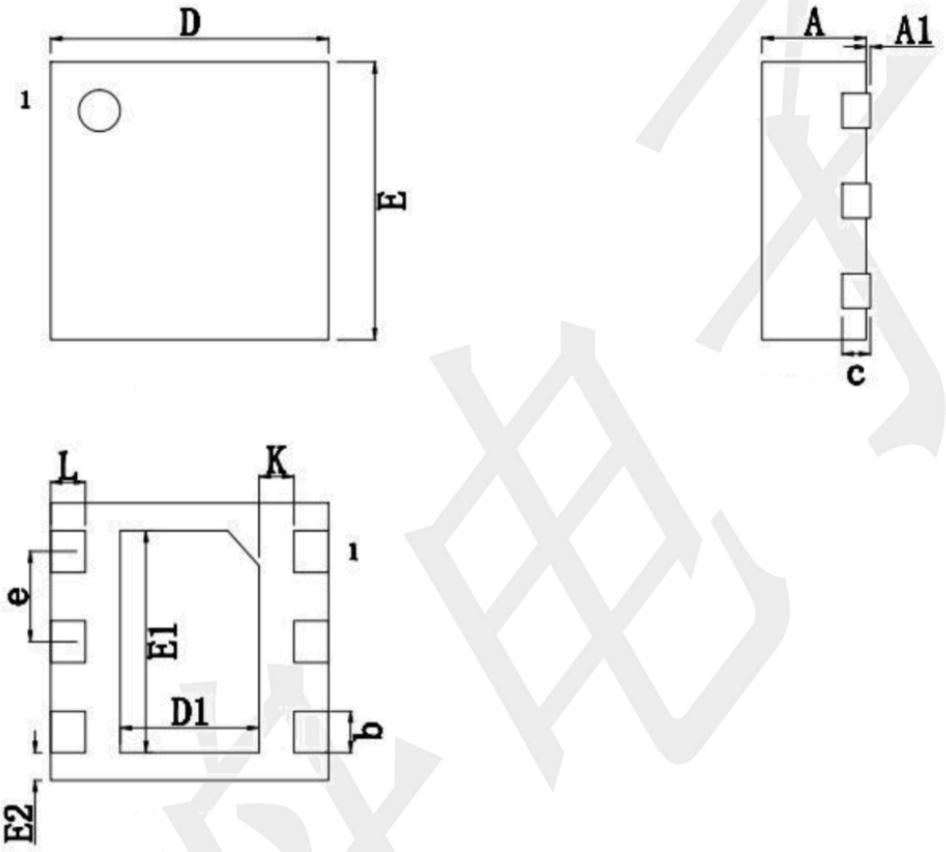


VIN=5V，Vout=3.3V，ILoad=50mA

VIN=5V，Vout=3.3V，ILoad=1.3A

Package Outline Dimensions (unit: mm)

DFN-6(2X2)



SYMBOL	MILLMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.8
A1	0	-	0.05
b	0.25	0.3	0.35
c		0.203 TYP	
D	1.95	2.00	2.05
D1	0.90	1.00	1.10
E	1.95	2.00	2.05
E1	1.55	1.60	1.65
E2		0.20 REF	
e		0.65 BSC	
K		0.25 REF	
L	0.20	0.25	0.3