HMC926LP5E

v01.0614

0.5 dB LSB 6-BIT DIGITAL VARIABLE GAIN AMPLIFIER, 700 - 2700 MHz

RoHS✓ EARTH FRIENDLY

Designer's Kit Available

Typical Applications

The HMC926LP5E is ideal for:

- Cellular Infrastructure
- WiBro, WiMAX and LTE/4G
- Microwave Radio & VSAT
- Test Equipment and Sensors
- IF & RF Applications

Features

Gain Control Range (in 0.5 dB Steps):

@ 900 MHz, +6.5 to +38 dB
@ 1900 MHz, +1 to +32.5 dB
@ 2600 MHz, -4 to +27.5 dB

High Output IP3: +45 dBm

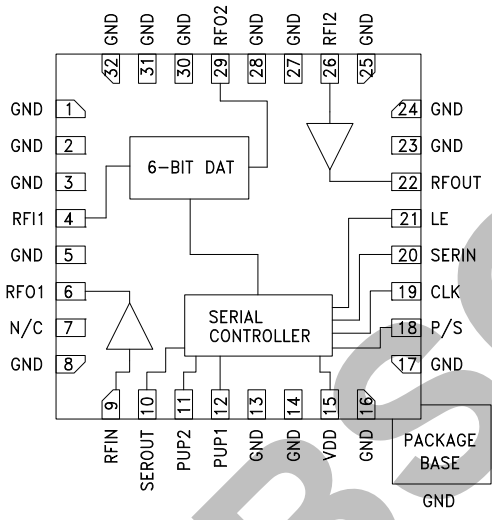
Noise Figure: 4.4 dB

Convenient Serial Control Interface

±0.25 dB Typical Step Error

32 Lead 5 x 5 mm SMT Package: 25 mm²

Functional Diagram



General Description

The HMC926LP5E is a digitally controlled variable gain amplifier which operates from 700 MHz to 2700 MHz, and can be programmed to provide between +6.5 dB to +38 dB of gain, in 0.5 dB steps at 900 MHz. Gain control range is from +1 dB to +32.5 dB at 1900 MHz and from -4 dB to +27.5 dB at 2600 MHz. The HMC926LP5E delivers noise figure of 4.4 dB in its maximum gain state, with output IP3 of up to +45 dBm. The HMC926LP5E features a serial only gain control interface, a user selectable power up state, and a serial output for cascading other Hittite serially controlled components.

Electrical Specifications, T_A = +25° C, Vs = +5V

Parameter	900 MHz Tune [1]			1900 MHz Tune [2]			2600 MHz Tune [3]			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Frequency Range	0.7 - 1.2			1.8 - 2.4			2.3 - 2.7			GHz
Gain (Maximum Gain State)	36	38		30	32.5		25.5	27.5		dB
Gain Control Range		31.5			31.5			31.5		dB
Input Return Loss		16			19			13		dB
Output Return Loss		13			10			13		dB
Attenuation Accuracy: (Referenced to Maximum Gain State)	± (0.4 + 5% of Attenuation Setting)			± (0.5 + 6% of Attenuation Setting)			± (0.5 + 6% of Attenuation Setting)			dB
Output Power for 1 dB Compression	21	24		22	25		22	25		dBm
Output Third Order Intercept Point (Pout = 0 dBm per tone, 1 MHz spacing)		45			40			45		dBm
Noise Figure		4.4			4.8			4.9		dB
Switching Characteristics tON (50% CTL to 90% RF) / tOFF (50% CTL to 10% RF)		-			-			400 / 150		ns
Total Current	162	218	262	162	218	262	162	218	262	mA

[1] See Evaluation PCB and Application Circuit for 900 MHz Tune. Unless otherwise noted, typical performance at 900 MHz, with maximum gain state.
[2] See Evaluation PCB and Application Circuit for 1900 MHz Tune. Unless otherwise noted, typical performance at 1900 MHz, with maximum gain state.
[3] See Evaluation PCB and Application Circuit for 2600 MHz Tune. Unless otherwise noted, typical performance at 2600 MHz, with maximum gain state.

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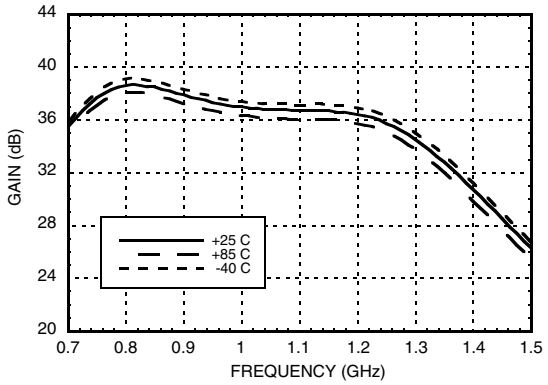
Application Support: Phone: 1-800-ANALOG-D

0.5 dB LSB 6-BIT DIGITAL VARIABLE GAIN AMPLIFIER, 700 - 2700 MHz

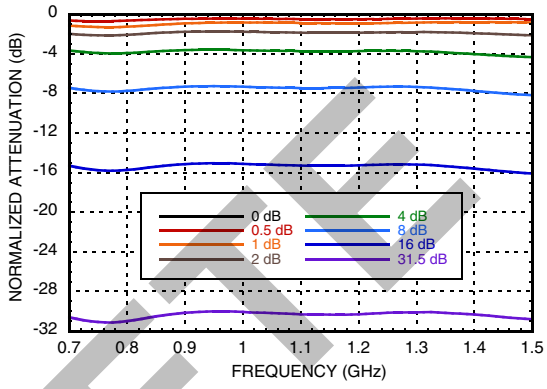
900 MHz Tune [1]

Maximum Gain vs. Frequency [2]



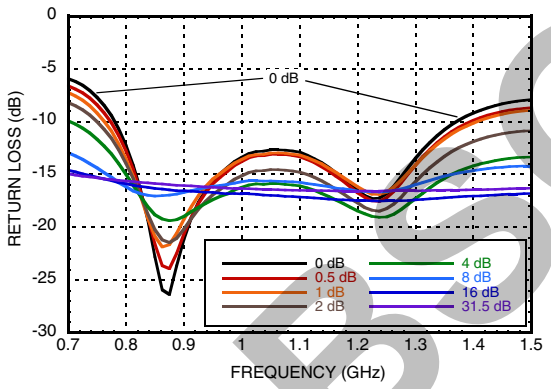
Normalized Attenuation

(Only Major States are Shown)



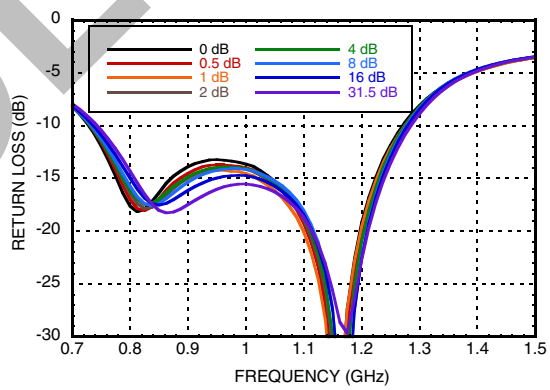
Input Return Loss

(Only Major States are Shown)



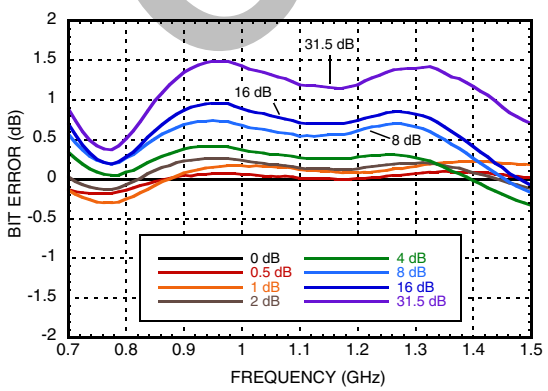
Output Return Loss

(Only Major States are Shown)

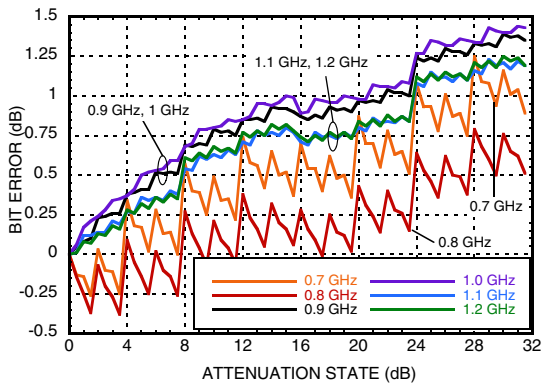


Bit Error vs. Frequency

(Only Major States are Shown)



Bit Error vs. Attenuation State



[1] See Evaluation PCB and Application Circuit for 900 MHz Tune.

[2] Maximum gain state with digital attenuation set to minimum attenuation.

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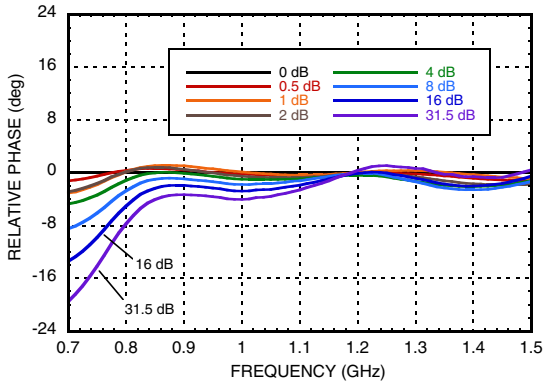
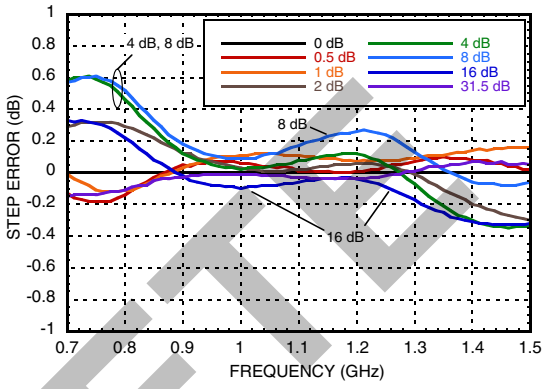
900 MHz Tune [1]

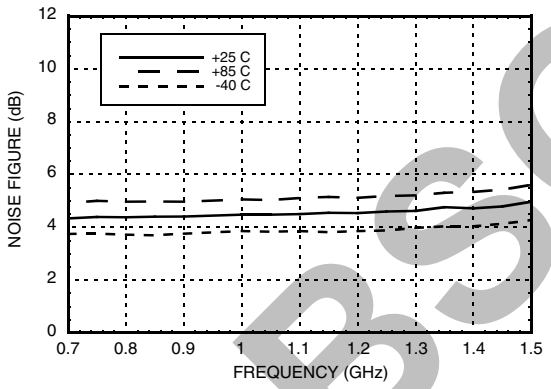
Relative Phase vs. Frequency
(Only Major States are Shown)



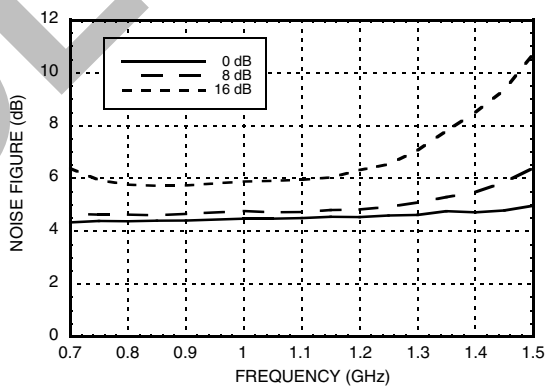
Step Error vs. Frequency
(Only Major States are Shown)



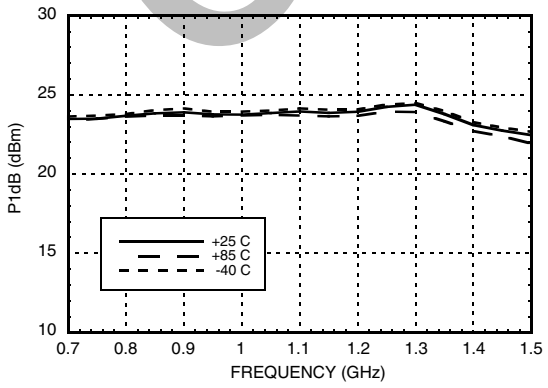
Noise Figure vs. Temperature [2]



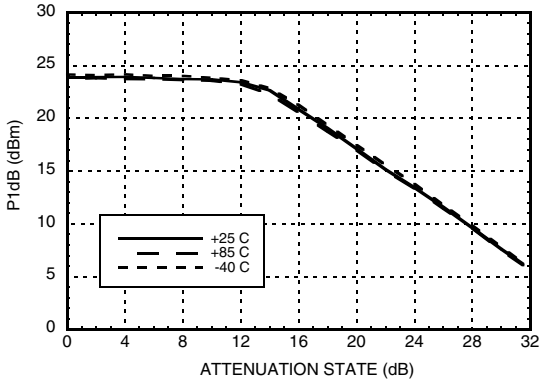
Noise Figure vs. Attenuation State



Output P1dB vs. Frequency [2]



Output P1dB vs. Attenuation State @ 900 MHz



[1] See Evaluation PCB and Application Circuit for 900 MHz Tune.
[2] Maximum gain state with digital attenuation set to minimum attenuation.

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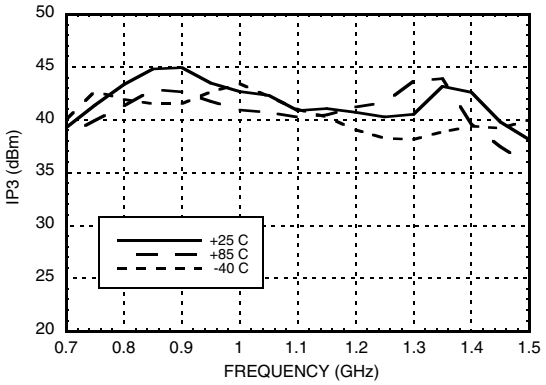
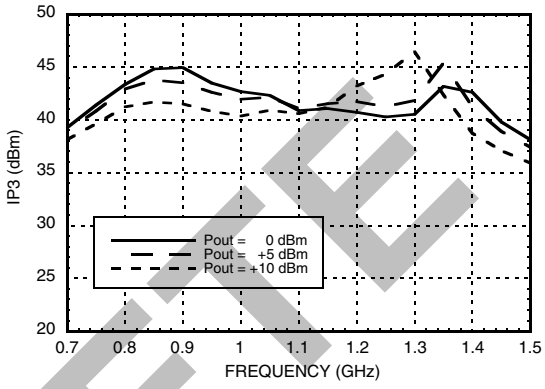
900 MHz Tune [1]

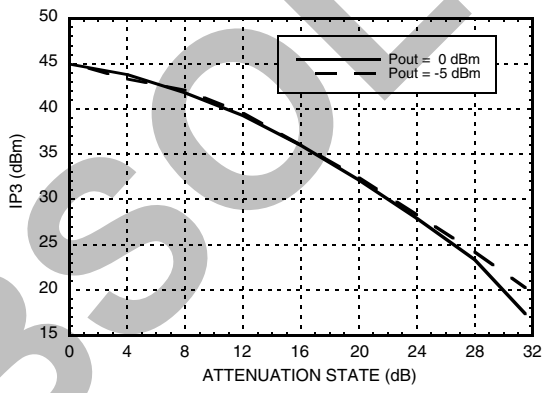
Output IP3 vs. Temperature [2][3]



Output IP3 vs. Tone Power [2]



Output IP3 vs. Attenuation State @ 900 MHz



[1] See Evaluation PCB and Application Circuit for 900 MHz Tune.
[2] Maximum gain state with digital attenuation set to minimum attenuation.
[3] Two-tone output power @ 0 dBm

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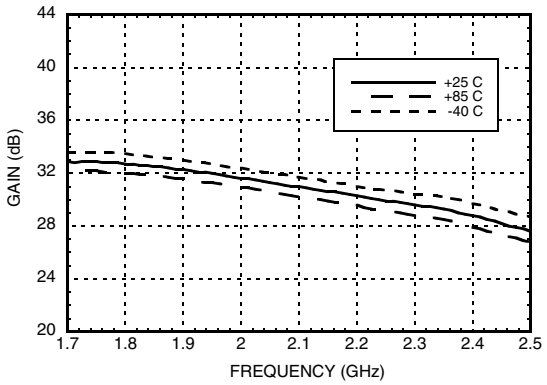
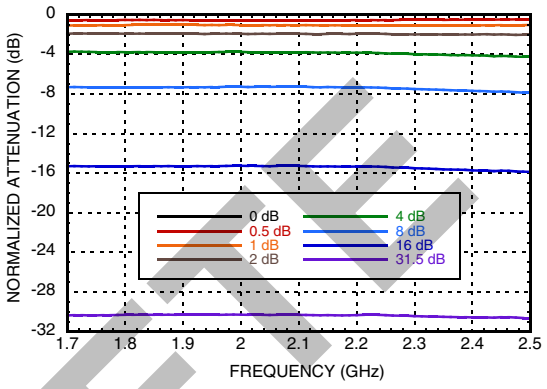
1900 MHz Tune [1]

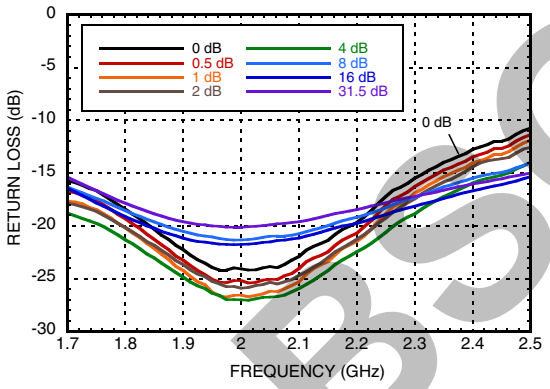
Maximum Gain vs. Frequency [2]



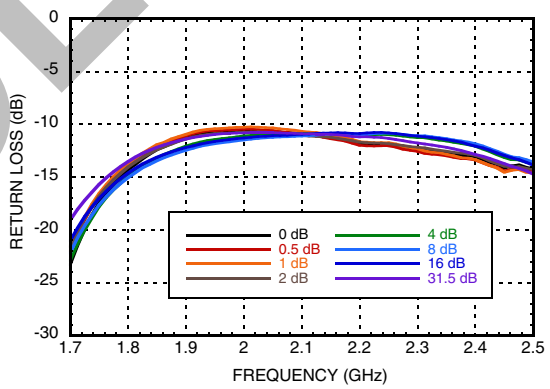
Normalized Attenuation
(Only Major States are Shown)



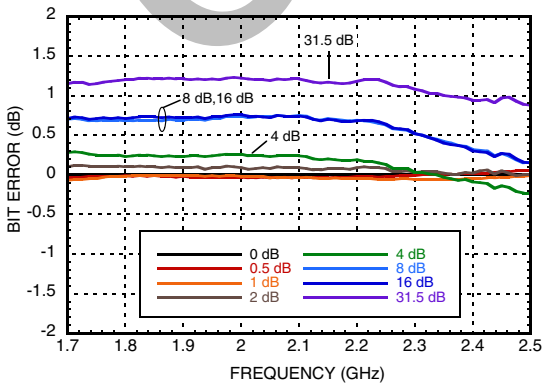
Input Return Loss
(Only Major States are Shown)



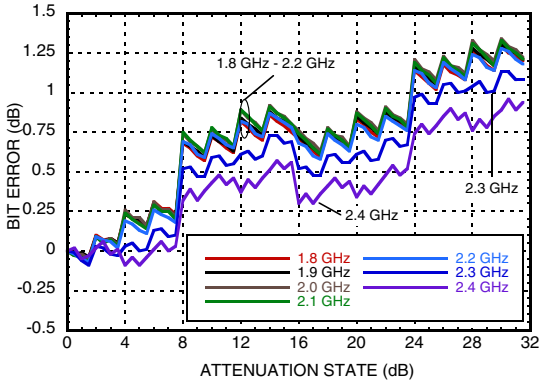
Output Return Loss
(Only Major States are Shown)



Bit Error vs. Frequency
(Only Major States are Shown)



Bit Error vs. Attenuation State



[1] See Evaluation PCB and Application Circuit for 1900 MHz Tune.
[2] Maximum gain state with digital attenuation set to minimum attenuation.

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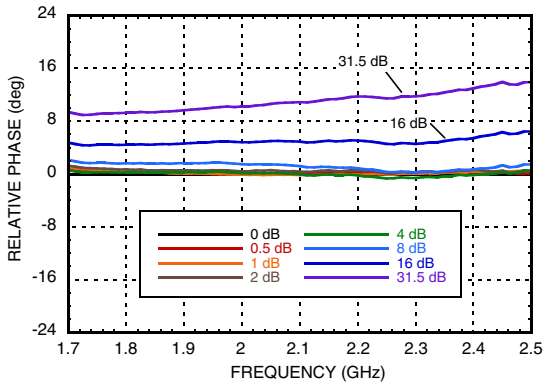
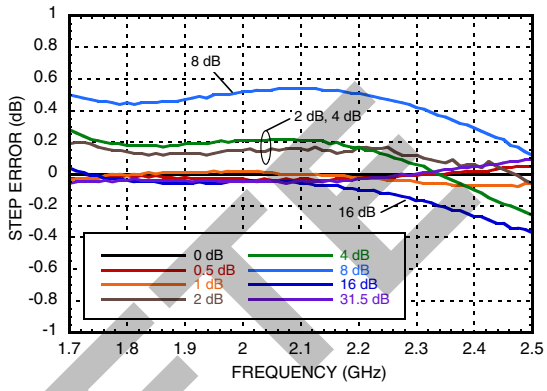
1900 MHz Tune [1]

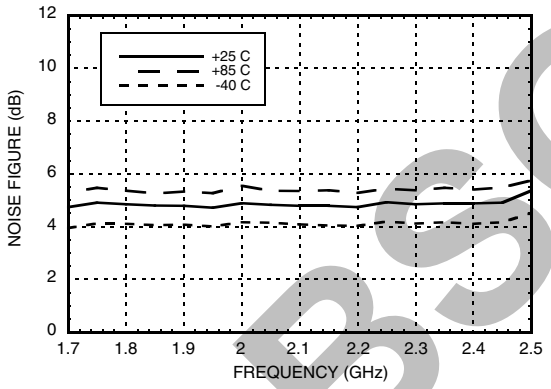
Relative Phase vs. Frequency
(Only Major States are Shown)



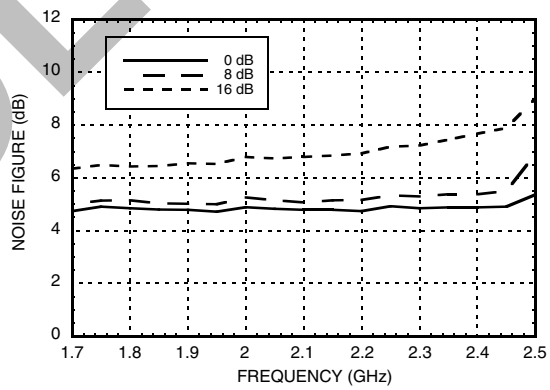
Step Error vs. Frequency
(Only Major States are Shown)



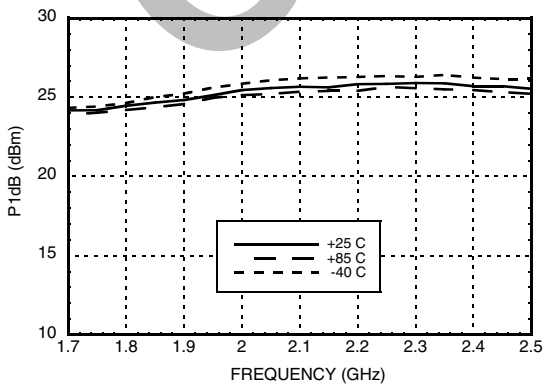
Noise Figure vs. Temperature [2]



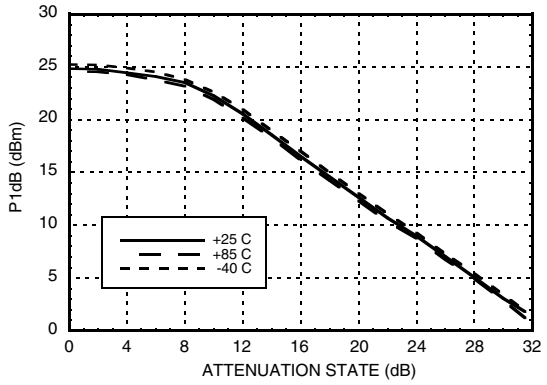
Noise Figure vs. Attenuation State



Output P1dB vs. Frequency [2]



Output P1dB vs. Attenuation State @ 1900 MHz



[1] See Evaluation PCB and Application Circuit for 1900 MHz Tune.
[2] Maximum gain state with digital attenuation set to minimum attenuation.

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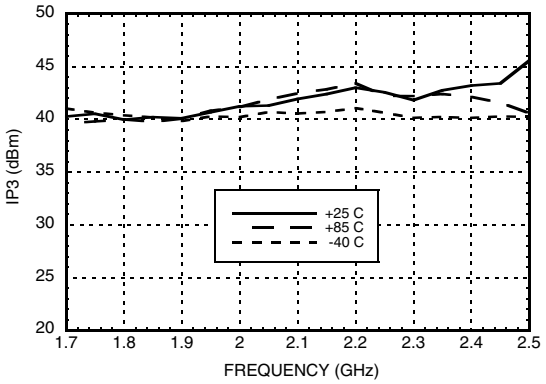
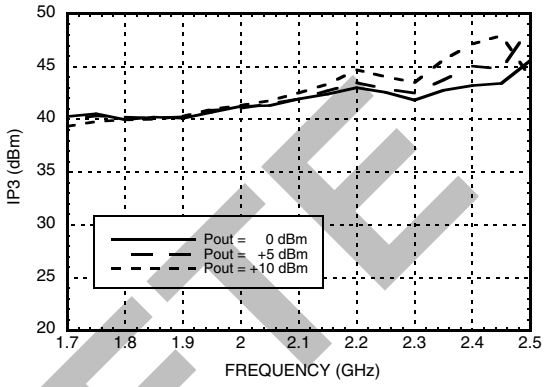
1900 MHz Tune [1]

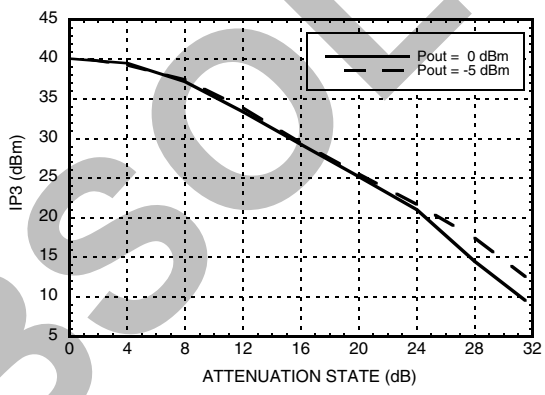
Output IP3 vs. Temperature [2][3]



Output IP3 vs. Tone Power [2]



Output IP3 vs. Attenuation State @ 1900 MHz



[1] See Evaluation PCB and Application Circuit for 1900 MHz Tune.
[2] Maximum gain state with digital attenuation set to minimum attenuation.
[3] Two-tone output power @ 0 dBm

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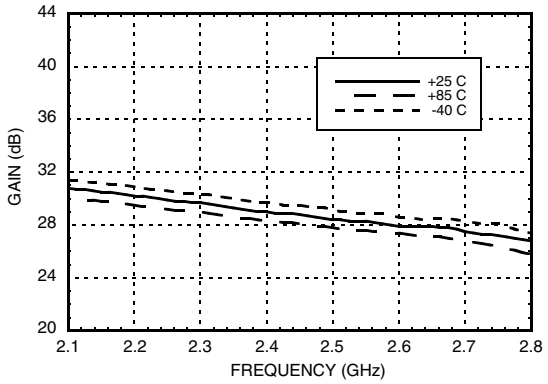
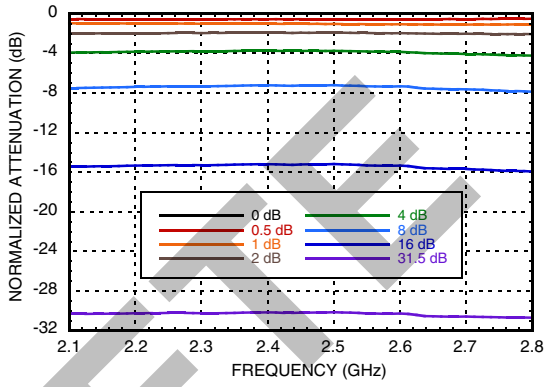
2600 MHz Tune [1]

Maximum Gain vs. Frequency [2]



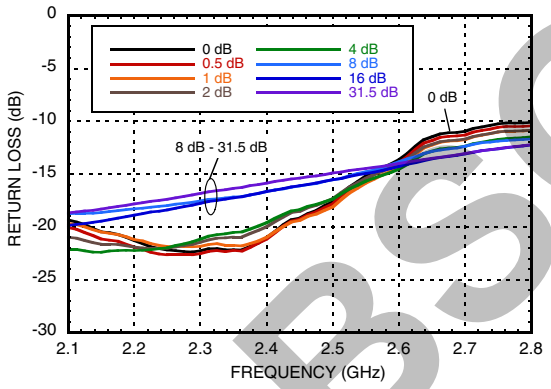
Normalized Attenuation

(Only Major States are Shown)



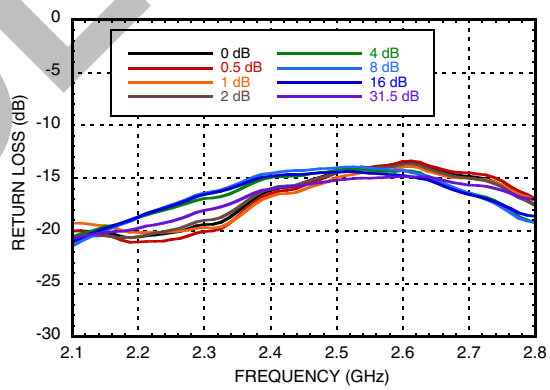
Input Return Loss

(Only Major States are Shown)



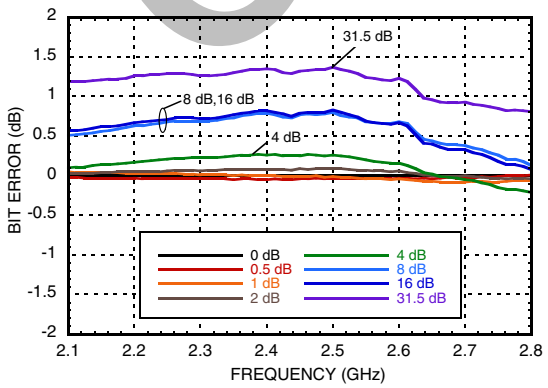
Output Return Loss

(Only Major States are Shown)

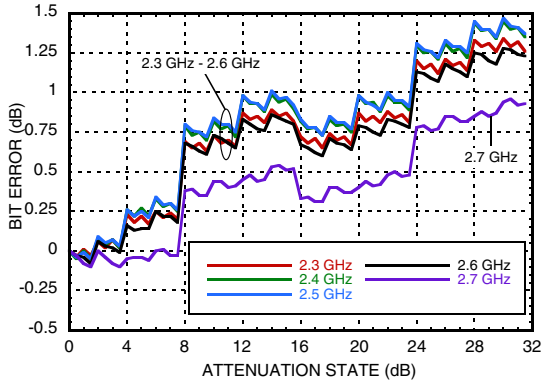


Bit Error vs. Frequency

(Only Major States are Shown)



Bit Error vs. Attenuation State



[1] See Evaluation PCB and Application Circuit for 2600 MHz Tune.

[2] Maximum gain state with digital attenuation set to minimum attenuation.

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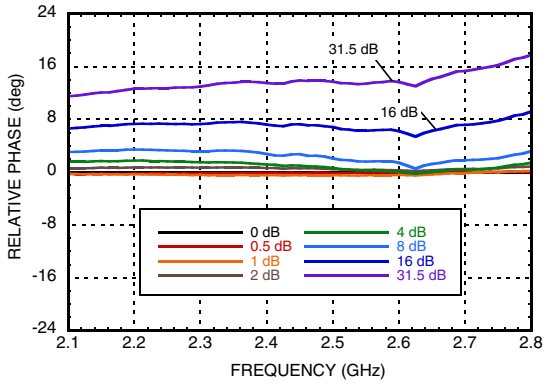
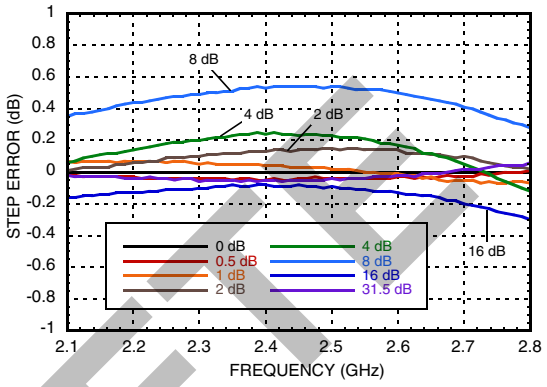
2600 MHz Tune [1]

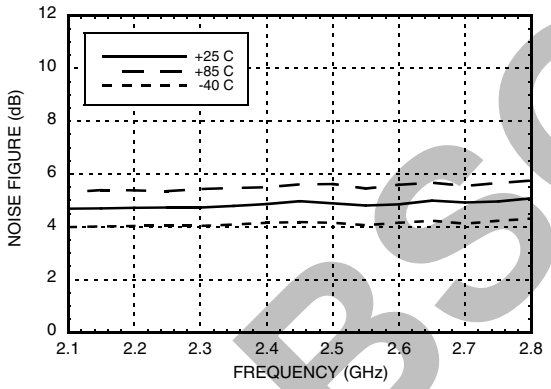
Relative Phase vs. Frequency
(Only Major States are Shown)



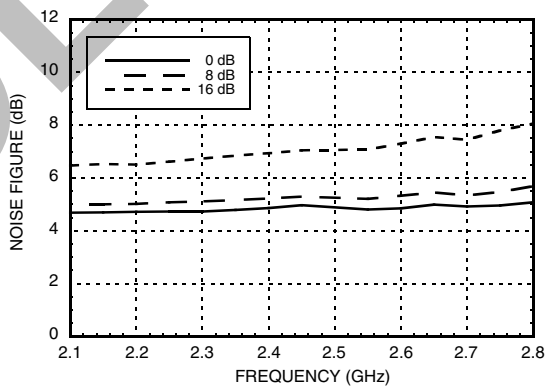
Step Error vs. Frequency
(Only Major States are Shown)



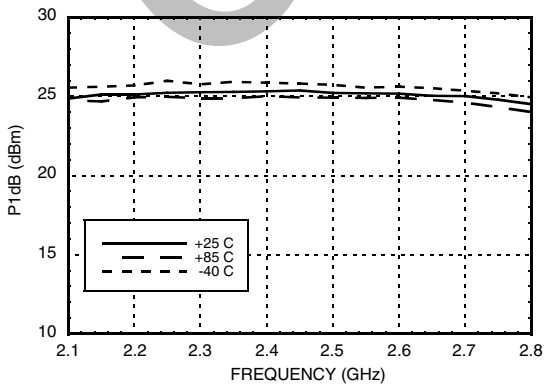
Noise Figure vs. Temperature [2]



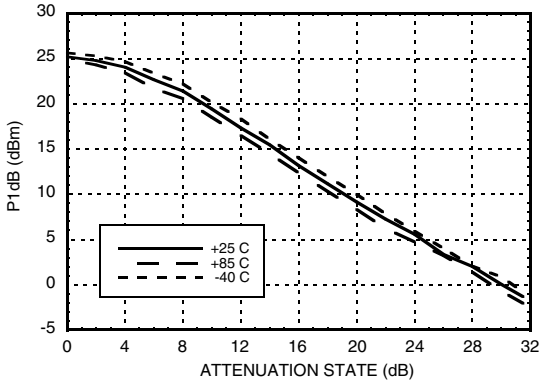
Noise Figure vs. Attenuation State



Output P1dB vs. Frequency [2]



Output P1dB vs. Attenuation State @ 2600 MHz



[1] See Evaluation PCB and Application Circuit for 2600 MHz Tune.
[2] Maximum gain state with digital attenuation set to minimum attenuation.

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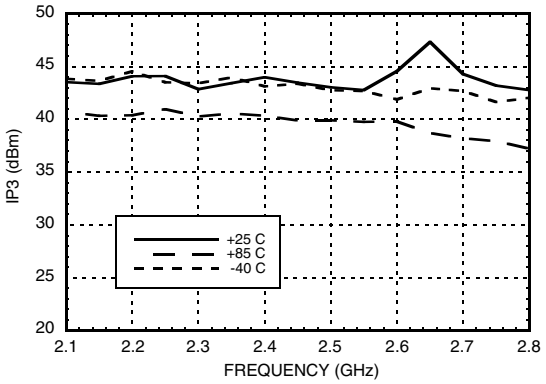
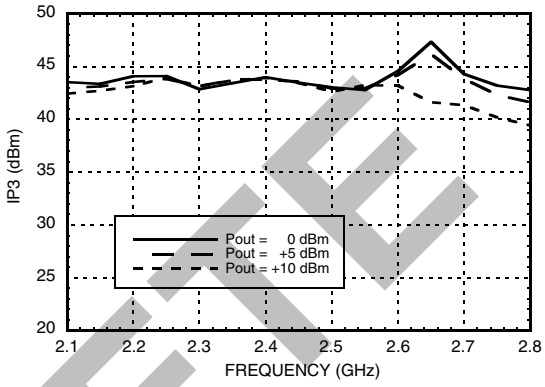
0.5 dB LSB 6-BIT DIGITAL VARIABLE GAIN AMPLIFIER, 700 - 2700 MHz

2600 MHz Tune [1]

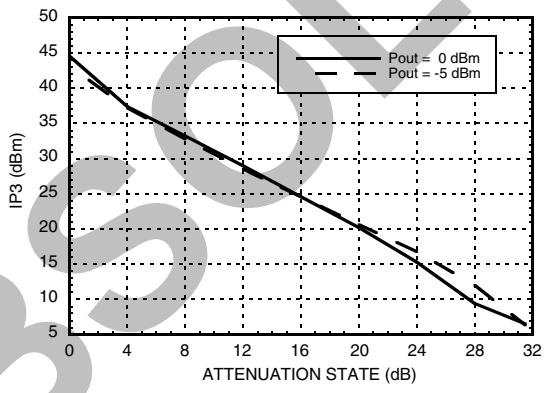
Output IP3 vs. Temperature [2][3]



Output IP3 vs. Tone Power [2]



Output IP3 vs. Attenuation State @ 2600 MHz



[1] See Evaluation PCB and Application Circuit for 2600 MHz Tune.
[2] Maximum gain state with digital attenuation set to minimum attenuation.
[3] Two-tone output power @ 0 dBm

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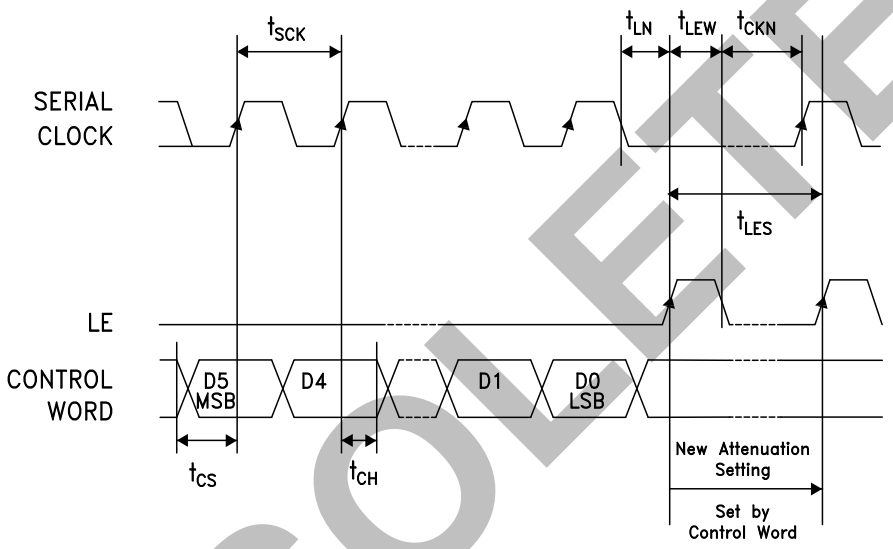
Serial Control Interface

The HMC926LP5E contains a 3-wire SPI compatible digital interface (SERIN, CLK, LE). It is activated when P/S is kept high. The 6-bit serial word must be loaded MSB first. The positive-edge sensitive CLK and LE requires clean transitions. Standard logic families work well. If mechanical switches were used, sufficient debouncing should be provided. When LE is high, 6-bit data in the serial input register is transferred to the attenuator. When LE is high CLK is masked to prevent data transition during output loading.



Parameter	Typ.
Min. serial period, t_{SCK}	100 ns
Control set-up time, t_{CS}	20 ns
Control hold-time, t_{CH}	20 ns
LE setup-time, t_{LN}	10 ns
Min. LE pulse width, t_{LEW}	10 ns
Min LE pulse spacing, t_{LES}	630 ns
Serial clock hold-time from LE, t_{CKN}	10 ns

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Power-Up States

If LE is set to logic LOW at power-up, the logic state of PUP1 and PUP2 determines the power-up state of the part per PUP truth table. The DVGA latches in the desired power-up state approximately 200 ms after power-up.

Power-On Sequence

The ideal power-up sequence is: GND, Vs, digital inputs, RF inputs. The relative order of the digital inputs are not important as long as they are powered after Vs / GND

Absolute Maximum Ratings

Bias Voltage (Vdd)	5.5 V
RF Input Power (RFIN) (Vdd = +5 Vdc)	+10 dBm up to 1 GHz +8 dBm from 1 - 2.7 GHz
Digital I/O (Latch Enable, Clock, Serial Input, Serial Output, P/S, PUP1-2)	-0.5 to Vdd +0.5V
Junction / Channel Temperature	150 °C
Continuous Pdiss (T= 85 °C) (derate 26 mW/°C above 85 °C)	1.354 W
Thermal Resistance (junction / channel to ground paddle)	48 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C
ESD Sensitivity (HBM)	Class 1A

PUP Truth Table

LE	PUP1	PUP2	Gain Relative to Maximum Gain
0	0	0	-31.5 dB
0	1	0	-24 dB
0	0	1	-16 dB
0	1	1	Insertion Loss

Control Voltage Table

State	Vdd = +5V
Low	0 to 0.8V @ <1 µA
High	2 to 5V @ <1 µA

Typical Supply Current vs. Vs

Vs (V)	Total Is (mA)
4.5	153
5.0	218
5.5	288

Note: Amplifier will operate over full voltage ranges shown above.

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

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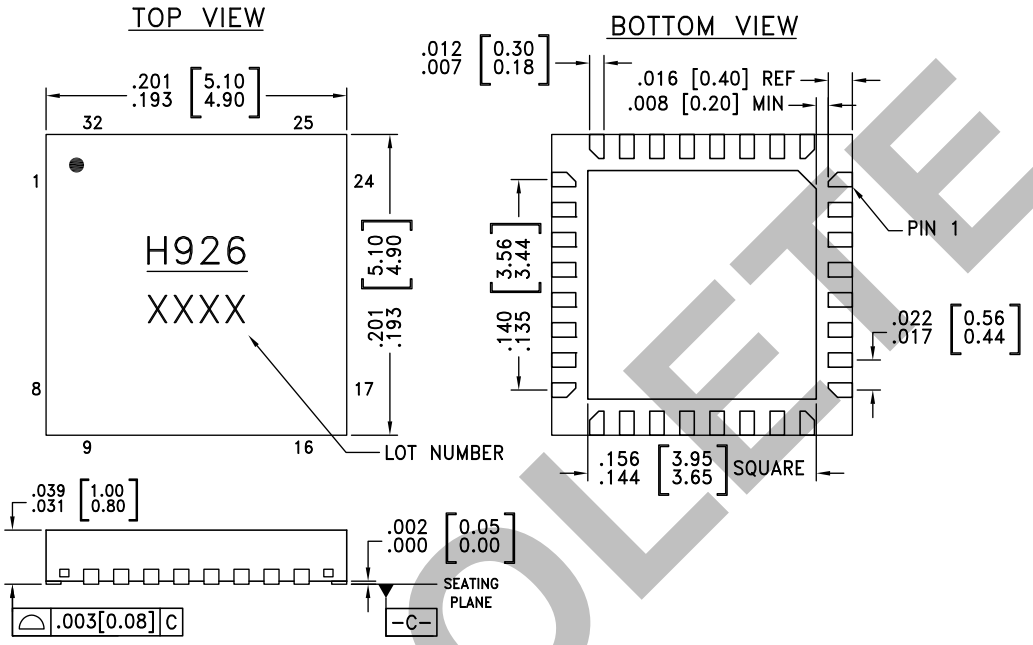
0.5 dB LSB 6-BIT DIGITAL VARIABLE GAIN AMPLIFIER, 700 - 2700 MHz

Outline Drawing



NOTES:

1. LEADFRAME MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS]
3. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
4. PAD BURR LENGTH SHALL BE 0.15 mm MAXIMUM. PAD BURR HEIGHT SHALL BE 0.05 mm MAXIMUM.
5. PACKAGE WARP SHALL NOT EXCEED 0.05 mm.
6. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
7. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED LAND PATTERN.

Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [1]
HMC926LP5E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 [2]	H926 XXXX

[1] 4-Digit lot number XXXX

[2] Max peak reflow temperature of 260 °C

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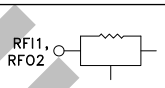
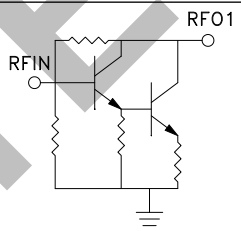
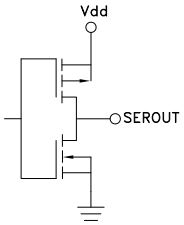
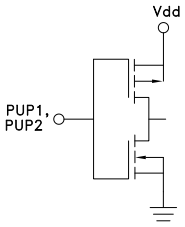
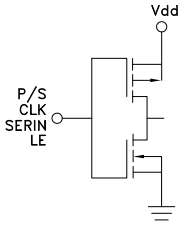
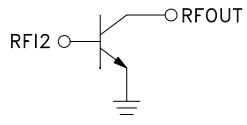
Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1 - 3, 5, 8, 13, 14, 16, 17, 23 - 25, 27, 28, 30 - 32	GND	These pins and package bottom must be connected to RF/DC ground.	
4	RFI1	Input and output of the 6-bit digital attenuator (6-Bit DAT). These pins are DC coupled and matched to 50 Ohms. Blocking capacitors are required. Select value based on lowest frequency of operation.	
29	RFO2		
9	RFIN	This pin is DC coupled. An off chip DC blocking capacitor is required.	
6	RFO1	RF output and DC Bias (Vcc) for the output stage.	
7	N/C	The pin is not connected internally; however, all data shown herein was measured with this pin connected to RF/DC ground externally.	
10	SEROUT	Serial input data delayed by 6 clock cycles.	
12, 11	PUP1, PUP2	See PUP truth table, control voltage table.	
15	Vdd	Supply voltage	
18	P/S	See truth table, control voltage table and timing diagram.	
19	CLK		
20	SERIN		
21	LE		
26	RFI2	This pin is DC coupled. Off chip matching components are required. See Application Circuit herein.	
22	RFOUT	RF output and DC Bias input for the amplifier. Off chip matching components are required. See Application Circuit herein.	

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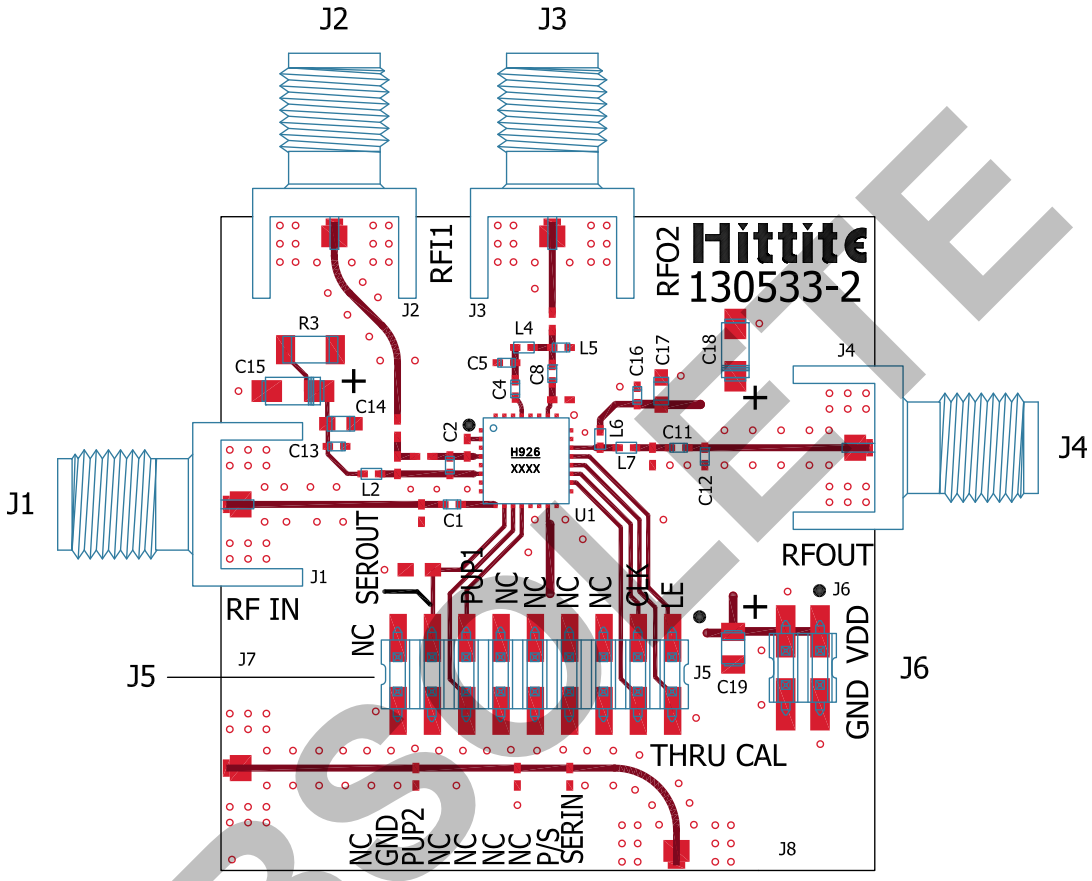
Evaluation PCB - 900 MHz



List of Materials for Evaluation PCB 131836 [1]

Item	Description
J1 - J4	Johnson SMA Connector
J5	2 mm Vertical Molex 18 pos Connector
J6	2 mm Vertical Molex 4 pos Connector
C1, C2, C4, C11, C13, C16	100 pF Capacitor, 0402 Pkg.
C5	6.8 pF Capacitor, 0402 Pkg.
C8	10 pF Capacitor, 0402 Pkg.
C12	1.2 pF Capacitor, 0402 Pkg.
C14, C17	1 nF Capacitor, 0603 Pkg.
C15, C18	2.2 µF Capacitor, Tantalum
C19	4.7 µF Capacitor, 0805 Pkg.
L2, L6	18 nH Inductor, 0402 Pkg.
L4	1.8 nH Inductor, 0402 Pkg.
L5	1.2 nH Inductor, 0402 Pkg.

Item	Description
L7	3.9 nH Inductor, 0402 Pkg.
R3	1.8 Ω Resistor, 1206 Pkg.
U1	HMC926LP5E DVGA
PCB [2]	130533 Evaluation PCB

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Arlon 25FR or Roger 4350

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

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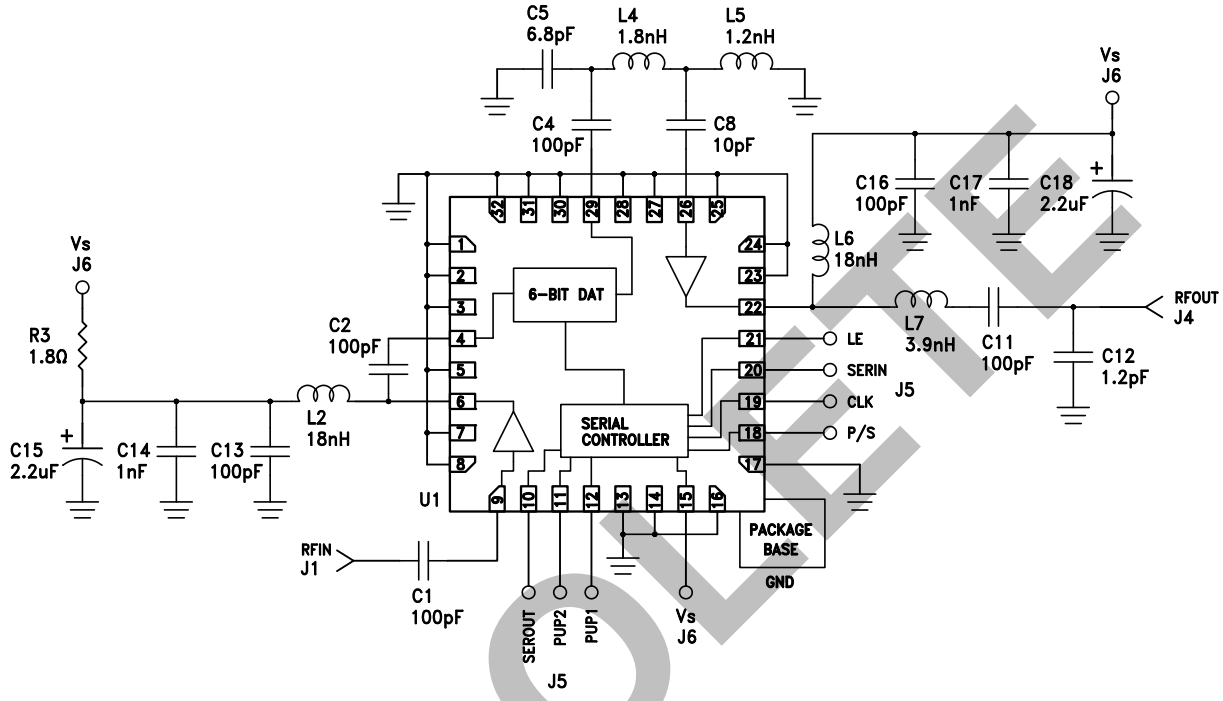
0.5 dB LSB 6-BIT DIGITAL VARIABLE GAIN AMPLIFIER, 700 - 2700 MHz

Application Circuit - 900 MHz



Note: The HMC926LP5E requires interconnection traces with matching components from RFO1 pin to RFI1 pin, and from RFO2 pin to RFI2 pin. The proper component network (L2, C2, C4, C5, L4, L5, C8, L6, L7, C11 and C12) for 900MHz applications is provided in this schematic. The performance of the HMC926LP5E would be sensitive to the placement of these components and variations in the component values. For best performance use the identical component placement with same length transmission lines as shown in the Evaluation PCB – 900MHz. Contact factory if assistance is required on component placement and selection.

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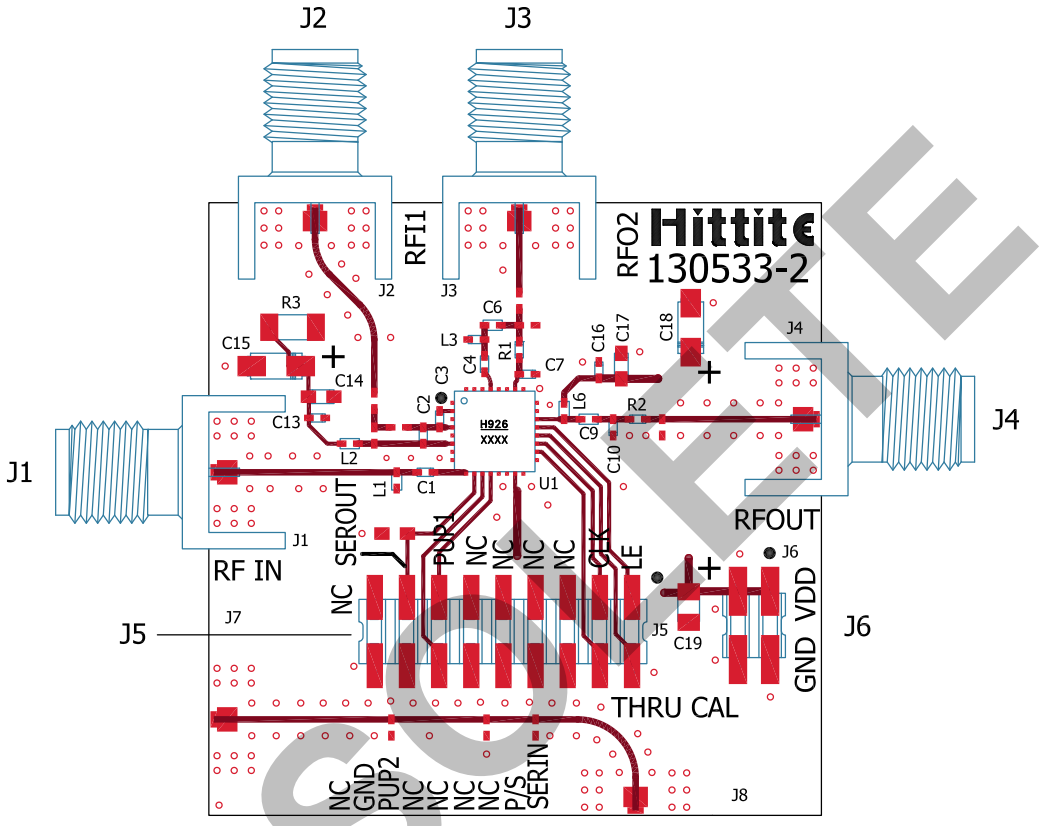
Evaluation PCB - 1900 & 2600 MHz



List of Materials for Evaluation PCB [1]

Item	Description
J1-J4	Johnson SMA Connector
J5	2 mm Vertical Molex 18 pos Connector
J6	2 mm Vertical Molex 4 pos Connector
C1	3 pF Capacitor, 0402 Pkg.
C2, C4, C9, C13, C16	100 pF Capacitor, 0402 Pkg.
C3	0.6 pF Capacitor, 0402 Pkg.
C6, C10	1.5 pF Capacitor, 0402 Pkg.
C7 [2]	Capacitor, 0402 Pkg.
C14, C17	1 nF Capacitor, 0603 Pkg.
C15, C18	2.2 µF Capacitor, Tantalum
C19	4.7 µF Capacitor, 0805 Pkg.
L1	4.7 nH Inductor, 0402 Pkg.
L2	2.0 nH Inductor, 0402 Pkg.
L3 [2]	Inductor, 0402 Pkg.
L6	2.7 nH Inductor, 0402 Pkg.
R1-R2	0 Ω Resistor, 0402 Pkg.
R3	1.8 Ω Resistor, 1206 Pkg.

Item	Description
U1	HMC926LP5E DVGA
PCB [3]	130533 Evaluation PCB

[1] When requesting an evaluation board, please reference the appropriate evaluation PCB number listed in the table "Components for Selected Frequency Tune"

[2] Please refer to "Components for Selected Frequency Tune" table for values

[3] Circuit Board Material: Arlon 25FR or Roger 4350

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

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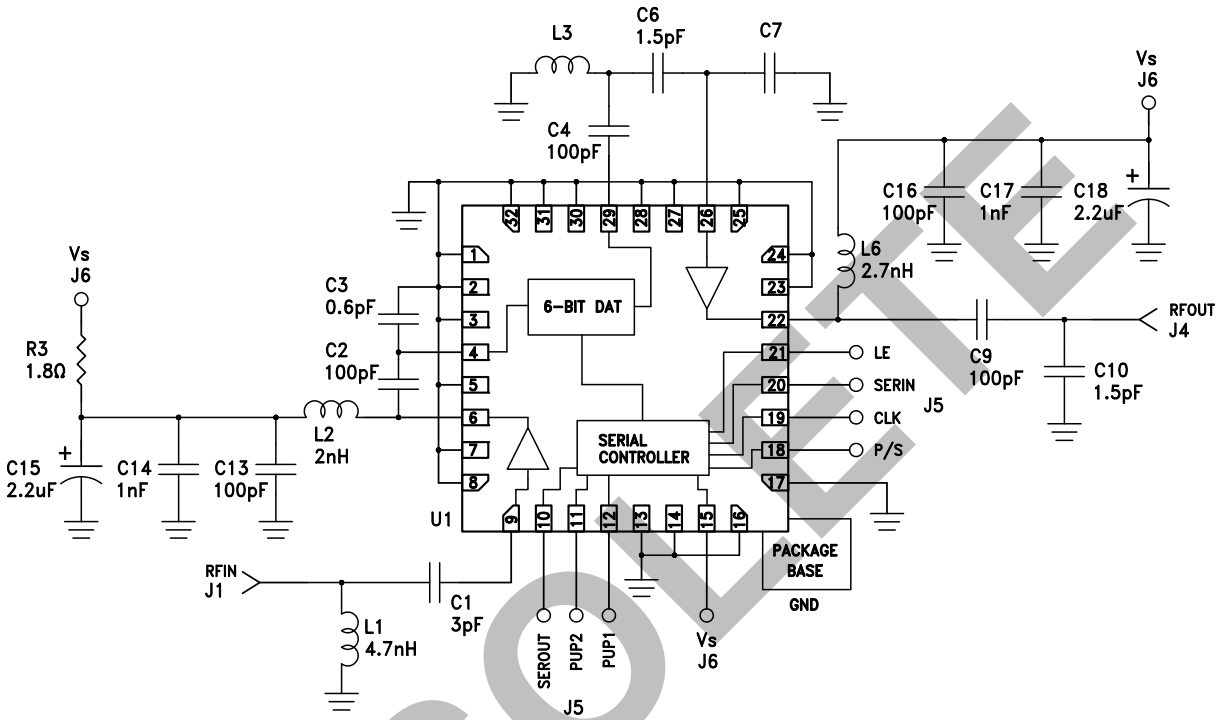
Application Circuit - 1900 & 2600 MHz



Components for Selected Frequency Tune

Tune Option	Evaluation PCB Number	L3	C7
1900 MHz	131838	2.7 nH	3.9 pF
2600 MHz	131839	3.3 nH	2.7 pF

Note: The HMC926LP5E requires interconnection traces with matching components from RFO1 pin to RFI1 pin, and from RFO2 pin to RFI2 pin. The proper component network (L2, C2, C3, C4, L3, C6, C7, L6, C9, and C10) for 1900 & 2600 MHz applications is provided in this schematic. The performance of the HMC926LP5E would be sensitive to the placement of these components and variations in the component values. For best performance use the identical component placement with same length transmission lines as shown in the Evaluation PCB – 1900 & 2600 MHz. Contact factory if assistance is required on component placement and selection.

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