## Feature

- 2.7V to 5.5V Input Voltage Range
- Four Buck Converters
- Typical Feedback Voltage: 0.6V
- Maximum Continuous Load Current:2A (4CH total output power consumption must be less than 10W)
- Fixed 1.2MHz Switching Frequency
- 100% Duty Cycle Low Dropout Operation
- <1uA Shutdown Current
- Independent Enable Control
- Internal Compensation
- Cycle-by-Cycle Current Limit
- Short Circuit Protection
- Each Channel Efficiency Up to 95%
- Auto Recovery OTP Protection
- Available in 24-pin 4mm × 4mm QFN Package

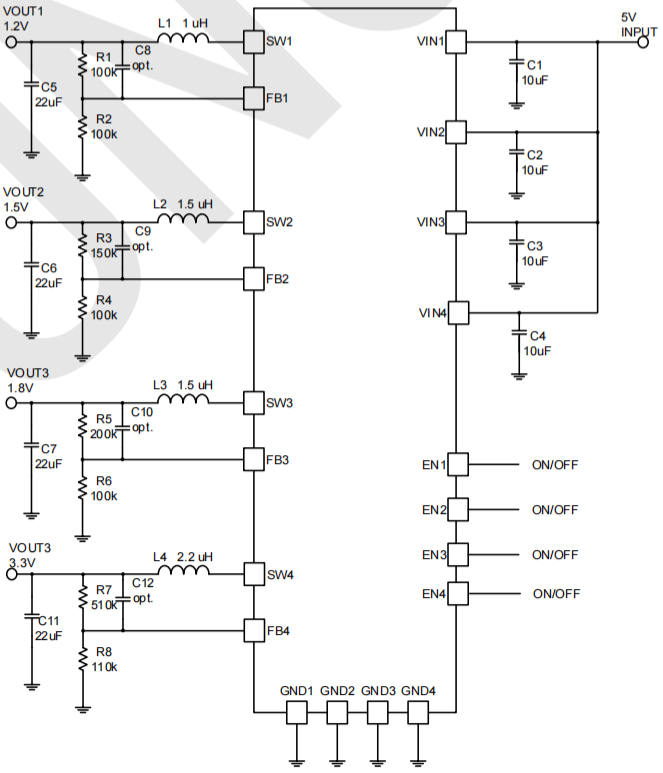
## Applications

- IP Camera
- Video Door Bell
- DVR
- OTT/DVR

## General Description

The EA3059 is a 4-CH power management IC for applications powered by one Li-Ion battery or a DC 5V adapter. It integrates four synchronous buck regulators and can provide high efficiency output at light load and heavy load operation. The internal compensation architecture simplifies the application circuit design. Besides, the independent enable control makes the designer have the greatest flexibility to optimize timing for power sequencing purposes. The EA3059 is available in a 24 pin QFN 4×4 package.

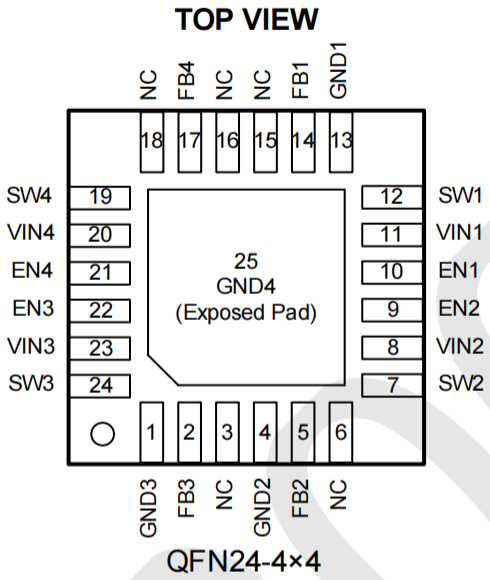
## Typical Applications




Basic Application Circuit

# Pin Description

## Pin Configuration




## Pin Description

| Item | Name | Function Description |
|---|---|---|
| 1 | GND3 | Ground pin of CH3. |
| 2 | FB3 | Feedback input of CH3. Connect to output voltage with a resistor divider. |
| 3 | NC | No connect. |
| 4 | GND2 | Ground pin of CH2. |
| 5 | FB2 | Feedback input of CH2. Connect to output voltage with a resistor divider. |
| 6 | NC | No connect. |
| 7 | SW2 | Internal MOSFET switching output of CH2. Connect SW2 pin with a low pass filter circuit to obtain a stable DC output voltage. |
| 8 | VIN2 | Power input pin of CH2. Recommended to use a 10uF MLCC capacitor between VIN2 pin and PGND2 pin. |
| 9 | EN2 | CH2 turns on/turns off control input. Don't leave this pin floating. |
| 10 | EN1 | CH1 turns on/turns off control input. Don't leave this pin floating. |
| 11 | VIN1 | Power input pin of CH1. Recommended to use a 10uF MLCC capacitor between VIN1 pin and PGND1 pin. |
| 12 | SW1 | Internal MOSFET switching output of CH1. Connect SW1 pin with a low pass filter circuit to obtain a stable DC output voltage. |
| 13 | GND1 | Ground pin of CH1. |
| 14 | FB1 | Feedback input of CH1. Connect to output voltage with a resistor divider. |
| 15 | NC | No connect. |
| 16 | NC | No connect. |
| 17 | FB4 | Feedback input of CH4. Connect to output voltage with a resistor divider. |

| | | |
|---|---|---|
| 18 | NC | No connect. |
| 19 | SW4 | Internal MOSFET switching output of CH4. Connect SW4 pin with a low pass filter circuit to obtain a stable DC output voltage. |
| 20 | VIN4 | Power input pin of CH4. Recommended to use a 10uF MLCC capacitor between VIN4 pin and PGND4 pin. |
| 21 | EN4 | CH4 turns on/turns off control input. Don't leave this pin floating. |
| 22 | EN3 | CH3 turns on/turns off control input. Don't leave this pin floating. |
| 23 | VIN3 | Power input pin of CH3. Recommended to use a 10uF MLCC capacitor between VIN3 pin and PGND3 pin. |
| 24 | SW3 | Internal MOSFET switching output of CH3. Connect SW3 pin with a low pass filter circuit to obtain a stable DC output voltage. |
| 25 | GND4 (Exposed Pad) | Ground pin of CH4. |

## Order Information (1)

| Part No. | Model | Description | Package | T/R Qty. |
|---|---|---|---|---|
| 00304003 | EA3059 | EA3059 4×Buck, 2.7-5.5V, 2.0A, 1.2MHz, VFB0.6V , QFN24-4×4 | QFN24-4×4 | 3000PCS |

Note (1): All SUNGOOD parts are Pb-Free and adhere to the RoHS directive.

## Specifications

### Absolute Maximum Ratings (1) (2)

| Item | Min | Max | Unit |
|---|---|---|---|
| $V_{IN1}$, $V_{IN2}$, $V_{IN3}$ Voltage | -0.3 | 6.5 | V |
| $V_{SW1}$, $V_{SW2}$, $V_{SW3}$ Voltage | -0.3 | $V_{IN}$+0.3V | V |
| All Other Pins Voltage | -0.3 | 6.5 | V |
| Power Dissipation (3) | Internally Limited | | |
| Operating Junction Temperature, $T_J$ | -40 | 150 | °C |
| Storage Temperature, $T_{stg}$ | -55 | 150 | °C |
| Lead Temperature (Soldering, 10sec.) | | 260 | °C |

Note (1): Exceeding these ratings may damage the device.

Note (2): The device is not guaranteed to function outside of its operating conditions.

Note (3): The maximum allowable power dissipation is a function of the maximum junction temperature, $T_{J(MAX)}$, the junction-to-ambient thermal resistance, $R_{\theta JA}$, and the ambient temperature, $T_A$. The maximum allowable power dissipation at any ambient temperature is calculated using: $P_{D\,(MAX)} = (T_{J(MAX)} - T_A)/R_{\theta JA}$. Exceeding the maximum allowable power dissipation causes excessive die temperature, and the regulator goes into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at $T_J$=160°C (typical) and disengages at $T_J$= 130°C (typical).

## ESD Ratings

| Item | Description | Value | Unit |
|---|---|---|---|
| $V_{(ESD-HBM)}$ | Human Body Model (HBM)<br>ANSI/ESDA/JEDEC JS-001-2014<br>Classification, Class: 2 | ±2000 | V |
| $V_{(ESD-CDM)}$ | Charged Device Mode (CDM)<br>ANSI/ESDA/JEDEC JS-002-2014<br>Classification, Class: C0b | ±200 | V |
| $I_{LATCH-UP}$ | JEDEC STANDARD NO.78E APRIL 2016<br>Temperature Classification,<br>Class: I | ±150 | mA |

## Recommended Operating Conditions

| Item | Min | Max | Unit |
|---|---|---|---|
| Operating Junction Temperature (1) | -40 | 125 | °C |
| Operating Temperature Range | -40 | 85 | °C |
| Each Channel Input Voltage | 2.7 | 5.5 | V |
| Each Channel Output Current | 0 | 2 | A |

Note (1): All limits specified at room temperature (TA = 25°C) unless otherwise specified. All room temperature limits are 100% production tested. All limits at temperature extremes are ensured through correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).

## Thermal Information

| Item | Description | Value | Unit |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance (1)(2) | 37.5 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 22.8 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 12.8 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 0.3 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 12.5 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (Bottom) thermal resistance | 1.5 | °C/W |

Note (1): The package thermal impedance is calculated in accordance to JESD 51-7.
Note (2): Thermal Resistances were simulated on a 4-layer, JEDEC board

## Electrical Characteristics (1) (2)

| Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Input Voltage Range | | 2.7 | | 5.5 | V |
| Supply Current (Quiescent) | $V_{EN}$ =3.0V | | 80 | | μA |
| Supply Current (Shutdown) | $V_{EN}$ =0 or EN = GND | | 0.1 | 1.0 | μA |
| Feedback Voltage | | 0.588 | 0.600 | 0.612 | V |
| High-Side Switch On-Resistance | $I_{SW}$=100mA | | 80 | | mΩ |
| Low-Side Switch On-Resistance | $I_{SW}$=-100mA | | 50 | | mΩ |
| Upper Switch Current Limit | | 3 | | | A |
| Over Voltage Protection Threshold | | | 6.1 | | V |
| Switching Frequency | | | 1.2 | | MHz |
| Maximum Duty Cycle | | | 100 | | % |
| EN Rising Threshold | | 1.2 | | | V |
| EN Falling Threshold | | | | 0.6 | V |
| Under-Voltage Lockout Threshold | Wake up $V_{IN}$ Voltage | | 2.5 | 2.6 | V |
| | Shutdown $V_{IN}$ Voltage | 1.8 | 1.9 | | V |
| | Hysteresis $V_{IN}$ voltage | | 600 | | mV |
| Soft Start | | | 1 | | mS |
| Thermal Shutdown | | | 160 | | ℃ |
| Thermal Hysteresis | | | 30 | | ℃ |

Note (1): MOSFET on-resistance specifications are guaranteed by correlation to wafer level measurements.

Note (2): Thermal shutdown specifications are guaranteed by correlation to the design and characteristics analysis.

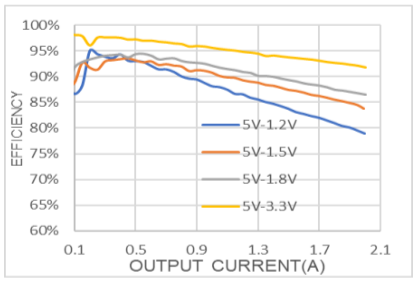
## Typical Performance Characteristics (1)(2)

Note (1): Performance waveforms are tested on the evaluation board.

Note (2): $V_{IN}$ =5V, $T_A$ = +25°C, unless otherwise noted.

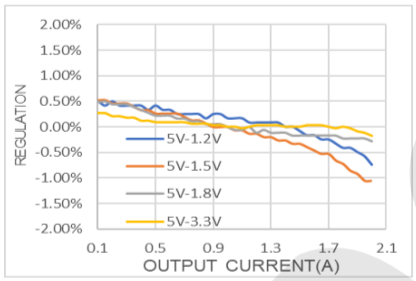
**Efficiency vs Load Current**

$V_{IN}$=5V, $V_{OUT}$=1.2V/1.5V/1.8V/3.3V



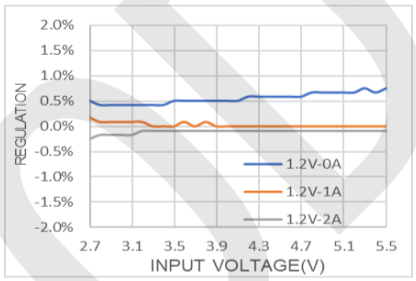

**Load Regulation**

$V_{IN}$=5V, $V_{OUT}$=1.2V/1.5V/1.8V/3.3V



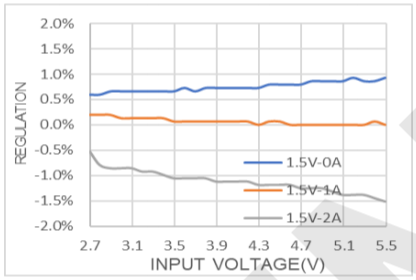

**Line Regulation**

$V_{OUT}$=1.2V



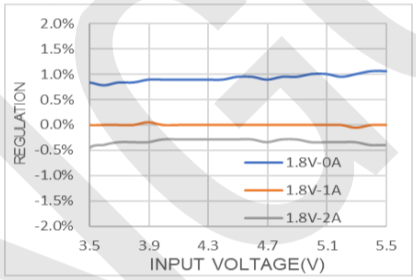

**Line Regulation**

$V_{OUT}$=1.5V



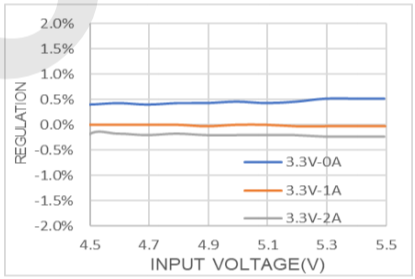

**Line Regulation**

$V_{OUT}$=1.8V



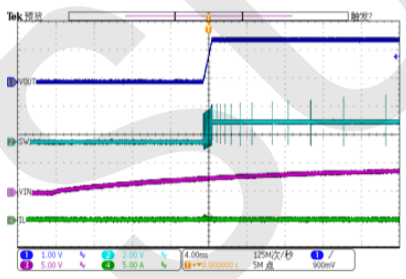

**Line Regulation**

$V_{OUT}$=3.3V



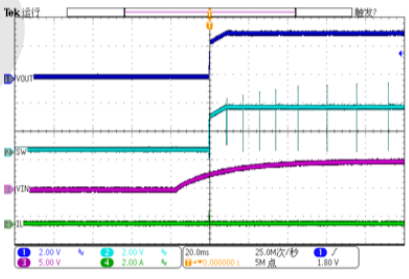

**Power Up at No Load**

$V_{IN}$=5V, $V_{OUT}$=1.2V, $I_{OUT}$=0A



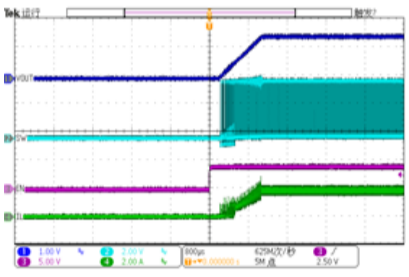
**Power Up at No Load**

$V_{IN}$=5V, $V_{OUT}$=3.3V, $I_{OUT}$=0A



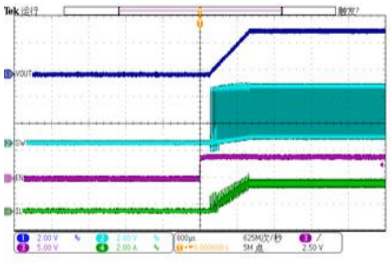
**Enable Startup at Full Load**

$V_{IN}$=5V, $V_{OUT}$=1.2V, $I_{OUT}$=2A



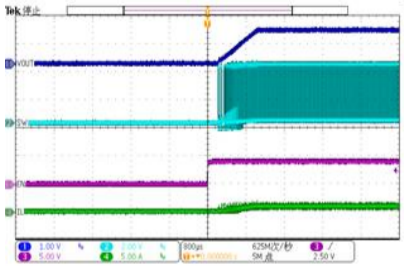
**Enable Startup at Full Load**

$V_{IN}$=5V, $V_{OUT}$=3.3V, $I_{OUT}$=2A



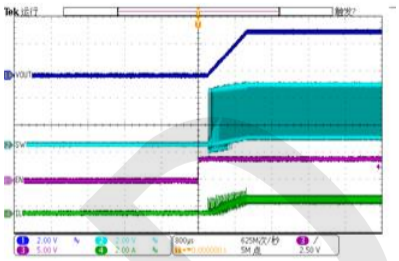
**Enable Startup at Half Load**

$V_{IN}$=5V, $V_{OUT}$=1.2V, $I_{OUT}$=1A



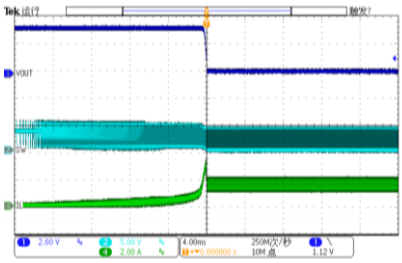
**Enable Startup at Half Load**

$V_{IN}$=5V, $V_{OUT}$=3.3V, $I_{OUT}$=1A



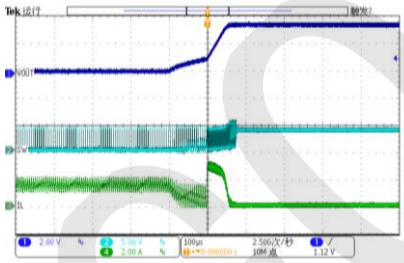
**Short Circuit Entry**

$V_{IN}$=5V, $V_{OUT}$=3.3V



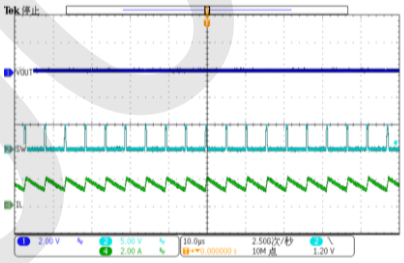
**Short Circuit Recovery**

$V_{IN}$=5V, $V_{OUT}$=3.3V

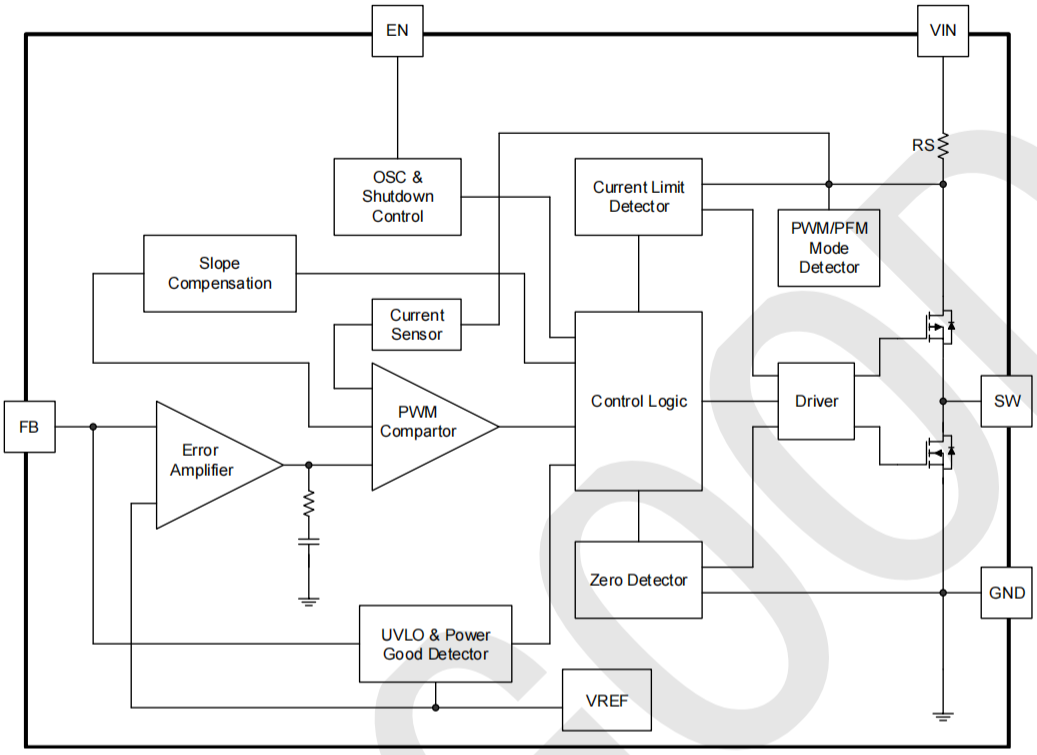


**Output Short**

$V_{IN}$=5V, $V_{OUT}$=3.3V



## Single Channel Functional Block Diagram




Block Diagram

## Functions Description

### Feature Description

EA3059 is a highly efficient and integrated Power Management IC for Systems-on-a-Chip (SoCs), ASICs, and processors. The device incorporates 4 high-efficiency synchronous buck regulators.

Each of the buck regulators is specially designed for high-efficiency operation throughout the load range. With 1.2MHz typical switching frequency, the external LC filter can be small and still provide very low output voltage ripple. The bucks are internally compensated to be stable with the recommended external inductors and capacitors as detailed in the application diagram. Synchronous rectification yields high efficiency for low voltage and high output currents.

Additional features include soft-start, under-voltage lockout, bypass, and current and thermal overload protection.

4 channel BUCKs are nearly identical in performance and mode of operation. They can operate in automatic mode (PFM/PWM). At very light loads, BUCKs enter PFM mode and operate with reduced switching frequency and supply current to maintain high efficiency.

### Internal Regulator

The EA3059 is a 4-channel current mode step down DC/DC converter that provides excellent transient response with no extra external compensation components. This device contains an internal, low resistance, high voltage power MOSFET, and operates at a high 1.2MHz operating frequency to ensure a compact, high efficiency design with excellent performance.

### Current Limit

A current limit feature protects the device and any external components during overload conditions. In PWM mode the current limiting is implemented by using an internal comparator that trips at current levels according to the buck capability. If the output is shorted to ground the device enters a timed current limit mode where the NFET is turned on for a longer duration until the inductor current falls below a low threshold, ensuring inductor current has more time to decay, thereby preventing runaway.

### Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. UVLO protection monitors the internal regulator voltage. When the voltage is lower than UVLO threshold voltage, the device is shut off. When the voltage is higher than UVLO threshold voltage, the device is enabled again.

### Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds 160°C, it shuts down the whole chip. When the temperature falls below its lower threshold (Typ. 130°C) the chip is enabled again.

### Internal Soft-Start

The soft-start is implemented to prevent the converter output voltage from overshooting during startup. When the chip starts, the internal circuitry generates a soft-start voltage (SS) ramping up from 0V to 0.6V. When it is lower than the internal reference (REF), SS overrides REF so the error amplifier uses SS as the reference. When SS is higher than REF, REF regains control. The SS time is internally to 1ms.

# Applications Information

## Setting the Output Voltage

Each channel requires an input capacitor, an output capacitor and an inductor. These components are critical to the performance of the device. EA3059 are internally compensated and do not require external components to achieve stable operation. The output voltage can be programmed by resistor divider.

$$V_{OUT} = V_{FB} \times \frac{R1 + R2}{R2}$$

When sizing R2, in order to achieve low current consumption and acceptable noise sensitivity, use a maximum of 200kΩ for R2. Larger currents through R2 improve noise sensitivity and output voltage accuracy but increase current consumption.

## Selecting the Inductor

The recommended inductor values are shown in the Application Diagram. It is important to guarantee the inductor core does not saturate during any foreseeable operational situation. The inductor should be rated to handle the maximum inductor peak current: Care should be taken when reviewing the different saturation current ratings that are specified by different manufacturers. Saturation current ratings are typically specified at 25°C, so ratings at maximum ambient temperature of the application should be requested from the manufacturer. The inductor value can be calculated with:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times F_{OSC}}$$

Where $\Delta I_L$ is the inductor ripple current. Choose inductor ripple current to be approximately 30% to 40% of the maximum load current. The maximum inductor peak current can be estimated as:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

Under light load conditions below 100mA, larger inductance is recommended for improved efficiency. Larger inductances lead to smaller ripple currents and voltages, but they also have larger physical dimensions, lower saturation currents and higher linear impedance. Therefore, the choice of inductance should be compromised according to the specific application.

## Selecting the Input Capacitor

The input current to the step-down converter is discontinuous and therefore requires a capacitor to supply AC current to the step-down converter while maintaining the DC input voltage. For a better performance, use ceramic capacitors placed as close to VIN as possible and a 0.1μF input capacitor to filter out high frequency interference is recommended. Capacitors with X5R and X7R ceramic dielectrics are recommended because they are stable with temperature fluctuations.

The capacitors must also have a ripple current rating greater than the maximum input ripple current of the converter. The input ripple current can be estimated with Equation:

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

From the above equation, it can be concluded that the input ripple current reaches its maximum at $V_{IN}$=2$V_{OUT}$ where $I_{CIN} = \frac{I_{OUT}}{2}$. For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitance value determines the input voltage ripple of the converter. If there is an input voltage ripple requirement in the system, choose the input capacitor that meets the specification. The input voltage ripple can be estimate with Equation:

$$\Delta V_{IN} = \frac{I_{OUT}}{F_{OSC} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Similarly, when $V_{IN}$=2$V_{OUT}$, input voltage ripple reaches its maximum of $\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{F_{OSC} \times C_{IN}}$.

## Selecting the Output Capacitor

An output capacitor is required to maintain the DC output voltage. The output voltage ripple can be estimated with Equation:

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{OSC} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times F_{OSC} \times C_{OUT}}\right)$$

There are some differences between different types of capacitors. In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. For simplification, the output voltage ripple can be estimated with Equation:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times {F_{OSC}}^2 \times L \times C_{OUT}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

A larger output capacitor can achieve a better load transient response, but the maximum output capacitor limitation should also be considered in the design application. If the output capacitor value is too high, the output voltage will not be able to reach the design value during the soft-start time and will fail to regulate. The maximum output capacitor value ($C_{OUT\_MAX}$) can be limited approximately with Equation:

$$C_{OUT\_MAX} = (I_{LIM\_AVG} - I_{OUT}) \times T_{SS}/V_{OUT}$$

Where $L_{LIM\_AVG}$ is the average start-up current during the soft-start period, and $T_{SS}$ is the soft- start time.

On the other hand, special attention should be paid when selecting these components. The DC bias of these capacitors can result in a capacitance value that falls below the minimum value given in the recommended capacitor specifications table.

The ceramic capacitor's actual capacitance can vary with temperature. The capacitor type X7R, which operates over a temperature range of −55°C to +125°C, will only vary the capacitance to within ±15%. The capacitor type X5R has a similar tolerance over a reduced temperature range of −55°C to +85°C. Many large value ceramic capacitors, larger than 1uF are manufactured with Z5U or Y5V temperature characteristics. Their capacitance can drop by more than 50% as the temperature varies from 25°C to 85°C. Therefore, X5R or X7R is recommended over Z5U and

Y5V in applications where the ambient temperature will change significantly above or below 25°C.

### Feed-Forward Capacitor ($C_{FF}$)

EA3059 has internal loop compensation, so adding $C_{FF}$ is optional. Specifically, for specific applications, if necessary, consider whether to add feed-forward capacitors according to the situation.

The use of a feed-forward capacitor ($C_{FF}$) in the feedback network is to improve the transient response or higher phase margin. For optimizing the feed-forward capacitor, knowing the cross frequency is the first thing. The cross frequency (or the converter bandwidth) can be determined by using a network analyzer. When getting the cross frequency with no feed-forward capacitor identified, the value of feed-forward capacitor ($C_{FF}$) can be calculated with the following Equation:

$$C_{FF} = \frac{1}{2\pi \times F_{CROSS}} \times \sqrt{\frac{1}{R1} \times \left(\frac{1}{R1} + \frac{1}{R2}\right)}$$

Where $F_{CROSS}$ is the cross frequency.

To reduce transient ripple, the feed-forward capacitor value can be increased to push the cross frequency to higher region. Although this can improve transient response, it also decreases phase margin and cause more ringing. In the other hand, if more phase margin is desired, the feed-forward capacitor value can be decreased to push the cross frequency to lower region.

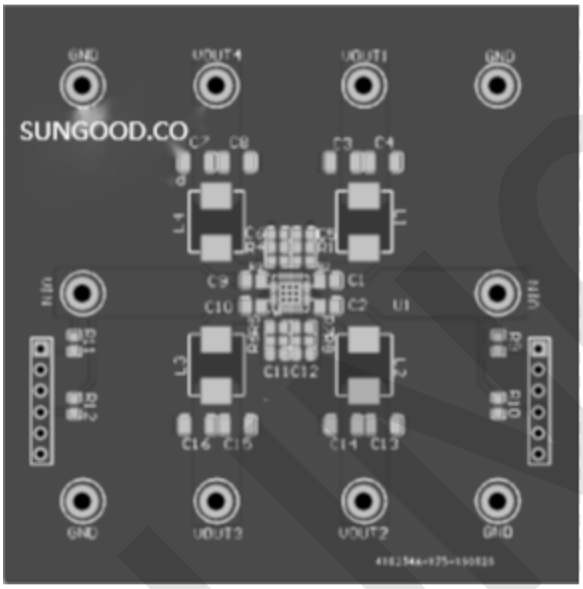
## PC Board Layout Consideration

PCB layout is very important to achieve stable operation. It is highly recommended to duplicate EVB layout for optimum performance. If change is necessary, please follow these guidelines for reference.

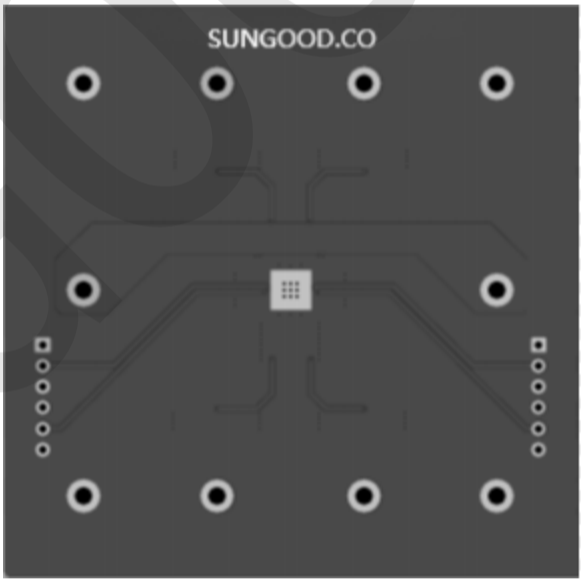
1. Keep the path of switching current short and minimize the loop area formed by Input capacitor, high-side MOSFET and low-side MOSFET.
2. Bypass ceramic capacitors are suggested to be put close to the $V_{IN}$ Pin.
3. Ensure all feedback connections are short and direct. Place the feedback resistors and compensation components as close to the chip as possible.
4. $V_{OUT}$, SW away from sensitive analog areas such as FB.

Connect IN, SW, and especially GND respectively to a large copper area to cool the chip to improve thermal performance and long-term reliability.

Top Layer

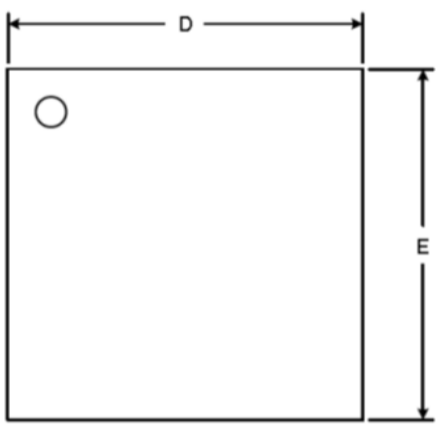


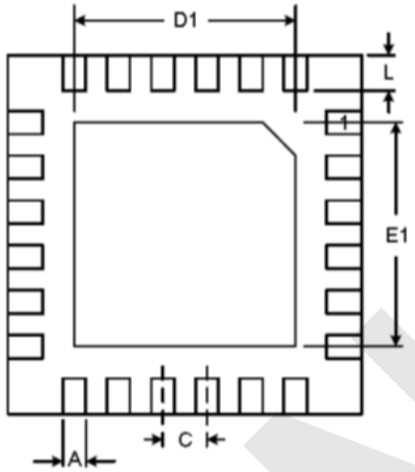

Bottom Layer



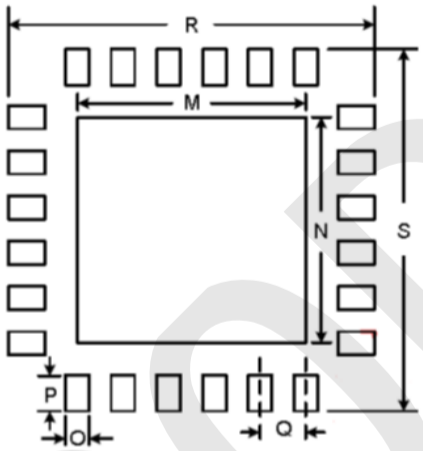

Sample Board Layout

## Package Description

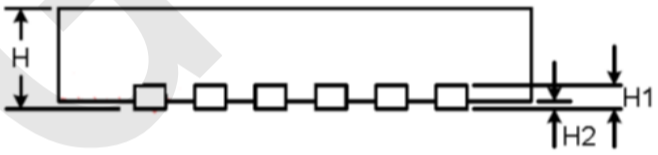



Bottom View




Recommended Power Pattern




Side View

## Package Outline and Dimensions

| | Dimension | | Dimension | |
|---|---|---|---|---|
| **Symbol** | **Min** | **Max** | **Symbol** | **Typ** |
| A | 0.18 | 0.3 | M | 2.6 |
| C | 0.45 | 0.55 | N | 2.6 |
| D | 3.95 | 4.05 | O | 0.3 |
| E | 3.95 | 4.05 | P | 0.8 |
| D1 | 2.3 | 2.7 | Q | 0.5 |
| E1 | 2.3 | 2.7 | R | 4.7 |
| L | 0.35 | 0.45 | S | 4.7 |
| H | 0.8 | 1 | | |
| H1 | 0.17 | 0.25 | | |
| H2 | 0 | 0.25 | | |

Unit: mm