NL17SZ374

Product Preview

Single D-Type Flip-Flop

The NL17SZ374 is a single positive edge–triggered D–Type Flip–Flop in a tiny footprint package. The SC70–6/SC–88 occupies a very small board area. The device performs much as LCX multi–gate products in speed and drive.

- Tiny SC70–6/SC–88 Package
- TPD(MAX) < 5.0 nsecs at 3.0 Volts
- Source/Sink 24 mA at 3.0 Volts
- Over–Voltage Tolerant Inputs and Outputs
- Pin For Pin with NC7SZ374
- Chip Complexity: FETs = TBD

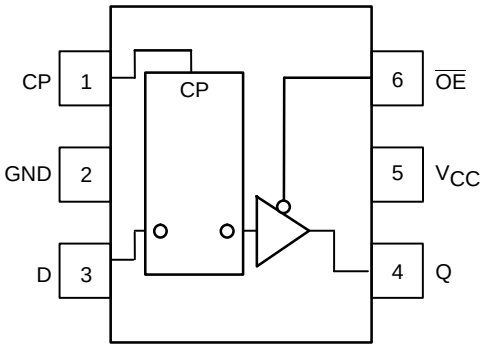

Figure 1. Pinout (Top View)

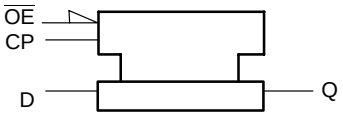

Figure 2. Logic Symbol

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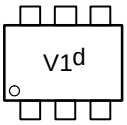
MARKING DIAGRAMS

SC–88/SOT–363/SC70–6
DF SUFFIX
CASE 419B



Pin 1

d = Date Code

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

PIN ASSIGNMENT

Pin	Function
D	Data Input
CP	Clock Pulse Input
$\overline{OE}$	Output Enable Input
Q	Flip–Flop Output

FUNCTION TABLE

Inputs			Output
CP	**D**	**$\overline{OE}$**	**Q**
∫	L	L	L
∫	H	L	H
⌊	X	L	Q_n
X	X	H	Z

H = HIGH Logic Level
L = LOW Logic Level
Z= High Impedance
Q_n = No Change in Data
X = Immaterial

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage		−0.5 to +7.0	V
V_{IN}	DC Input Voltage		−0.5 to +7.0	V
V_{OUT}	DC Output Voltage		−0.5 to +7.0	V
I_{IK}	DC Input Diode Current		−50	mA
I_{OK}	DC Output Diode Current		−50	mA
I_{OUT}	DC Output Sink Current		±50	mA
I_{CC}	DC Supply Current per Supply Pin		±100	mA
T_{STG}	Storage Temperature Range		−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds		260	°C
T_J	Junction Temperature Under Bias		+150	°C
θ_{JA}	Thermal Resistance	SC–70/SC–88A (Note 1) TSOP–5	350 230	°C/W
P_D	Power Dissipation in Still Air at 85°C	SC–70/SC–88A TSOP–5	150 200	mW
MSL	Moisture Sensitivity		Level 1	
F_R	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V–0 @ 0.125 in	
V_{ESD}	ESD Withstand Voltage	Human Body Model (Note 2) Machine Model (Note 3) Charged Device Model (Note 4)	>2000 >200 N/A	V
$I_{Latch–Up}$	Latch–Up Performance	Above V_{CC} and Below GND at 85°C (Note 5)	UL 94 V–0 @ 0.125 in	

Maximum Ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum–rated conditions is not implied. Functional operation should be restricted to the Recommended Operating Conditions.

1. Measured with minimum pad spacing on an FR4 board, using 10 mm–by–1 inch, 2–ounce copper trace with no air flow.
2. Tested to EIA/JESD22–A114–A.
3. Tested to EIA/JESD22–A115–A.
4. Tested to JESD22–C101–A.
5. Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage		2.0	5.5	V
V_{IN}	DC Input Voltage		0	5.5	V
V_{OUT}	DC Output Voltage		0	5.5	V
T_A	Operating Temperature Range		−40	+85	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 3.0 V ±0.3 V V_{CC} = 5.0 V ±0.5 V	0 0	100 20	ns/V

DEVICE JUNCTION TEMPERATURE VERSUS TIME TO 0.1% BOND FAILURES

Junction Temperature °C	Time, Hours	Time, Years
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

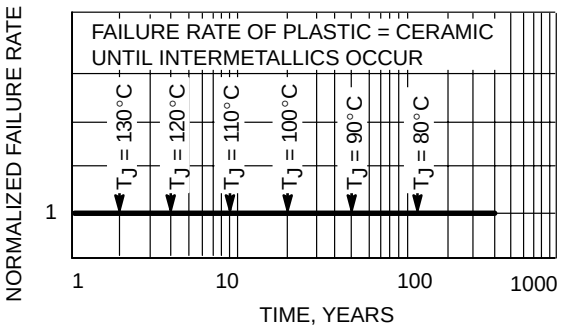


Figure 3. Failure Rate vs. Time Junction Temperature

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Condition	V_{CC} (V)	T_A = 25°C			−40°C ≤ T_A ≤ 85°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	High–Level Input Voltage		2.3 to 5.5	0.7 V_{CC}			0.7 V_{CC}		V
V_{IL}	Low–Level Input Voltage		2.3 to 5.5			0.3 V_{CC}		0.3 V_{CC}	V
V_{OH}	High–Level Output Voltage	I_{OH} = 100 μA	2.3 to 5.5	V_{CC} – 0.1	V_{CC}		V_{CC} – 0.1		V
	V_{IN} = V_{IL} or V_{IH}	I_{OH} = –8 mA	2.3	1.9	2.1		1.9		
		I_{OH} = –12 mA	2.7	2.2	2.4		2.2		
		I_{OH} = –16 mA	3.0	2.4	2.7		2.4		
		I_{OH} = –24 mA	3.0	2.3	2.5		2.3		
		I_{OH} = –32 mA	4.5	3.8	4.0		3.8		
V_{OL}	Low–Level Output Voltage	I_{OL} = 100 μA	2.3 to 5.5			0.1		0.1	V
	V_{IN} = V_{IH} or V_{OH}	I_{OL} = 8 mA	2.3		0.20	0.3		0.3	
		I_{OL} = 12 mA	2.7		0.22	0.4		0.4	
		I_{OL} = 16 mA	3.0		0.28	0.4		0.4	
		I_{OL} = 24 mA	3.0		0.38	0.55		0.55	
		I_{OL} = 32 mA	4.5		0.42	0.55		0.55	
I_{IN}	Input Leakage Current	V_{IN} = V_{CC} or GND	0 to 5.5			±0.1		±1.0	μA
I_{OFF}	Power Off–Output Leakage Current	V_{OUT} = 5.5 V	0			1		10	μA
I_{CC}	Quiescent Supply Current	V_{IN} = V_{CC} or GND	5.5			1		10	μA

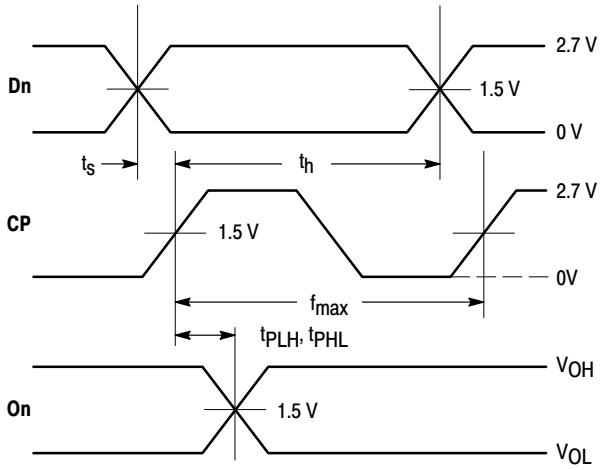
AC ELECTRICAL CHARACTERISTICS t_R = t_F = 3.0 ns

Symbol	Parameter	Condition	V_{CC} (V)	T_A = 25°C			−40°C ≤ T_A ≤ 85°C		Unit
				Min	Typ	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	R_L = 500 MΩ, C_L = 50 pF	2.5 ± 0.2				125		MHz
			3.3 ± 0.3				150		
			5.0 ± 0.5				175		
t_{plh} t_{phl}	Propagation Delay CP to Q (Figure 6)	R_L = 1 MΩ, C_L = 15 pF	2.5 ± 0.2	2.0	3.8	6.5	2.0	7.0	ns
		R_L = 1 MΩ, C_L = 15 pF	3.3 ± 0.3	1.5	2.8	4.5	1.4	5.0	
		R_L = 500 Ω, C_L = 50 pF		2.0	3.4	5.5	1.6	6.2	
		R_L = 1 MΩ, C_L = 15 pF	5.0 ± 0.5	1.0	2.2	3.5	1.0	3.8	
		R_L = 500 Ω, C_L = 50 pF		1.5	2.6	4.0	1.4	4.7	
t_{pzl} t_{pzh}	Output Enable Time (Figure 7)	R_L = 250 Ω, C_L = 50 pF	2.5 ± 0.2	2.0	3.7	6.0	1.8	6.6	ns
			3.3 ± 0.3	1.5	2.8	5.0	1.4	5.3	
			5.0 ± 0.5	1.0	2.2	3.7	1.0	3.9	
t_{plz} t_{phz}	Output Disable Time (Figure 8)	R_L and R1 = 500 Ω, C_L = 50 pF	2.5 ± 0.2	2.0	3.5	6.0	1.8	6.3	ns
			3.3 ± 0.3	1.5	2.8	4.5	1.4	4.7	
			5.0 ± 0.5	1.0	2.3	3.7	1.0	3.9	
t_S	Setup Time CP to D (Figure 6)	R_L = 500 Ω, C_L = 50 pF	2.5 ± 0.2				2.5		ns
			3.3 ± 0.3				2.0		
			5.0 ± 0.5				1.5		
t_H	Hold Time CP to D (Figure 6)	R_L = 500 Ω, C_L = 50 pF	2.5 ± 0.2				1.5		ns
			3.3 ± 0.3				1.5		
			5.0 ± 0.5				1.5		
t_W	CP Pulse Width (Figure 6)	R_L = 500 Ω, C_L = 50 pF	2.5 ± 0.2				3.0		ns
			3.3 ± 0.3				2.8		
			5.0 ± 0.5				2.5		

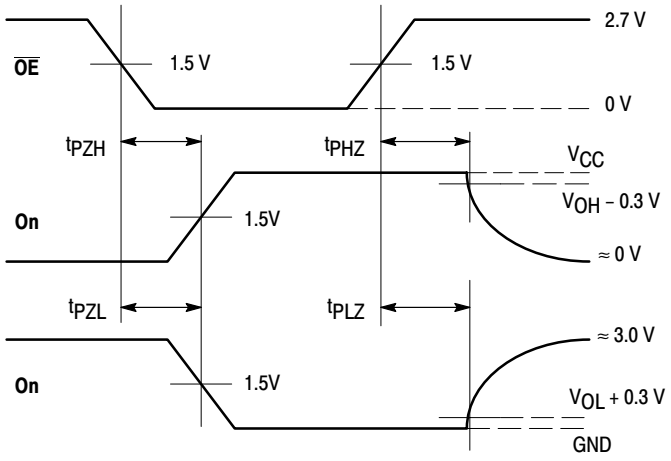
CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Unit
C_{IN}	Input Capacitance	V_{CC} = 5.5 V, V_I = 0 V or V_{CC}	4.0	pF
C_{OUT}	Output Capacitance	V_{CC} = 5.5 V, V_O = 0 V or V_{CC}	4.0	pF
C_{PD}	Power Dissipation Capacitance (Note 6)	10 MHz, V_{CC} = 3.3 V, V_I = 0 V or V_{CC}	25	pF
		10 MHz, V_{CC} = 5.5 V, V_I = 0 V or V_{CC}	30	

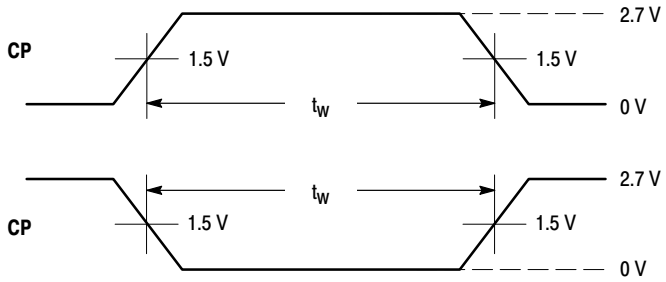
6. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.



WAVEFORM 1 – PROPAGATION DELAYS, SETUP AND HOLD TIMES
$t_R = t_F$ = 2.5 ns, 10% to 90%; f = 1 MHz; t_W = 500 ns



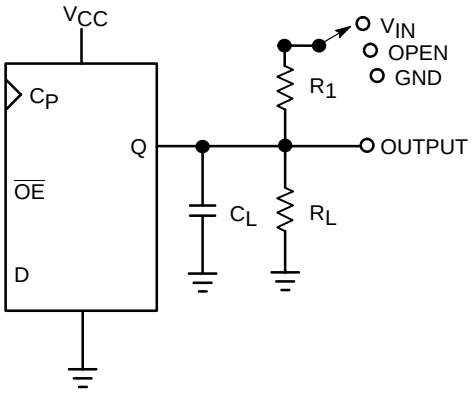
WAVEFORM 2 – OUTPUT ENABLE AND DISABLE TIMES
$t_R = t_F$ = 2.5 ns, 10% to 90%; f = 1 MHz; t_W = 500 ns



WAVEFORM 3 – PULSE WIDTH
$t_R = t_F$ = 2.5 ns (or fast as required) from 10% to 90%;
Output requirements: $V_{OL} \le 0.8$ V, $V_{OH} \ge 2.0$ V

Figure 4. AC Waveforms

TEST CIRCUITS



CL includes load and stray capacitance Input

Figure 5.

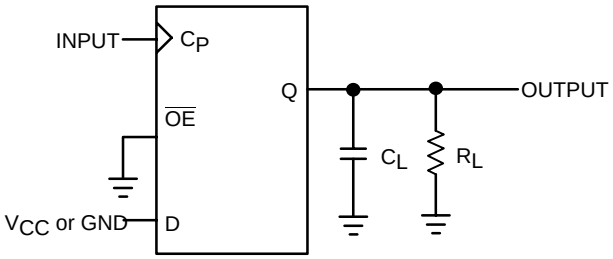


Figure 6.

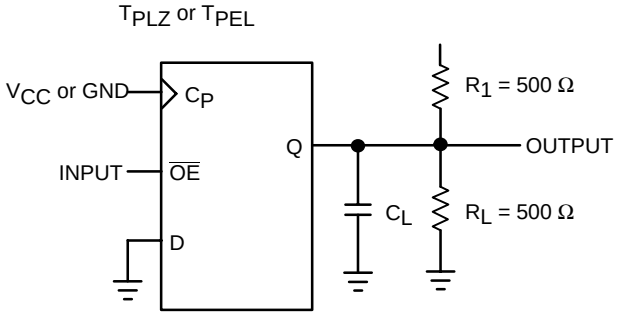


Figure 7.

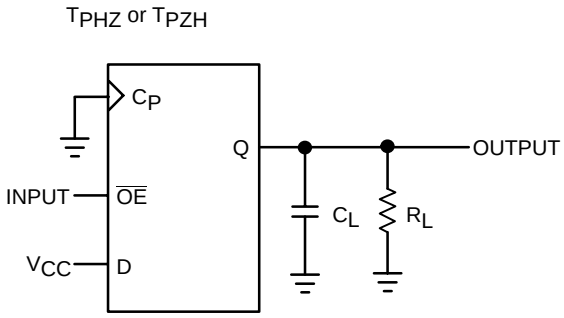


Figure 8.

DEVICE ORDERING INFORMATION

Device Order Number	Device Nomenclature							Package Type	Tape and Reel Size
	Logic Circuit Indicator	No. of Gates per Package	Temp Range Identifier	Technology	Device Function	Package Suffix	Tape and Reel Suffix		
NL17SZ374DFT2	NL	1	7	SZ	374	DF	T2	SC–88/ SOT–363/ SC70–6	178 mm, 3000 Units

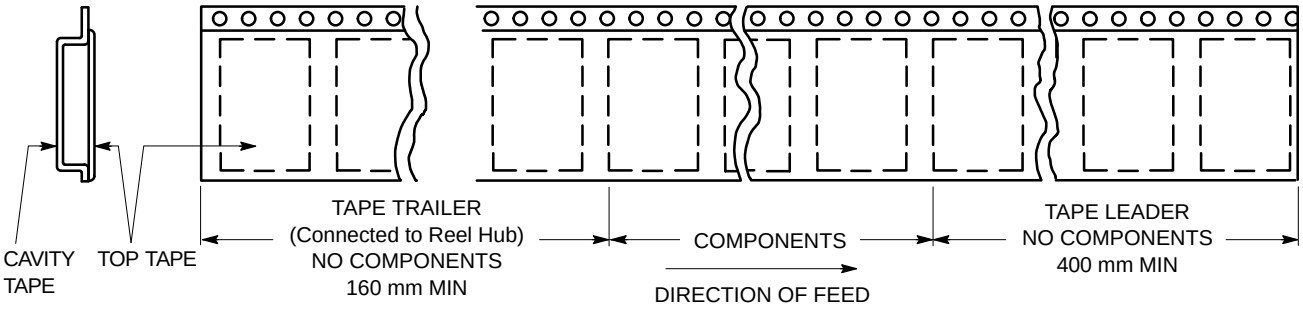


Figure 9. Tape Ends for Finished Goods

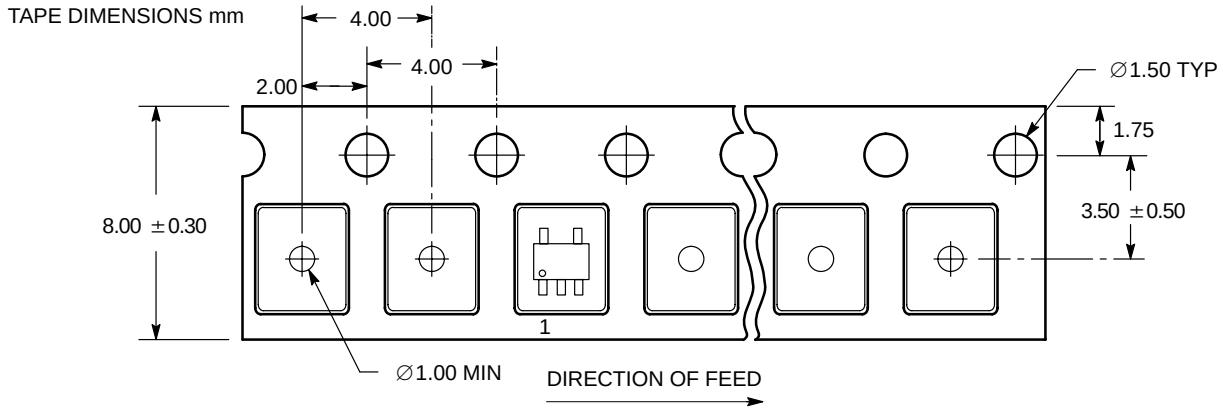


Figure 10. SC−70/SC−88A/SOT−353 DFT2 Reel Configuration/Orientation

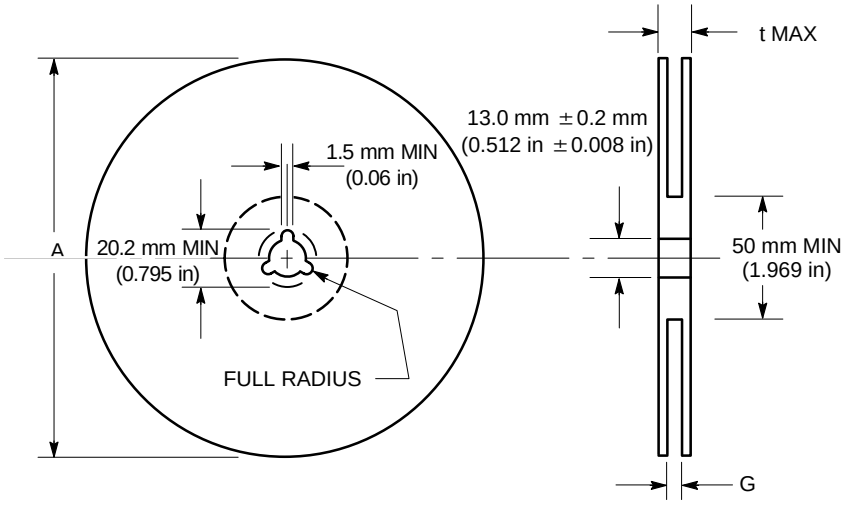


Figure 11. Reel Dimensions

REEL DIMENSIONS

Tape Size	T and R Suffix	A Max	G	t Max
8 mm	T1, T2	178 mm (7 in)	8.4 mm, + 1.5 mm, –0.0 (0.33 in + 0.059 in, –0.00)	14.4 mm (0.56 in)

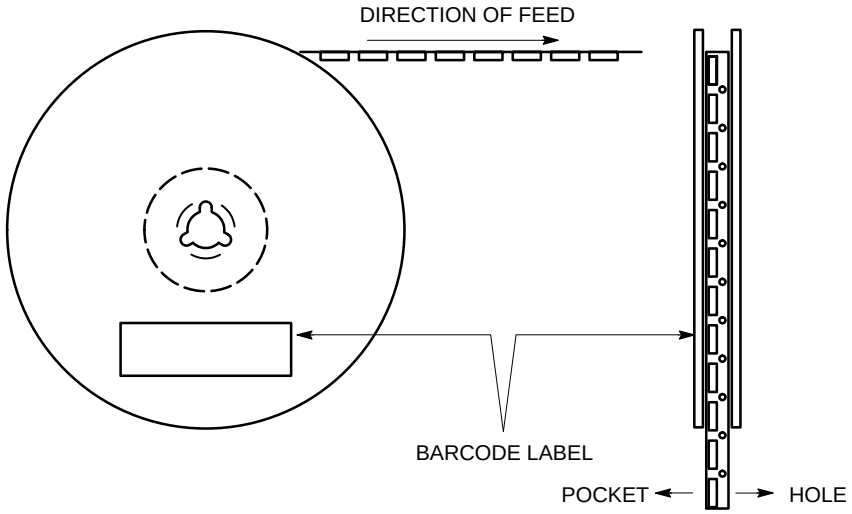
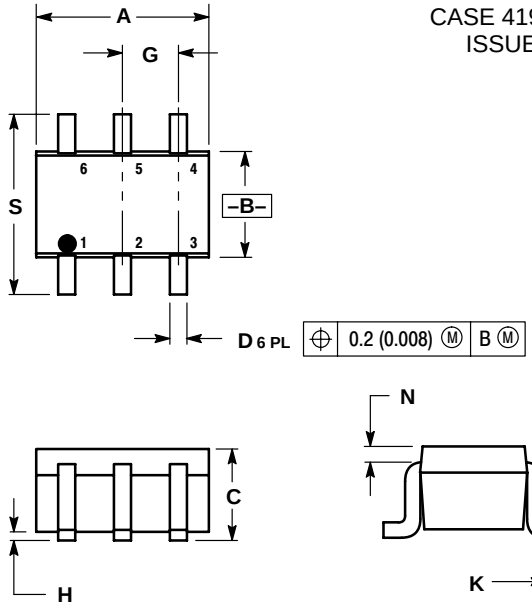


Figure 12. Reel Winding Direction

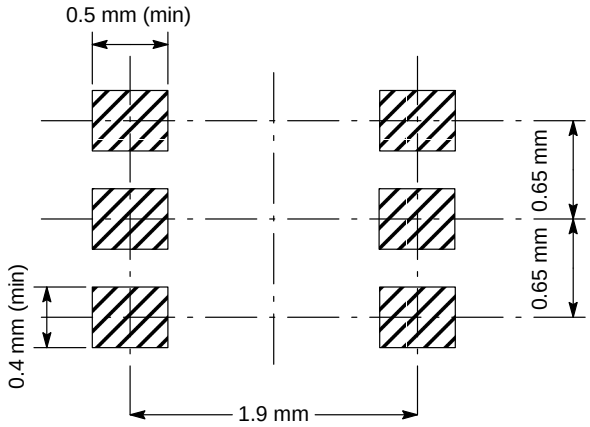
PACKAGE DIMENSIONS

SC70–6/SC–88/SOT–363
DF SUFFIX
6–LEAD PACKAGE
CASE 419B–02
ISSUE H



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026 BSC		0.65 BSC	
H	---	0.004	---	0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20 REF	
S	0.079	0.087	2.00	2.20



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