Triple-Output AMOLED Display Power Supply

■ General Description

The OCP2133 is designed to drive AMOLED displays (Active Matrix Organic Light Emitting Diode) requiring V(AVDD), V(ELVDD) and V(ELVSS). The device integrates a boost converter for V(ELVDD), an inverting buck-boost converter for V(ELVSS) and a boost converter for V(AVDD), which are suitable for battery operated products. The digital interface control pin(CTRL) allows programming V(AVDD), V(ELVDD) and V(ELVSS) in digital steps. The OCP2133 uses a novel technology enabling excellent line and load regulation.

■ Features

- 2.9V to 4.5V Input Voltage Range
- Synchronous Boost Converter (AVDD)
  5.8V to 7.9V Output Voltage (programmable)
  6.1V Default Output Voltage
  1% Accuracy
  80mA Output Current Capability
  135mA Output Current Protection
  V_I to V_O and V_O to V_I Isolation
- Synchronous Boost Converter (ELVDD)
  4.6V to 5V Output Voltage (programmable)
  4.6V Default Output Voltage
  0.5% Accuracy
  500mA Output Current Capability
  External Output Voltage Sensing Pin for Load Drop Compensation
  Excellent Line Transient Response
  V_I to V_O and V_O to V_I Isolation
- Synchronous Inverting Buck-Boost Converter （ELVSS）
  –5.4V to –1.4V Output Voltage（programmable）
  –2.5V Default Output Voltage
  1.2% Accuracy at –2.5 V (±30 mV)
  500mA Output Current Capability
  V_I to V_O and V_O to V_I Isolation
- Single-Wire Digital Interface for Programming
- Short Circuit Protection
- Thermal Shutdown
- Available in 3mm × 3mm x 0.75mm 16Pin QFN Package

■ Applications

- Cellular Phones
- Portable Media Players
- Ultra Mobile Devices
- GPS Receivers
- White LED Backlighting for Media Form Factor Display

■ Pin Configuration

QFN3X3-16L (TOP VIEW)

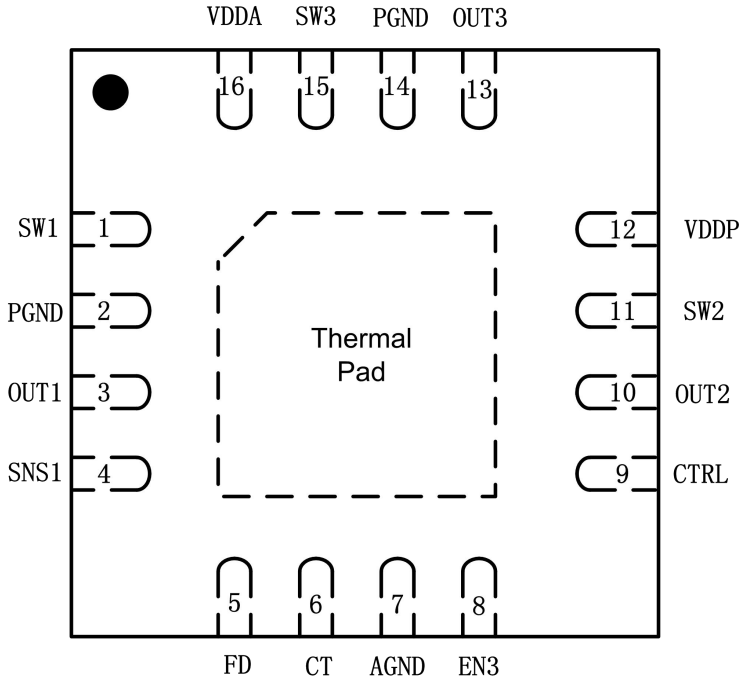


Figure 1, Pin Assignments of OCP2133

Pin Name	Pin No.	I/O	Pin Function
AGND	7	-	Analog ground
CT	6	I/O	Control of the ELVSS transition time.
CTRL	9	I	Enable ELVDD boost converter and delayed ELVSS inverting buck-boost converter. Digital programming.
EN3	8	I	Enable AVDD boost converter.
FD	5	I	Active discharge enables / disable during shut-down.
OUT1	3	O	Output of the ELVDD boost converter
OUT2	10	O	Output of the ELVSS inverting buck-boost converter.
OUT3	13	O	Output of the AVDD boost converter.
PGND	2	-	Power ground of the ELVDD boost converter.
PGND	14	-	Power ground of the AVDD boost converter.
SNS1	4	I	ELVDD sense input.
SW1	1	O	Switch pin of the ELVDD boost converter.
SW2	11	O	Switch pin of the ELVSS inverting buck-boost converter.
SW3	15	O	Switch pin of the AVDD boost converter.
VDDA	16	-	Supply for the internal analog circuits.
VDDP	12	-	Supply for ELVSS inverting buck-boost converter.
Thermal Pad	-	-	Connect this pad to AGND and PGND.

■ Typical Application Circuit

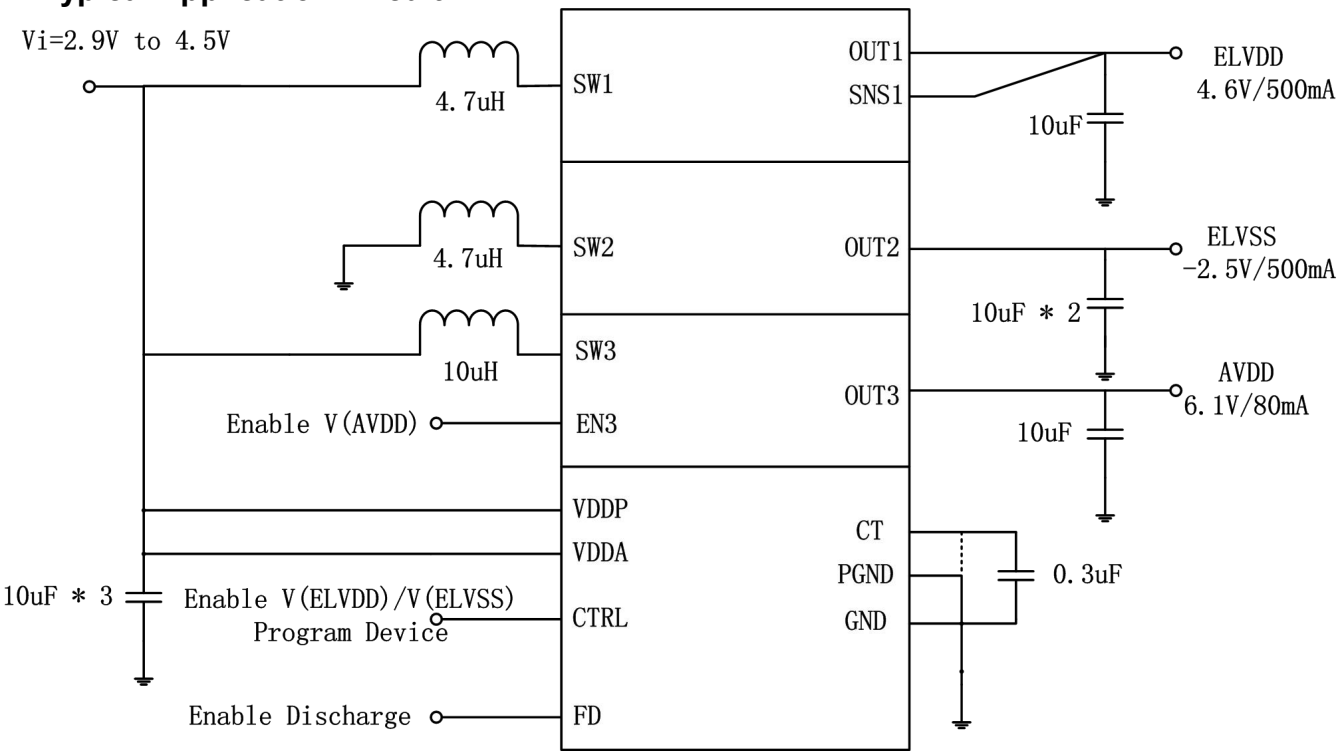


Figure 2, Typical Application Circuit of OCP2133

■ Block Diagram

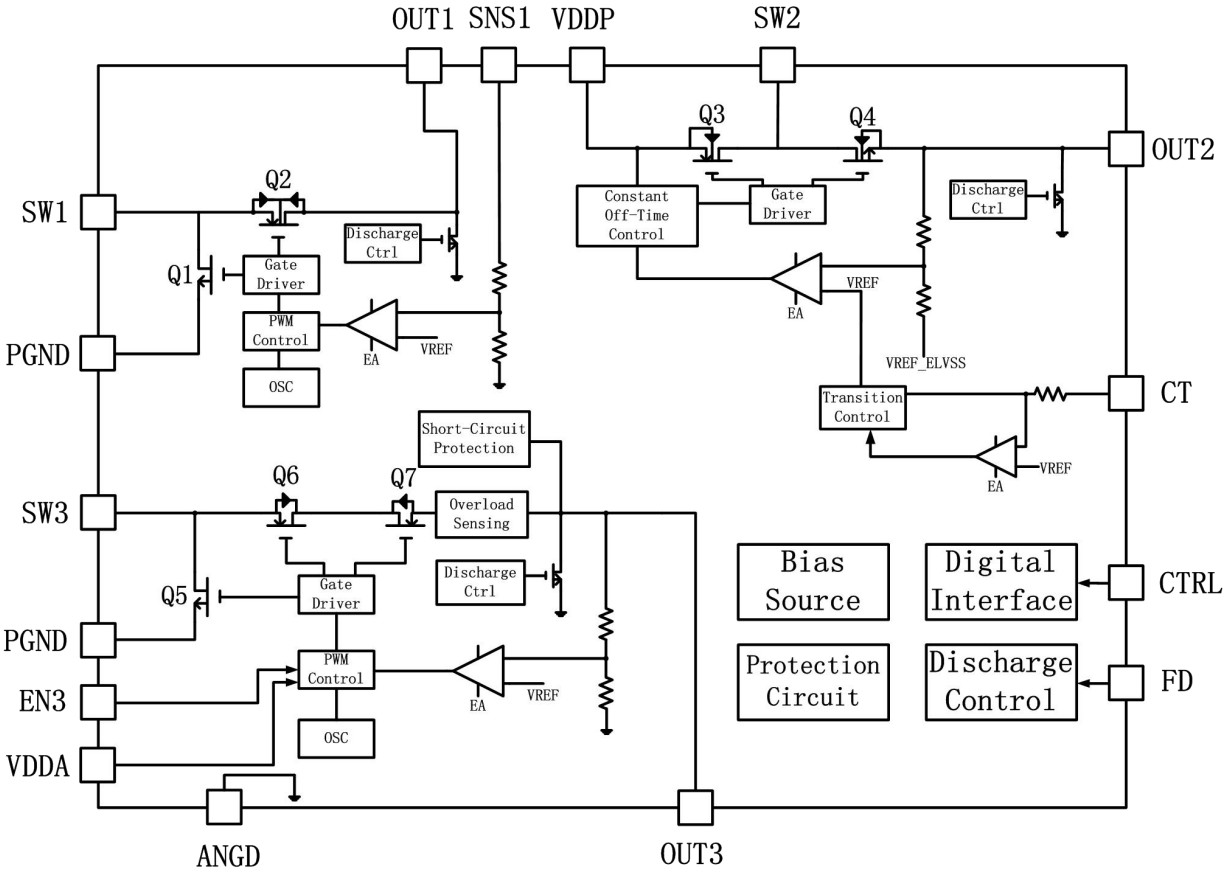


Figure 3, Block Diagram of OCP2133

■ Absolute Maximum Ratings (T_A=25°C, unless otherwise noted)

Parameter	Symbol	Rating	Unit
Supply Voltages on VIN	V_I	-0.3 to 6	V
V_{SW3} Pin to OUT3	V_{SW}	-0.3 to 10	V
OUT2	V_{OUT2}	-6.5 to 0.3	V
SW2	V_{SW2}	-6.5 to 5.5	
Operating Junction Temperature Range	T_J	–40 to 150	°C
Storage Temperature Range	T_{STG}	–65 to 150	°C
Maximum Soldering Temperature (at leads, 10 sec)	T_{LEAD}	300	°C

■ Recommended Operating Conditions

Parameter	Symbol	Rating	Unit
Input voltage range	VIN	2.9 to 4.5	V
Operating junction temperature	TJ	-40 to 125	°C
ELVDD BOOST CONVERTER (OUT1)			
ELVDD boost converter output voltage range	VO	4.6 to 5	V
Inductance	L	4.7	μH
Input capacitance placed at the inductor(1)	CI	10	μF
Output capacitance placed at OUT1 pin(1)	CO	10-22	μF
ELVSS INVERTING BUCK-BOOST CONVERTER (OUT2)			
ELVSS inverting buck-boost output voltage range	VO	-5.4 to -1.4	V
Inductance	L	4.7	μH
Input capacitance placed at VDDP pin(1)	C(VDDP)	10	μF
Output capacitance placed at OUT2 pin(1)	CO	10*2	μF
CT-pin capacitance(1)	C(CT)	300	nF
AVDD BOOST CONVERTER (OUT3)			
AVDD boost converter output voltage range	VO	5.8 to 7.9	V
Inductance	L	10	μH
Input capacitance placed at the inductor(1)	CI	10	μF
Output capacitance placed at OUT1 pin(1)	CO	10-22	μF

■ Electrical Characteristics

Typical limits tested at T_A= 25°C. Minimum and maximum limits apply over the full operating ambient temperature range (−40°C ≤ T_A ≤ 85°C). Unless otherwise specified, VIN= 3.7V, CTRL=VIN, EN3=VIN, ELVDD=4.6V, ELVSS=-2.5V, AVDD=6.1V.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
SUPPLY AND THERMAL PROTECTION						
VI	Input voltage range, VIN		2.9	-	4.5	V
ISD	Shutdown current	V(CTRL) = V(EN3) = GND, V(FD) = 3.7 V or GND	-		1	μA
UVLO	Under voltage lockout threshold	VIN Rising	-	2.5	2.7	V
Vhys	Under voltage lockout hysteresis		-	100	-	mV
LOGIC SIGNALS (EN3,CTRL,FD)						
VIH	logic high voltage(EN3，CTRL,FD)	VIN = 2.9 V to 4.5 V	1.2	-	-	V
VIL	logic low voltage(EN3，CTRL,FD)	VIN = 2.9 V to 4.5 V	-	-	0.4	V
RI	pull down resistor		-	460	-	kΩ

ELVDD BOOST CONVERTER(OUT1)						
VO	Output Voltage (OUT1)		4.6		5	V
	Output Voltage accuracy (OUT1)	T=25℃,No Load	-0.5%		0.5%	
RDS(on)	MOSFET on-state resistance (Q1)	IDS = 100 mA		250		mΩ
RDS(on)	MOSFET on-state resistance (Q2)	IDS = 100 mA		350		mΩ
	Current limit (Q1)	Inductor valley current	0.8	1	1.3	A
	Short-circuit threshold in operation (SNS1)	Percentage of nominal VO	85	90	95	%
	Voltage-sensing threshold (OUT1)	V(OUT1) – V(SNS1) increasing	200	300	450	mV
	Voltage-sensing threshold (SNS1)	V(OUT1) – V(SNS1) decreasing	100	200	350	mV
	Off current (combined) (OUT1, SNS1)	V(FD) = V(CTRL) = GND		0.8	5	μA
R(SNS1)	Pull-down resistance (SNS1)			1.6		MΩ
	Line regulation	IO = 100 mA, VI = 2.9 V to 4.5 V		0.01		%/V
	Load regulation	1 mA ≤ IO ≤ 300 mA		0.1		%/A
ELVSS INVERTING BUCK-BOOST CONVERTER (OUT2)						
VO	Output Voltage (OUT2)		-1.4	-2.5	-5.4	V
	Output Voltage accuracy (OUT2)	T=25℃,No Load	-30		30	mV
RDS(on)	MOSFET on-state resistance (Q3)	IDS = 100 mA		250		mΩ
RDS(on)	MOSFET on-state resistance (Q4)	IDS = 100 mA		300		mΩ
	Current limit (Q3)	Inductor peak current	1.5	2.2	3	A
	Short-circuit threshold in operation (OUT2)	Voltage rise from nominal VO	400	500	650	mV
	Discharge comparator threshold (OUT2)		-950	-700	-400	mV
	Off current (OUT2)	V(FD) = V(CTRL) = GND		0.01	5	μA
	Discharge resistance (OUT2)	V(CTRL) = GND, IO = 1 mA	130	150	175	Ω
R(CT)	Output resistance (CT)		150	325	500	kΩ
	Input threshold voltage (CT)	V(CT) rising	10	50	200	mV
	Line regulation	IO = 100 mA, VI = 2.9 V to 4.5 V		0.02		%/V
	Load regulation	1 mA ≤ IO ≤300 mA		0.5		%/A
AVDD BOOST CONVERTER (OUT3)						
VO	Output Voltage (OUT3)		5.8	6.1	7.9	V
	Output Voltage accuracy (OUT3)	T=25℃,No Load	-1%		1%	
RDS(on)	MOSFET on-state resistance (Q5)	IDS = 100 mA		500		mΩ
RDS(on)	MOSFET on-state resistance (Q6 and Q7)	IDS = 100 mA		1200		mΩ
	Current limit (Q5)	Inductor peak current	0.25	0.35	0.55	A
	Overload current threshold (OUT3)			135		mA
	Short-circuit threshold voltage (OUT3)	Percentage of nominal VO	85	90	95	%
	Off current (OUT3)	V(FD) = V(EN3) = GND		1.5	5	μA
	Discharge resistance (OUT3)	V(EN3) = GND, IO = 1 mA		30		Ω

	Line regulation	IO = 30 mA, VI = 2.9 V to 4.5 V		0.02		%/V
	Load regulation	1 mA ≤ IO ≤80 mA		-0.4		%/A
Timing Requirements						
CTRL INTERFACE						
tw	High-level pulse duration (CTRL)		2	10	25	µs
	Low-level pulse duration (CTRL)		2	10	25	µs
td(reset)	Reset time to ensure proper logic reset		100			µs

■ Switching Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
CTRL INTERFACE						
td(on)	Turn-on delay time			300	400	µs
td(off)	Turn-off delay time		30		80	µs
td(store)	Data storage / accept time period		30		80	µs
PROTECTION AND DISCHARGE						
td(short)	Short-circuit detection delay during start up (OUT1)			10		ms
	Short-circuit detection delay during operation (OUT1)			4		ms
	Short-circuit detection delay during start up (OUT2)			20		ms
	Short-circuit detection delay during operation (OUT2)			4		ms
	Short-circuit detection delay during operation (OUT3)			4		ms
td(overload)	Overload detection delay (OUT3)			4		ms
td(discharge)	Discharge time after CTRL goes high (OUT2)			10		ms
SWITCHING FREQUENCY						
	AVDD boost converter switching frequency	IO = 30 mA	1.3	1.6	1.75	MHz
	ELVDD boost converter switching frequency	IO = 100 mA	1.3	1.6	1.75	MHz
	ELVSS inverting buck-boost converter frequency	IO = 100 mA		1.6		MHz
ELVSS BUCK-BOOST CONVERTER TRANSITION TIME CONTROL (CT)						
	Transition time programmed to 'fast'	VO = –2.5 V to –3 V		500		us
	Transition time programmed to 12 ms			12		ms

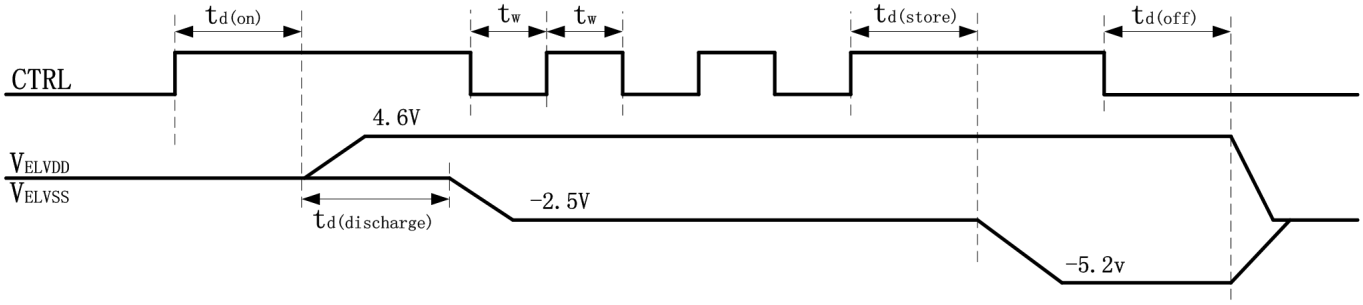
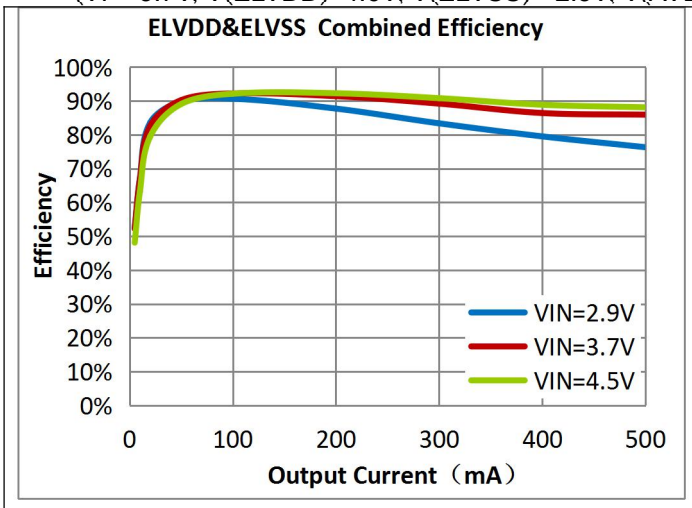
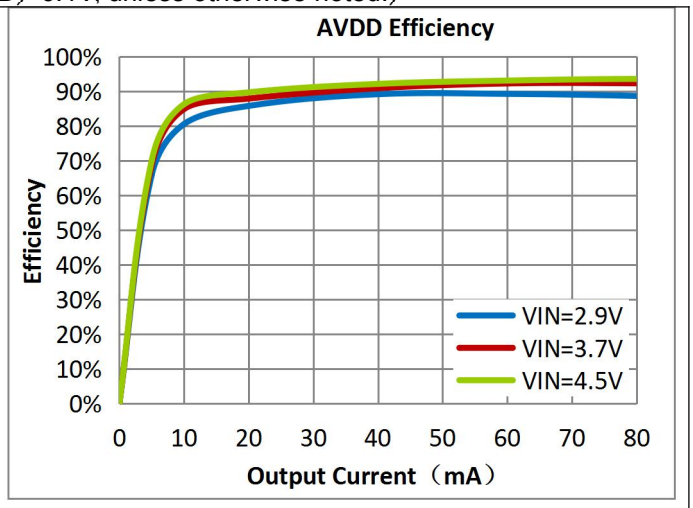


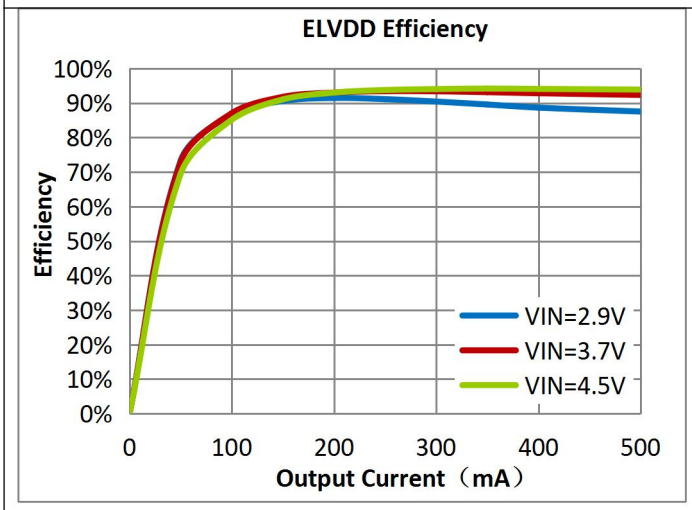
Figure 4. Timing Diagram

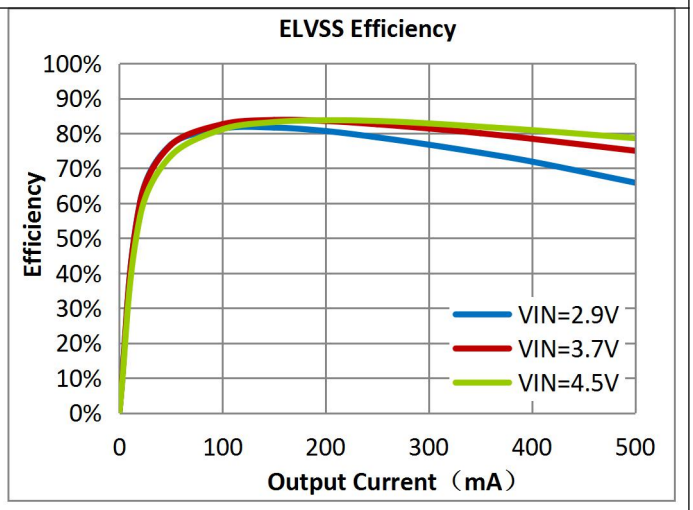
■ Typical Characteristic

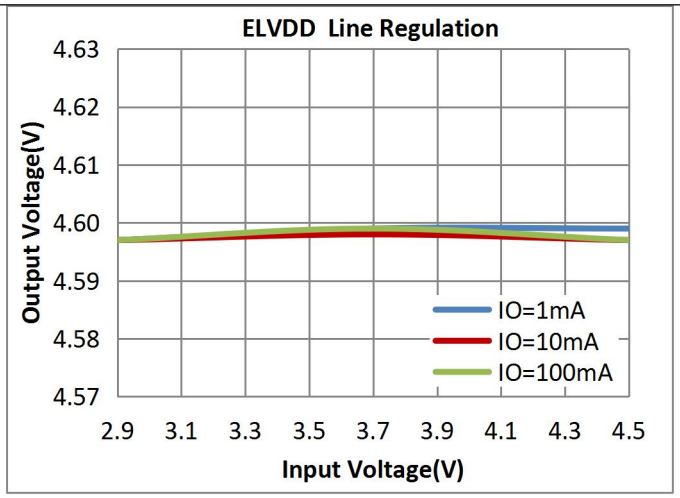
(VI = 3.7V, V(ELVDD)=4.6V, V(ELVSS)=-2.5V, V(AVDD)=6.1V, unless otherwise noted.)

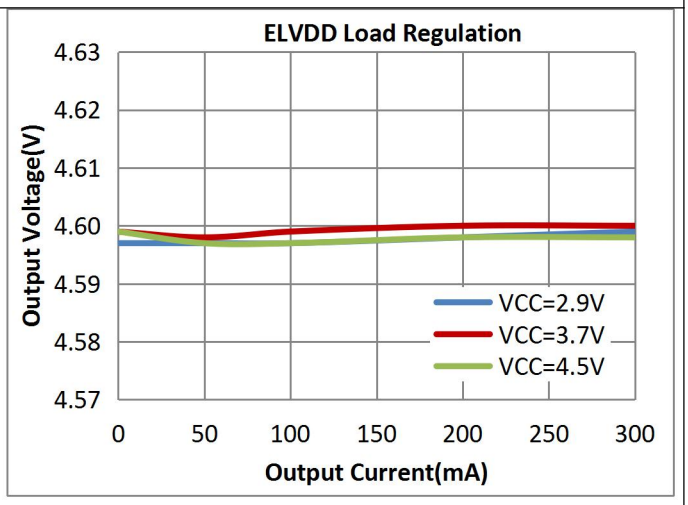






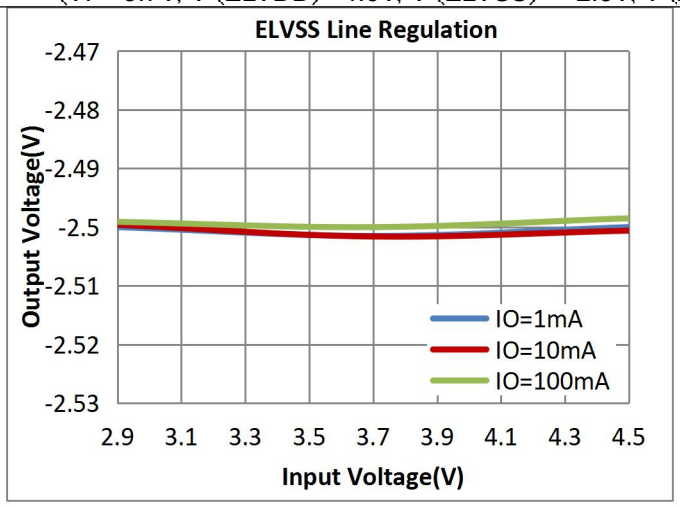


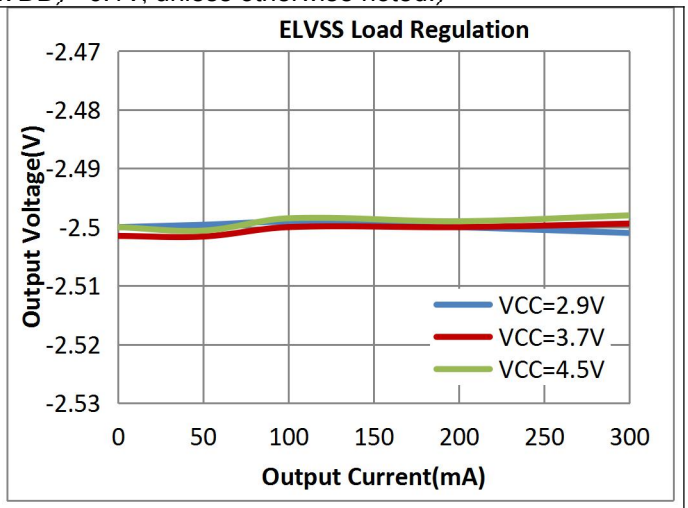


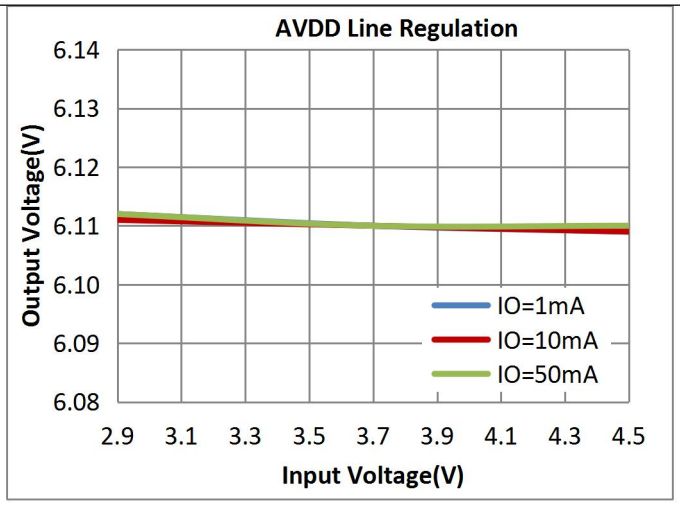


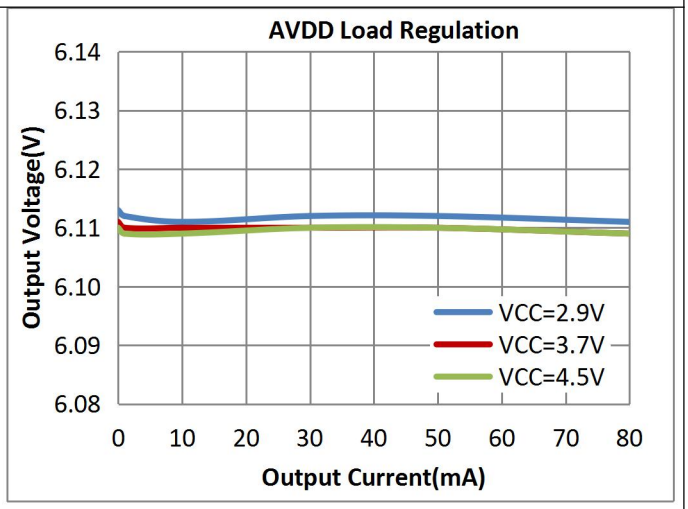
■ Typical Characteristic(continued)

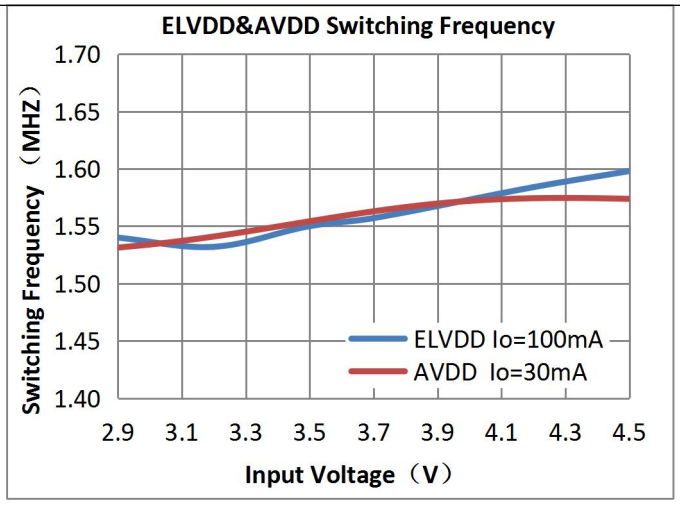
(VI = 3.7V, V (ELVDD) =4.6V, V (ELVSS) = -2.5V, V (AVDD) =6.1V, unless otherwise noted.)

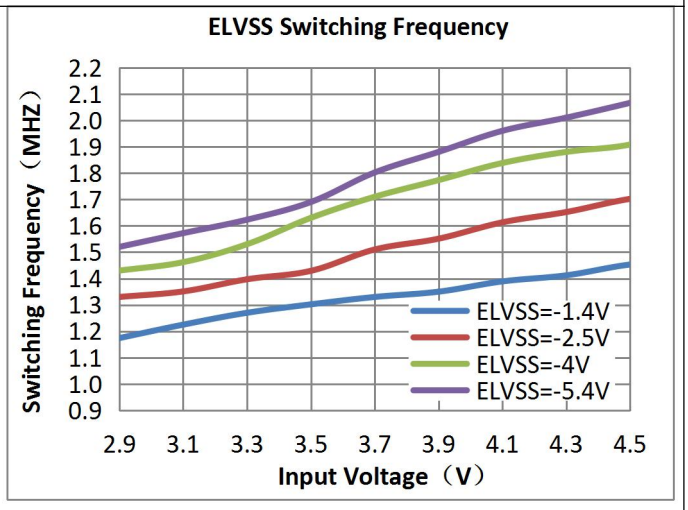












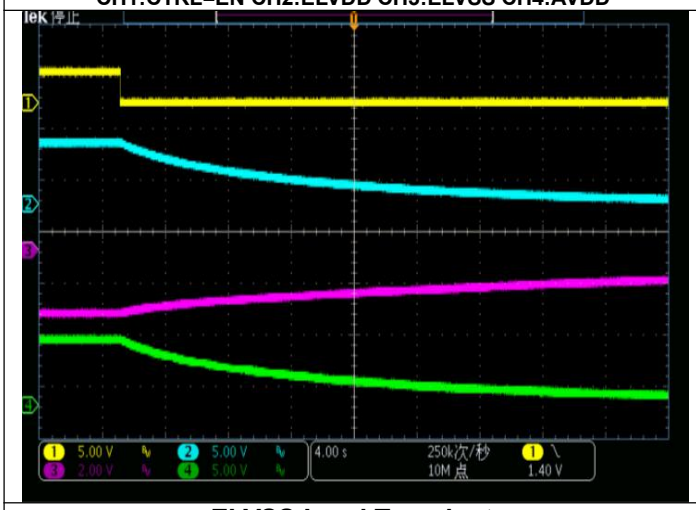
■ Typical Characteristic(continued)

(VI = 3.7V, V (ELVDD) =4.6V, V (ELVSS) = -2.5V, V (AVDD)=6.1V, unless otherwise noted.)

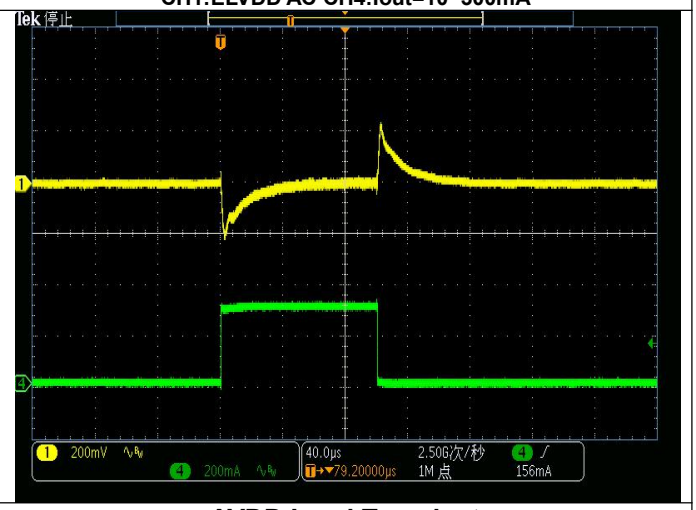
Start-up Waveform
CH1:ELVDD CH2:ELVSS CH3:AVDD CH4:Iin

Shut-down Waveform Discharge=on
CH1:CTRL=EN CH2:ELVDD CH3:ELVSS CH4:AVDD

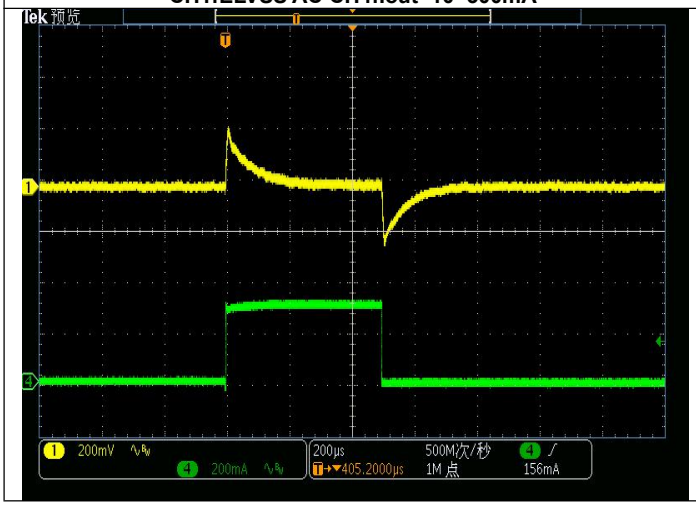
Shut-down Waveform Discharge=off
CH1:CTRL=EN CH2:ELVDD CH3:ELVSS CH4:AVDD



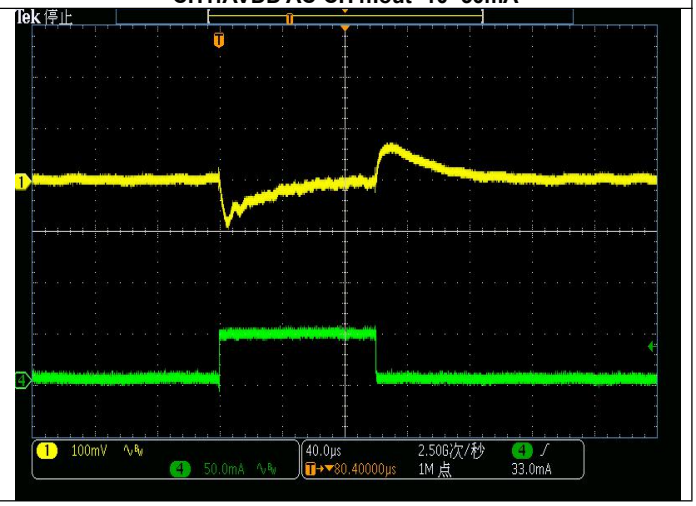
ELVDD Load Transient
CH1:ELVDD AC CH4:Iout=10~300mA



ELVSS Load Transient
CH1:ELVSS AC CH4:Iout=10~300mA



AVDD Load Transient
CH1:AVDD AC CH4:Iout=10~50mA



■ Functional Description

1 OVERVIEW

The OCP2133 consists of two boost converters and an inverting buck-boost converter. V (ELVDD) is programmable in the range of 4.6 V to 5 V (default = 4.6 V), V (ELVSS) is programmable in the range of –1.4 V to –5.4 V (default =–2.5 V) and V (AVDD) is programmable between 5.8 V and 7.9 V (default = 6.1 V). The transition time when (ELVSS) is programmed to a different voltage is adjustable by the CT-pin capacitor or by digital programming.

2 Under voltage Lockout

The device has a build in under voltage lockout function that disables the device when the input supply voltage is too low for normal operation

3 Thermal Shut-down

A thermal shutdown is implemented to prevent damage because of excessive heat and power dissipation. Once a temperature of typically 135°C is exceeded the device shuts down (the programming is not lost). When the temperature decreases to typ 130°C the device automatically restarts performing the start-up sequencing with the same voltages and programming as programmed before the thermal shutdown

4 ELVDD Boost Converter (OUT1)

The ELVDD boost converter uses a fixed-frequency valley-current-mode topology. The output voltage V(ELVDD) is adjustable between 4.6 V and 5 V with a default voltage of 4.6 V (see Table 1). In shut down its output is fully isolated (input to output and output to input).

For the highest output voltage accuracy, connect the output sense pin (SNS1) directly to the positive pin of the output capacitor. If not used, the SNS1 pin can be left floating or connected to ground, then the output voltage is sensed at the OUT1 pin.

5 ELVSS Inverting Buck-Boost Converter(OUT2)

The ELVSS inverting buck-boost converter uses a constant-off-time peak-current-mode topology. The output voltage V(ELVSS) is adjustable between –5.4 V and –1.4 V with a default voltage of –2.5 V (see Table 1). In shut down its output is fully isolated (input to output and output to input)

6 AVDD Boost Converter(OUT3)

The AVDD boost converter uses a fixed-frequency peak-current-mode topology. The output voltage V(AVDD) is adjustable between 5.8 V and 7.9 V with a default voltage of 6.1 V (see Table 1). In shut down its output is fully isolated (input to output and output to input).

7 Start-up Sequence, Soft-Start and Shut-down

The device has an implemented soft-start which limits the inrush current. When VI is applied, the Output Discharge is undefined until the rising edge of CTRL sets the Output Discharge to follow the FD-pin setting. When the converters are disabled all outputs are discharged if FD = high or high impedance if FD = low. If only the AVDD converter is disabled (EN3 = low, CTRL = high) a forward biased diode charges the AVDD output to VI until CTRL = low, then the AVDD output is disconnected from VI. The typical start-up sequence is shown in Figure 5.

- Pulling EN3 high starts the AVDD boost converter. V(AVDD) follows a linear 1.5 ms long voltage ramp until it reaches its default value of 6.1 V, the switch current is limited to typ. 0.35 A.
- Pulling CTRL high starts the ELVDD boost converter. V(ELVDD) starts with a reduced switch current limit of 0.1 A until it reaches its default voltage of 4.6 V then the full current limit is released.
- 10 ms after CTRL is pulled high the ELVSS inverting buck-boost converter starts. V(ELVSS) starts with a reduced switch current limit of 0.4 A until it reaches its default voltage of –2.5 V, then the full current limit is released.

All converters can start into an existing output voltage without generating a voltage drop at the output. When V (ELVSS) is < –0.7 V during startup, the 10 ms long discharge at V (ELVSS) is disabled to avoid a voltage drop.

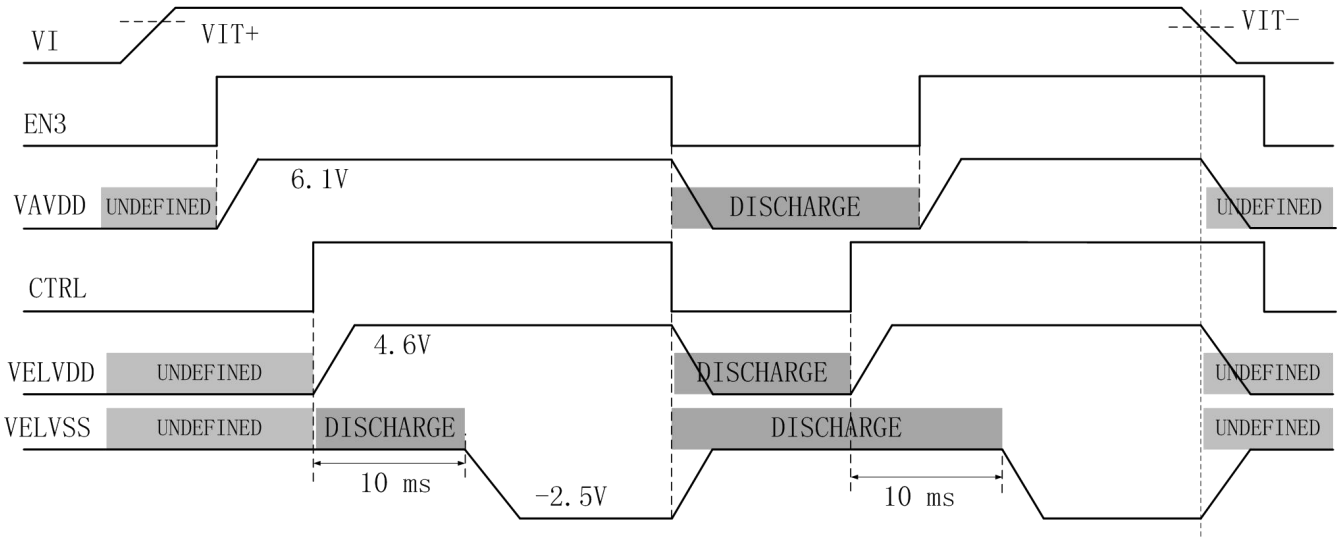


Figure 5. Start-up Sequencing Active Discharge Enabled

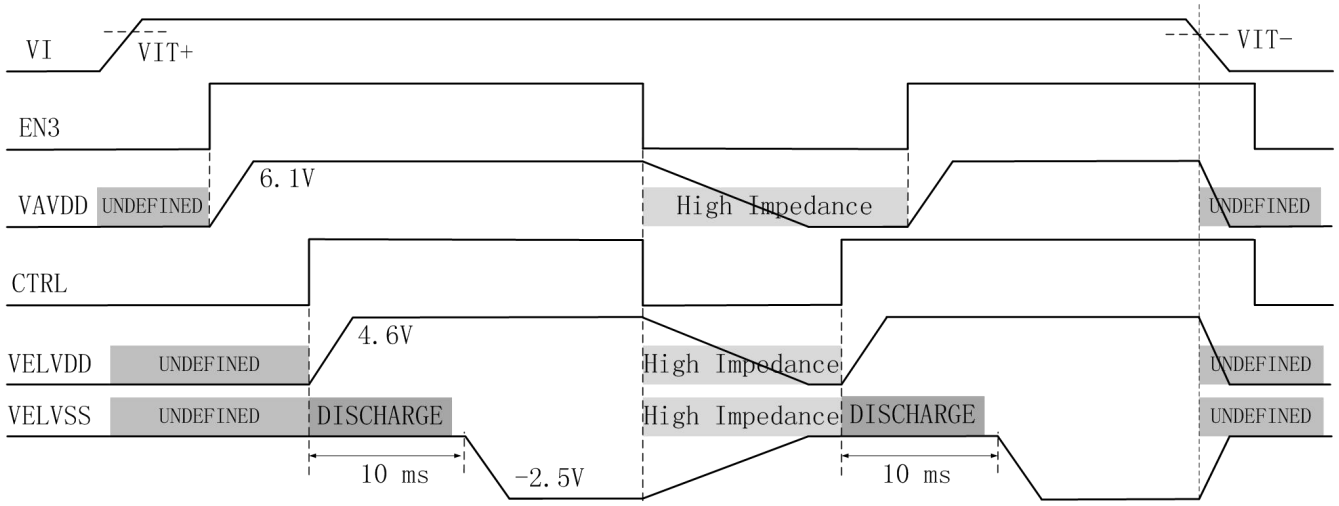
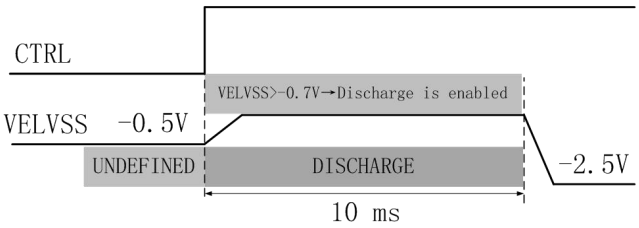


Figure 6. Start-up Sequencing Active Discharge Disabled



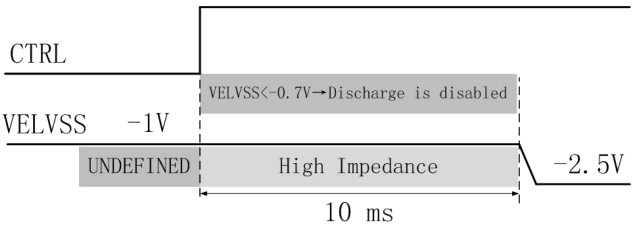


Figure 7. $V_{(ELVSS)}$ > –0.7 V →Discharge is enabled Figure8. $V_{(ELVSS)}$ <–0.7 V →Discharge is disabled

8 V (ELVSS) Transition Time Control (CT Pin)

The transition time is the time required to move V(ELVSS) from the actual voltage level to the new programmed voltage level. The transition time can be controlled by an external capacitor connected to the CT pin or by digital programming. The digital programming, 52 or 53 CTRL pulses, overwrites the CT pin setting until the function is reset. For the first V(ELVSS) voltage level change the transition time is as fast as possible, for all following V(ELVSS) changes the transition time is controlled by the capacitor connected to the CT pin or the programmed setting. The typical 50 mV CT pin comparator detects when the CT pin is connected to GND or floating, then the fastest possible transition time is used. When a capacitor is connected the R-C time constant τ sets the transition time. The output voltage is almost settled after 3τ, which means 95% of the target voltage is reached.

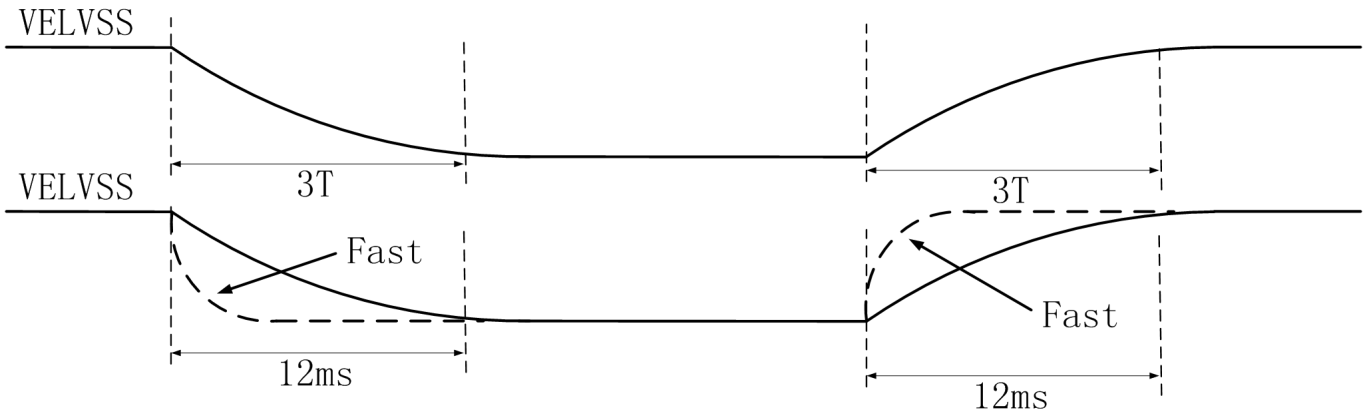


Figure 9. V (ELVSS) Transition Time Control

9 Digital Interface (CTRL Pin)

The digital interface allows programming of the positive output voltages V(AVDD), V(ELVDD) and the negative output voltage V(ELVSS) in discrete steps. By default, the V(ELVSS) transition time and the Output Discharge during shutdown are controlled by the CT and FD pin, the setting can be overwritten by programming. If programming is not required, the CTRL pin can also be used as a standard enable pin. Once the device is enabled the device starts with its default values (blue marked values in Table 1). The interface counts the rising edges applied to the CTRL pin and sets the new values as shown in Table 1. The settings are stored in a volatile memory, the reset behavior is described in the Device Reset section

Table 1. Programming Table

Rising Edges	$V_{(ELVSS)}$	Rising Edges	$V_{(ELVSS)}$	Rising Edges	$V_{(AVDD)}$	Rising Edges	Outputs Discharge	Rising Edges	$V_{(ELVSS)}$ transition time	Rising Edges	$V_{(ELVDD)}$
0 / no pulse	–2.5 V	21	–3.4 V	0 / no pulse	6.1 V	0 / no pulse	controlled by FD pin	0 / no pulse	controlled by CT pin	0 / no pulse	4.6 V
1	–5.4 V	22	–3.3 V	42	7.9 V	50	ON	52	fast	54	4.7 V
2	–5.3 V	23	–3.2 V	43	7.6 V	51	OFF	53	12 ms	55	4.8 V
3	–5.2 V	24	–3.1 V	44	7.3 V					56	4.9 V
4	–5.1 V	25	–3.0 V	45	7.0 V					57	5.0 V
5	–5.0 V	26	–2.9 V	46	6.7 V						
6	–4.9 V	27	–2.8 V	47	6.4 V						
7	–4.8 V	28	–2.7 V	48	6.1 V						
8	–4.7 V	29	–2.6 V	49	5.8 V						
9	–4.6 V	30	–2.5 V								
10	–4.5 V	31	–2.4 V								
11	–4.4 V	32	–2.3 V								
12	–4.3 V	33	–2.2 V								
13	–4.2 V	34	–2.1 V								
14	–4.1 V	35	–2.0 V								
15	–4.0 V	36	–1.9 V								

16	–3.9 V	37	–1.8 V								
17	–3.8 V	38	–1.7 V								
18	–3.7 V	39	–1.6 V								
19	–3.6 V	40	–1.5 V								
20	–3.5 V	41	–1.4 V								

10 Short Circuit and Overload Protection

The device is protected against short of V(AVDD), V(ELVDD) and V(ELVSS) to ground. V(ELVDD) andV(ELVSS) are also protected when they are shorted together. In addition to the switch current limit, which also limits the output current, V(AVDD) has a more accurate typ. 100 mA output current protection. A short at any converter and the V(AVDD) overload protection shuts down the whole device, the shut-down state is latched, input and outputs are fully disconnected. To reset the whole device VI has to cycle below under voltage lockout or EN3 and CTRL have to be low at the same time for minimum td(reset). The device detects a short or an overload when one of the below conditions is fulfilled:

- V(ELVDD) is not in regulation 10 ms after V(ELVDD) is enabled (CTRL = HIGH) → shut-down all
- V(ELVSS) is not in regulation 10 ms after V(ELVSS) is enabled (20 ms after CTRL = HIGH) → shut-down all
- V(AVDD) falls below 90% of its programmed voltage longer than 4 ms → shut-down all
- V(ELVDD) falls below 90% of its programmed voltage longer than 4 ms → shut-down all
- V(ELVSS) rises above 500 mV of its programmed voltage longer than 4 ms → shut-down all
- V(AVDD) output current is > 100 mA longer than 4 ms → shut-down all

11 Enable / Disable Active Discharge During Shutdown

The Active Discharge during shutdown can be enabled and disabled by the FD pin or by programming. The programming overwrites the FD pin setting until the function is reset.

FD pin connected to GND or 51 CTRL pulses

→ Active discharge is disabled and all outputs are high impedance.

FD pin connected to HIGH (VIH > 1.2 V) or 52 CTRL pulses

→ Active discharge is enabled and all outputs are discharged

12 Device Reset

A power cycle resets all settings to default values as well as the short-circuit and overload protection.

Enabling the V (ELVDD) converter (first rising edge of CTRL) resets the Output Discharge

→ Output Discharge is controlled by FD pin.

When CTRL is low for td (reset) then V(ELVDD), V(ELVSS) and V(ELVSS) transition time are reset to default values

→ 4.6 V, –2.5 V, V (ELVSS) transition time is controlled by CT pin.

EN3 and CTRL are low at the same time for td (reset)

→ V(AVDD) is reset to its default value of 6.1 V, short-circuit and overload protection is reset

■ Application Information and Implementation

1 Application Information

Figure 5 shows a typical application circuit suitable for supplying AMOLED displays in smart phone applications. The circuit is designed to operate from a single-cell Li-Ion battery and generates positive output voltages $V_{(AVDD)}$ of 6.1 V and $V_{(ELVDD)}$ of 4.6 V as well as a negative output voltage $V_{(ELVSS)}$ of –2.5 V. ELVDD and ELVSS are capable of supplying up to 500 mA of output current.

2 Typical Application

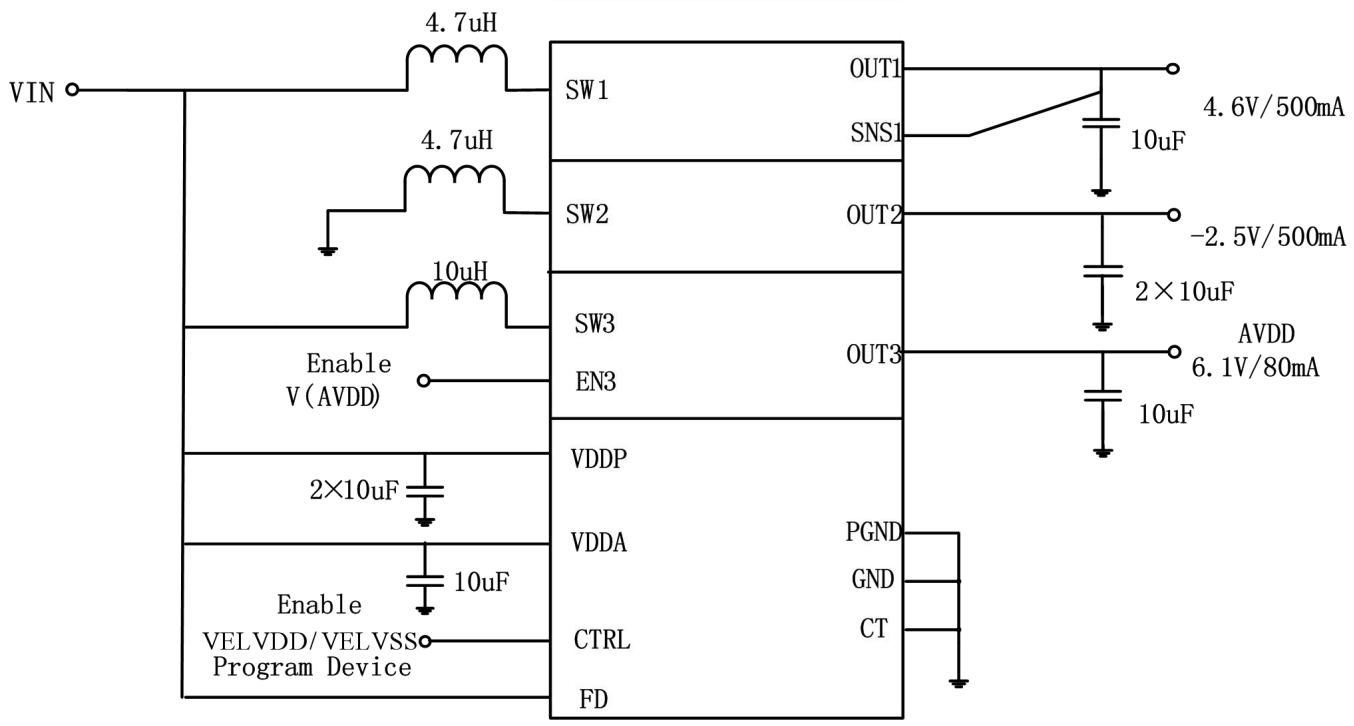


Figure 5, OCP2133 Typical Application

2.1 Design Requirements

For this design example, use the following input parameters in Table 2.

Table 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	2.9 V to 4.5 V
Output voltage	V(AVDD) = 6.1 V, V(ELVDD) = 4.6 V, V(ELVSS) = –2.5 V
Switching frequency	ELVDD, ELVSS and AVDD = 1.6 MHz

2.2 Detailed Design Procedure

In order to maximize performance, the device has been optimized for use with a relatively narrow range of component values. The $V_{(AVDD)}$ boost converter typically requires a 10μH inductor, $V_{(ELVDD)}$ and $V_{(ELVSS)}$ require a 4.7μH inductor. Ceramic capacitors are usually used for input and output capacitors. It is recommended to use the suggested values in all applications. Customers using other values are strongly recommended to characterize circuit performance on a case-by-case basis.

2.2.1 ELVDD Boost Converter (OUT1)

1) Inductor Selection

The main parameter for the inductor selection is the inductor saturation current, which must be higher than the peak switch current. Inductors with lower saturation current than the minimum switch current limit can be used when the maximum output current is not required, however a minimum saturation current of 0.5 A is required to

ensure proper startup. The minimum required saturation current is calculated by the peak inductor current formula.

The inductors DC resistance as well as its core losses affects the efficiency. Lower DC resistance results in higher high load efficiency. The core losses are especially important for light load efficiency. The core material as well as the inductors physical size has an influence on the core losses. The higher the quality factor Q of the inductor at the switching frequency (1.6 MHz) the lower the core losses. Table 3 shows examples of suitable inductors, equivalent parts can be used.

- Minimum 3.3µH, maximum 6.1µHinductance.
- Minimum 0.5A saturation current, for full output current capability 1.3A.
- Minimum V_I and maximum I_O must be taken to calculate the required saturation current.
- Duty Cycle: $D = \frac{V_O - V_I \times \eta}{V_O}$

  Where
  - VI is the boost converter input supply voltage.
  - V_O is the boost converter output voltage.
  - η is the boost converter efficiency (taken from the Application Curves or 80% as an assumption).

- Peak Inductor Current: $I_{(SW)M} = \frac{I_O}{1-D} + \frac{V_I \times D}{2 \times f \times L}$

  where
  - I_O is the boost converter output current.
  - f = 1.6 MHz (the boost converter switching frequency).
  - L is the boost converter inductance (4.7µH).

Table 3. ELVDD Boost Converter (OUT1) Inductor Selection

INDUCTANCE	I_{SAT}	DCR	MANUFACTURER	PART NUMBER	DIMENSIONS
4.7 µH	1.4A	250mΩ	TDK	VLS252010HBX-4R7M-1	2.5 mm × 2.0 mm × 1 mm

2) Capacitor Selection

The main parameter for the capacitor selection is the capacitance at the operating voltage. The more voltage is applied at the capacitor the lower is its resulting capacitance (DC-bias effect), also temperature and AC-Voltage changes the capacitance, however the DC-bias effect is dominant. For best voltage filtering (lowest voltage ripple), low ESR capacitors are recommended. Ceramic capacitors have a low ESR value, but also other types can be used. Table 4 and Table 5 show examples of suitable capacitors, equivalent parts can be used.

Table 4. Input Capacitor Selection ELVDD Boost Converter (OUT1)

CAPACITANCE	VOLTAGE RATING	MANUFACTURER	PART NUMBER	SIZE
10µF	6.3v	muRata	GRM188R60J106ME84	0603

Table 5. Output Capacitor Selection ELVDD Boost Converter (OUT1)

CAPACITANCE	VOLTAGE RATING	MANUFACTURER	PART NUMBER	SIZE
10µF	10V	muRata	GRM188Z71A106MA73D	0603

2.2.2 ELVSS Inverting Buck-Boost Converter (OUT2)

1) Inductor Selection

The main parameter for the inductor selection is the inductor saturation current, which must be higher than the peak switch current. Inductors with lower saturation current than the minimum switch current limit can be used when the maximum output current is not required, however a minimum saturation current of 0.5 A is required to ensure proper startup. The minimum required saturation current is calculated by the peak inductor current

formula.

The inductors DC resistance as well as its core losses affects the efficiency. Lower DC resistance results in higher high load efficiency. The core losses are especially important for light load efficiency. The core material as well as the inductors physical size has an influence on the core losses. The higher the quality factor Q of the inductor at the switching frequency (1.6 MHz) the lower the core losses. Table 6 shows examples of suitable inductors, equivalent parts can be used.

- Minimum 3.3µH, maximum 6.1µHinductance.
- Minimum 0.5A saturation current, for full output current capability 1.5A.
- Minimum V_I and maximum I_O must be taken to calculate the required saturation current.
- Duty Cycle: $D = \frac{V_O}{V_O - V_I \times \eta}$

  where
  - V_I is the inverting buck-boost converter input supply voltage.
  - V_O is the inverting buck-boost converter output voltage.
  - η is the inverting buck-boost converter efficiency (taken from the Application Curves or 80% as an assump
- Peak Inductor Current: $I_{(SW)M} = \frac{I_O}{1-D} + \frac{V_I \times D}{2 \times f \times L}$

  where
  - I_O is the inverting buck-boost converter output current.
  - f = 1.6 MHz (the inverting buck-boost converter switching frequency).
  - L is the inverting buck-boost converter inductance (4.7µH).

Table 6. ELVSS Inverting Buck-Boost Converter (OUT2) Inductor Selection

INDUCTANCE	I_{SAT}	DCR	MANUFACTURER	PART NUMBER	DIMENSIONS
4.7 µH	1.4A	250mΩ	TDK	VLS252010HBX-4R7M-1	2.5 mm × 2.0 mm × 1 mm

2) Capacitor Selection

The main parameter for the capacitor selection is the capacitance at the operating voltage. The more voltage is applied at the capacitor the lower is its resulting capacitance (DC-bias effect), also temperature and AC-Voltage changes the capacitance, and however the DC-bias effect is dominant. For best voltage filtering (lowest voltage ripple), low ESR capacitors are recommended. Ceramic capacitors have a low ESR value, but also other types can be used. Table 7 and Table 8 show examples of suitable capacitors, equivalent parts can be used.

Table 7. Input Capacitor Selection ELVSS Inverting Buck-Boost Converter (OUT2)

CAPACITANCE	VOLTAGE RATING	MANUFACTURER	PART NUMBER	SIZE
10µF	6.3V	muRata	GRM188R60J106ME84	0603

Table 8. Output Capacitor Selection ELVSS Inverting Buck-Boost Converter (OUT2)

CAPACITANCE	VOLTAGE RATING	MANUFACTURER	PART NUMBER	SIZE
10µF	10V	muRata	GRM188Z71A106MA73D	0603

2.2.3 AVDD Boost Converter (OUT3)

1) Inductor Selection

The main parameter for the inductor selection is the inductor saturation current, which must be higher than the peak switch current. Inductors with lower saturation current than the minimum switch current limit can be used when the maximum output current is not required, however a minimum saturation current of 0.2 A is required to ensure proper startup. The minimum required saturation current is calculated by the peak inductor current formula.

The inductors DC resistance as well as its core losses affects the efficiency. Lower DC resistance results in higher high load efficiency. The core losses are especially important for light load efficiency. The core material as well as the inductors physical size has an influence on the core losses. The higher the quality factor Q of the inductor at the switching frequency (1.6 MHz) the lower the core losses. Table 9 shows examples of suitable inductors, equivalent parts can be used.

- Minimum 7μH, maximum 13-μH inductance.
- Minimum 0.2A saturation current, for full output current capability 0.25A.
- Minimum V_I and maximum I_O must be taken to calculate the required saturation current.
- Duty Cycle: $D = \frac{V_O - V_I \times \eta}{V_O}$

where

– V_I is the boost converter input supply voltage.
– V_O is the boost converter output voltage.
– η is the boost converter efficiency (taken from the Application Curves or 80% as an assumption).

- Peak Inductor Current: Where $I_{(SW)M} = \frac{I_O}{1-D} + \frac{V_I \times D}{2 \times f \times L}$

where

– I_O is the boost converter output current.
– f = 1.6 MHz (the boost converter switching frequency).
– L is the boost converter inductance (10μH).

Table 9. AVDD Boost Converter (OUT3) Inductor Selection

INDUCTANCE	I_{SAT}	DCR	MANUFACTURER	PART NUMBER	DIMENSIONS
10 μH	0.95A	552mΩ	TDK	VLS252010HBX-100M-1	2.5 mm × 2.0 mm × 1 mm

2) Capacitor Selection

The main parameter for the capacitor selection is the capacitance at the operating voltage. The more voltage is applied at the capacitor the lower is its resulting capacitance (DC-bias effect), also temperature and AC-Voltage changes the capacitance, however the DC-bias effect is dominant. For best voltage filtering (lowest voltage ripple), low ESR capacitors are recommended. Ceramic capacitors have a low ESR value, but also other types can be used. Table 10 and Table 11 show examples of suitable capacitors, equivalent parts can be used.

Table 10. Input Capacitor Selection AVDD Boost Converter (OUT3)

CAPACITANCE	VOLTAGE RATING	MANUFACTURER	PART NUMBER	SIZE
10μF	6.3v	muRata	GRM188R60J106ME84	0603

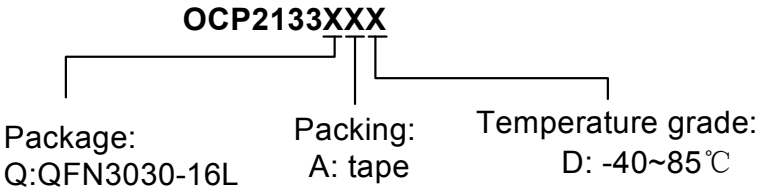
Table 11. Output Capacitor Selection AVDD Boost Converter (OUT3)

CAPACITANCE	VOLTAGE RATING	MANUFACTURER	PART NUMBER	SIZE
10μF	10V	muRata	GRM188Z71A106MA73D	0603

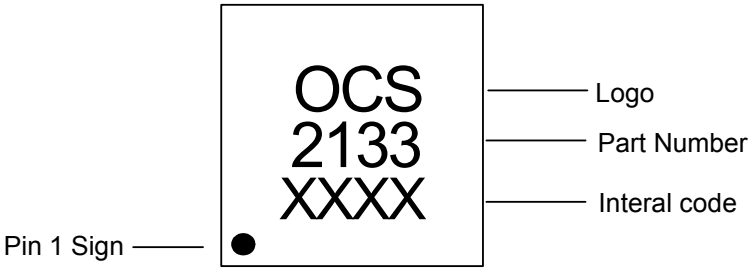
■ Power Supply Recommendations

The OCP2133 device is designed to operate with input supplies from 2.9 V to 4.5 V. The input supply should be stable and free of noise if the device's full performance is to be achieved. If the input supply is located more than a few centimeters away from the device, additional bulk capacitance may be required. The input capacitance shown in the application schematics is sufficient for typical applications.

■ Ordering Information

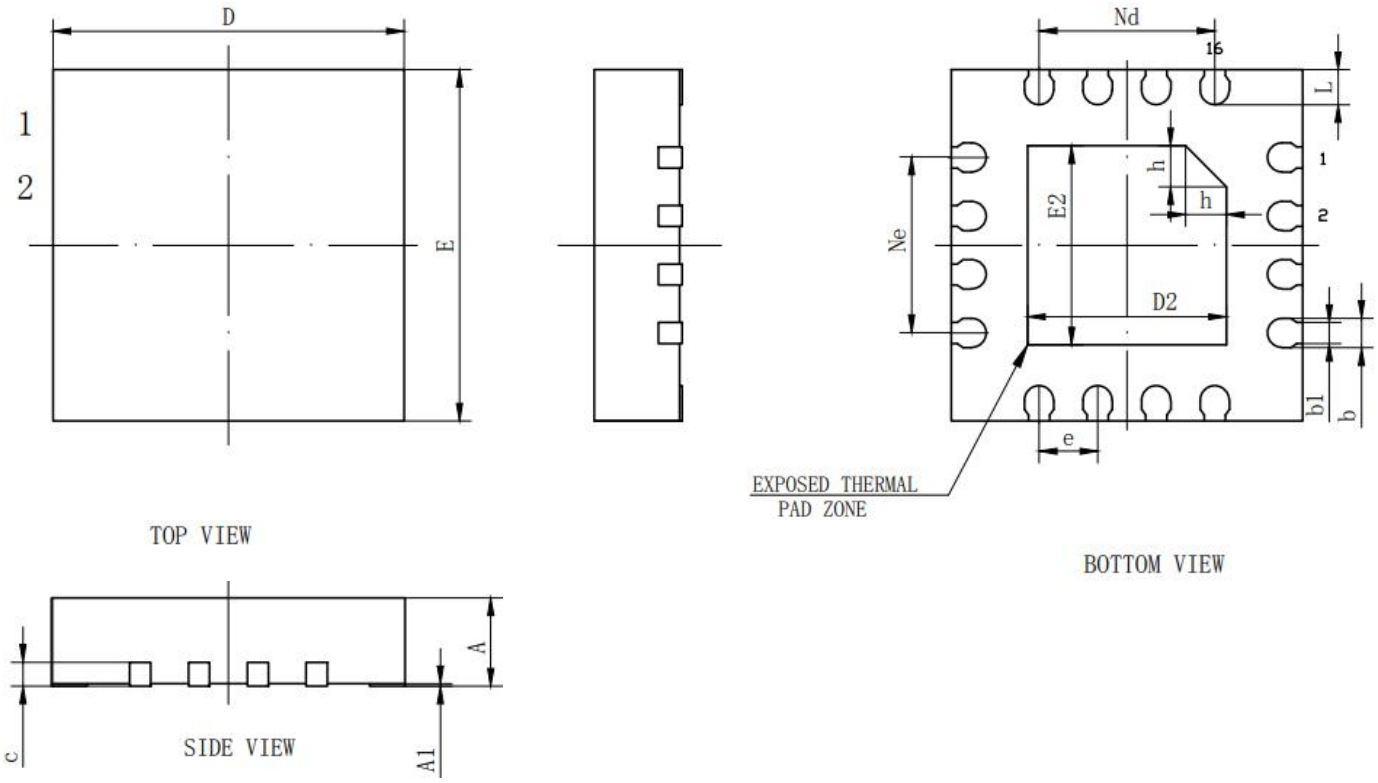


■ Marking Information

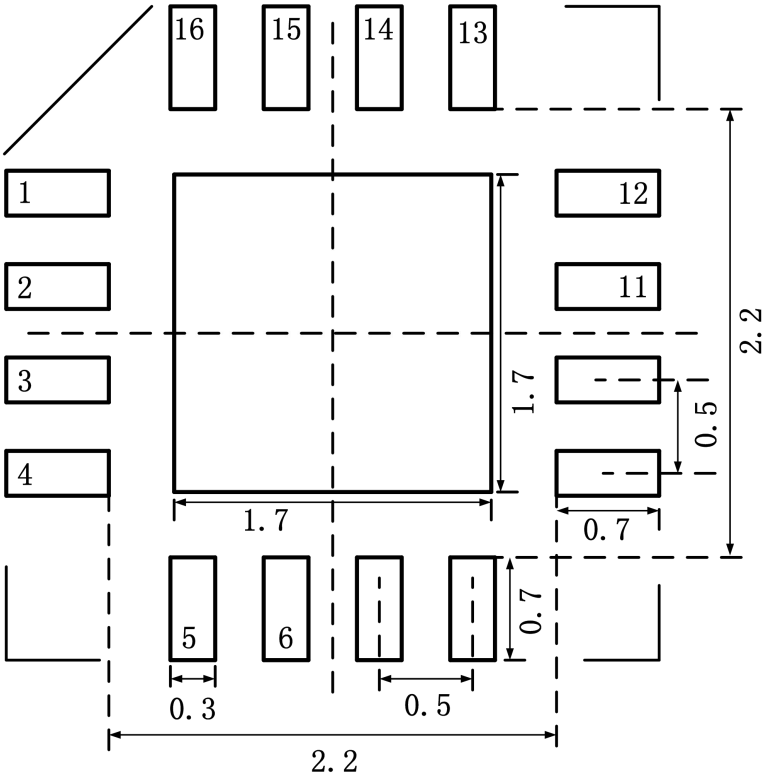


■ Package Information

QFN3030-16L

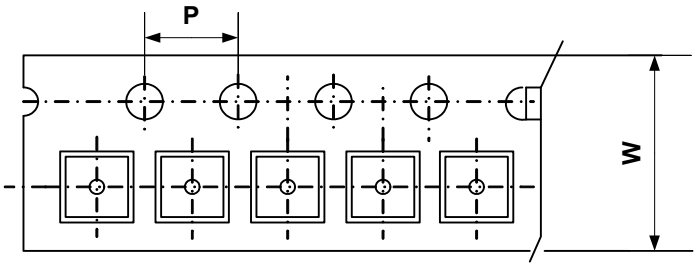


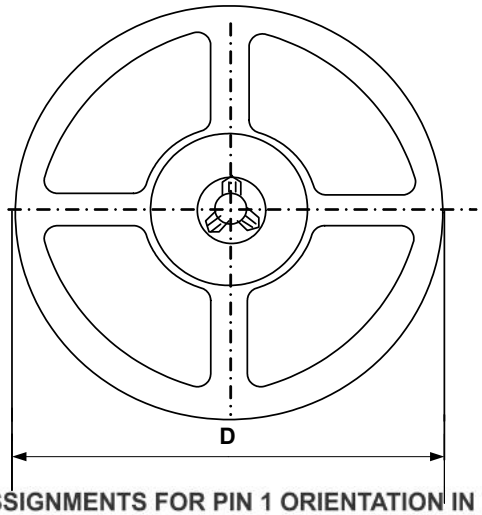
Symbol	Dimensions In Millimeters			Dimensions In Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	0.70	0.75	0.80	0.275	0.029	0.031
A1	0.00	0.02	0.05	0.00	0.00	0.001
c	0.203 (Ref.)			0.008(Ref.)		
b	0.18	0.25	0.30	0.007	0.010	0.012
b1	0.18 (Ref.)			0.007 (Ref.)		
L	0.25	0.3	0.35	0.010	0.012	0.013
h	0.30	0.35	0.40	0.012	0.013	0.015
D	2.90	3.00	3.10	0.114	0.118	0.122
E	2.90	3.00	3.10	0.114	0.118	0.122
D2	1.60	1.70	1.80	0.063	0.067	0.071
E2	1.60	1.70	1.80	0.063	0.067	0.071
e	0.5BCS			0.020 BCS		
Ne	1.5BCS			0.059 BCS		
Nd	1.5BCS			0.059 BCS		



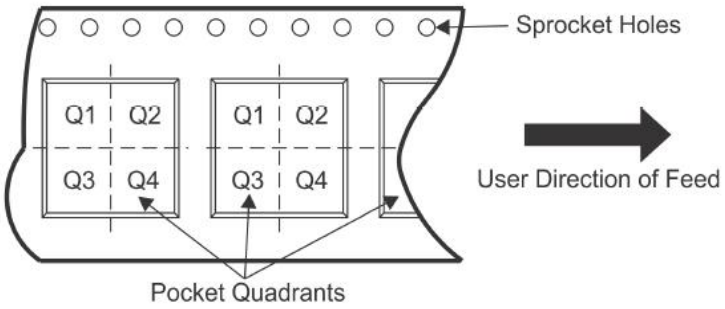
RECOMMENDED LAND PATTERN (unit: mm)

■ Package Information





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Package Type	MSL	Carrier Width(W)	Pitch(P)	Reel Size(D)	Packing Minimum	PIN A1 Quadrant
QFN3030-16L	Level-3	12.0±0.1 mm	4.0±0.1 mm	330±1 mm	3000pcs	Q1

Note: Carrier Tape Dimension, Reel Size and Packing Minimum

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