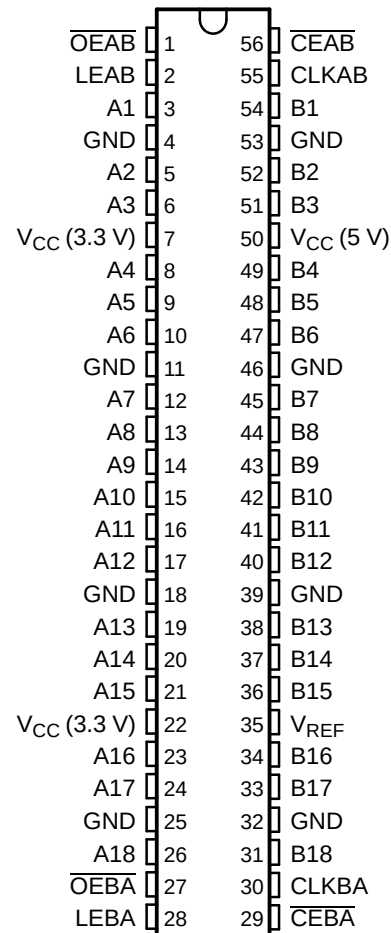


FEATURES

- Members of Texas Instruments Widebus™ Family
- UBT™ Transceivers Combine D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, Clocked, or Clock-Enabled Modes
- OEC™ Circuitry Improves Signal Integrity and Reduces Electromagnetic Interference
- Translate Between GTL/GTL+ Signal Levels and LVTTTL Logic Levels
- Support Mixed-Mode (3.3 V and 5 V) Signal Operation on A-Port and Control Inputs
- Identical to '16601 Function
- I_{off} Supports Partial-Power-Down Mode Operation
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors on A Port
- Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise
- Latch-Up Performance Exceeds 500 mA Per JESD 17

SN54GTL16612... WD PACKAGE
SN74GTL16612... DGG OR DL PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

The 'GTL16612 devices are 18-bit UBT™ transceivers that provide LVTTTL-to-GTL/GTL+ and GTL/GTL+-to-LVTTTL signal-level translation. They combine D-type flip-flops and D-type latches to allow for transparent, latched, clocked, and clock-enabled modes of data transfer identical to the '16601 function. The devices provide an interface between cards operating at LVTTTL logic levels and a backplane operating at GTL/GTL+ signal levels. Higher-speed operation is a direct result of the reduced output swing (<1 V), reduced input threshold levels, and OEC™ circuitry.

The user has the flexibility of using these devices at either GTL ($V_{TT} = 1.5$ V and $V_{REF} = 0.8$ V) or the preferred higher noise margin GTL+ ($V_{TT} = 1.5$ V and $V_{REF} = 1$ V) signal levels. GTL+ is the Texas Instruments derivative of the Gunning Transceiver Logic (GTL) JEDEC standard JESD 8-3. The B port normally operates at GTL or GTL+ signal levels, while the A-port and control inputs are compatible with LVTTTL logic levels and are 5-V tolerant. V_{REF} is the reference input voltage for the B port.

V_{CC} (5 V) supplies the internal and GTL circuitry while V_{CC} (3.3 V) supplies the LVTTTL output buffers.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus, UBT, OEC are trademarks of Texas Instruments.

SN54GTL16612, SN74GTL16612

18-BIT LVTTTL-TO-GTL/GTL+ UNIVERSAL BUS TRANSCEIVERS

SCBS480K–JUNE 1994–REVISED JULY 2005



DESCRIPTION/ORDERING INFORMATION (CONTINUED)

Data flow in each direction is controlled by output-enable ($\overline{OEAB}$ and $\overline{OEBA}$), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. The clock can be controlled by the clock-enable ($\overline{CEAB}$ and $\overline{CEBA}$) inputs. For A-to-B data flow, the devices operate in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if $\overline{CEAB}$ is low and CLKAB is held at a high or low logic level. If LEAB is low, the A data is stored in the latch/flip-flop on the low-to-high transition of CLKAB if $\overline{CEAB}$ also is low. When $\overline{OEAB}$ is low, the outputs are active. When $\overline{OEAB}$ is high, the outputs are in the high-impedance state. Data flow for B to A is similar to that for A to B, but uses $\overline{OEBA}$, LEBA, CLKBA, and $\overline{CEBA}$.

These devices are fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

Active bus-hold circuitry holds unused or undriven LVTTTL inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

ORDERING INFORMATION

T_A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SSOP – DL	Tube	SN74GTL16612DL	GTL16612
		Tape and reel	SN74GTL16612DLR	
	TSSOP – DGG	Tape and reel	SN74GTL16612DGGR	GTL16612
–55°C to 125°C	CFP – WD	Tube	SNJ54GTL16612WD	SNJ54GTL16612WD

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE⁽¹⁾

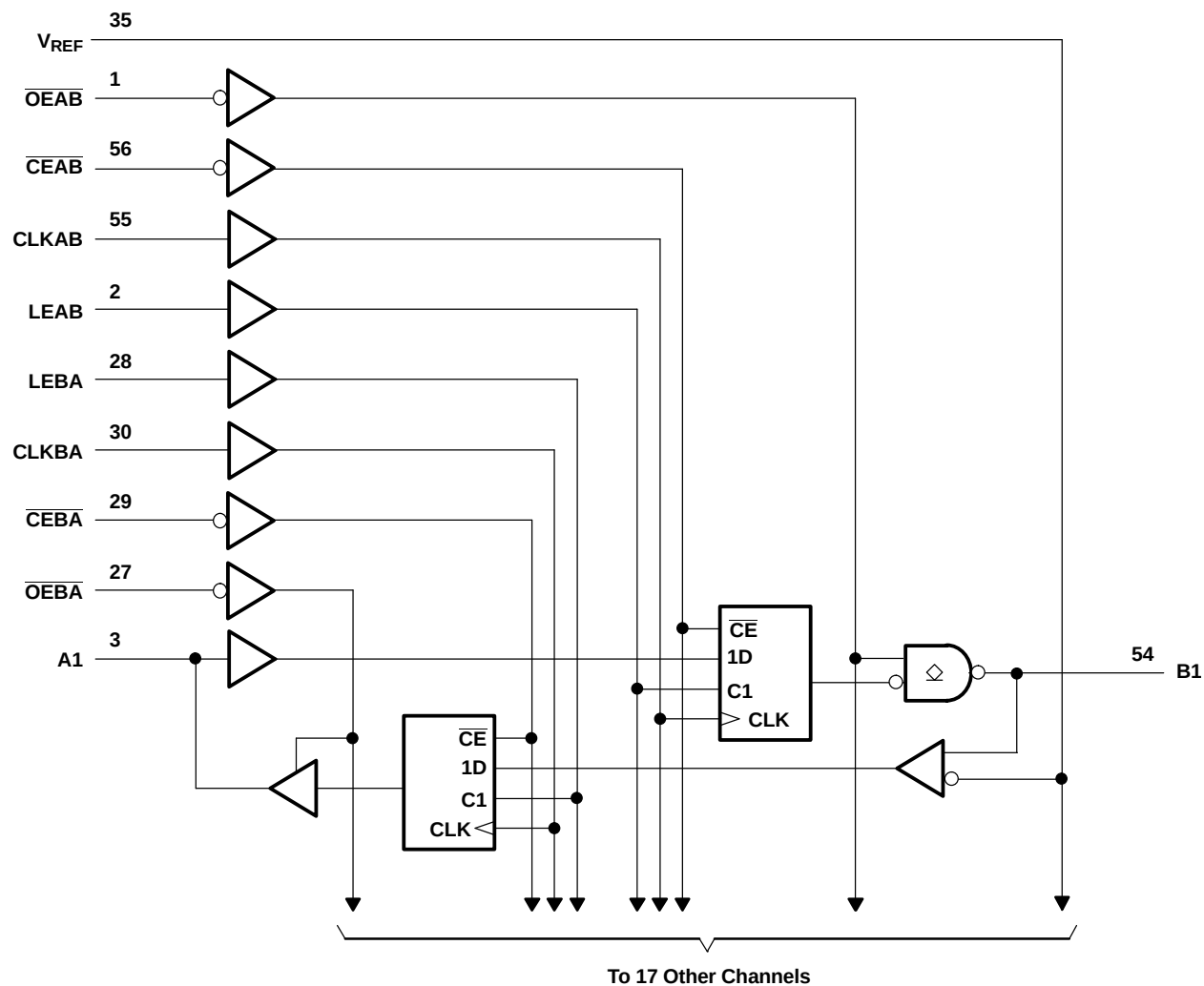
INPUTS					OUTPUT B	MODE
$\overline{CEAB}$	$\overline{OEAB}$	LEAB	CLKAB	A		
X	H	X	X	X	Z	Isolation
L	L	L	H	X	$B_0^{(2)}$	Latched storage of A data
L	L	L	L	X	$B_0^{(3)}$	
X	L	H	X	L	L	Transparent
X	L	H	X	H	H	
L	L	L	↑	L	L	Clocked storage of A data
L	L	L	↑	H	H	
H	L	L	X	X	$B_0^{(3)}$	Clock inhibit

(1) A-to-B data flow is shown. B-to-A data flow is similar, but uses $\overline{OEBA}$, LEBA, CLKBA, and $\overline{CEBA}$.

(2) Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAB went low

(3) Output level before the indicated steady-state input conditions were established

LOGIC DIAGRAM (POSITIVE LOGIC)



SN54GTL16612, SN74GTL16612

18-BIT LVTTTL-TO-GTL/GTL+ UNIVERSAL BUS TRANSCEIVERS

SCBS480K–JUNE 1994–REVISED JULY 2005

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range	3.3 V	–0.5	4.6	V
		5 V	–0.5	7	
V_I	Input voltage range ⁽²⁾	A-port and control inputs	–0.5	7	V
		B port and V_{REF}	–0.5	4.6	
V_O	Voltage range applied to any output in the high or power-off state ⁽²⁾	A port	–0.5	7	V
		B port	–0.5	4.6	
I_O	Current into any output in the low state	A port		128	mA
		B port		80	
I_O	Current into any A-port output in the high state ⁽³⁾			64	mA
	Continuous current through each V_{CC} or GND			±100	mA
I_{IK}	Input clamp current	$V_I < 0$		–50	mA
I_{OK}	Output clamp current	$V_O < 0$		–50	mA
θ_{JA}	Package thermal impedance ⁽⁴⁾	DGG package		64	°C/W
		DL package		56	
T_{stg}	Storage temperature range		–65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (3) This current flows only when the output is in the high state and $V_O > V_{CC}$.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions⁽¹⁾⁽²⁾⁽³⁾⁽⁴⁾

			SN54GTL16612			SN74GTL16612			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	3.3 V	3.15	3.3	3.45	3.15	3.3	3.45	V
		5 V	4.75	5	5.25	4.75	5	5.25	
V _{TT}	Termination voltage	GTL	1.14	1.2	1.26	1.14	1.2	1.26	V
		GTL+	1.35	1.5	1.65	1.35	1.5	1.65	
V _{REF}	Reference voltage	GTL	0.74	0.8	0.87	0.74	0.8	0.87	V
		GTL+	0.87	1	1.1	0.87	1	1.1	
V _I	Input voltage	B port	V _{TT}			V _{TT}			V
		Except B port	5.5			5.5			
V _{IH}	High-level input voltage	B port	V _{REF} + 50 mV			V _{REF} + 50 mV			V
		Except B port	2			2			
V _{IL}	Low-level input voltage	B port	V _{REF} – 50 mV			V _{REF} – 50 mV			V
		Except B port	0.8			0.8			
I _{IK}	Input clamp current		–18			–18			mA
I _{OH}	High-level output current	A port	–32			–32			mA
I _{OL}	Low-level output current	A port	64			64			mA
		B port	40			40			
T _A	Operating free-air temperature		–55		125	–40		85	°C

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
- (2) Normal connection sequence is GND first, $V_{CC} = 5$ V second, and $V_{CC} = 3.3$ V, I/O, control inputs, V_{TT} and V_{REF} (any order) last.
- (3) V_{TT} and R_{TT} can be adjusted to accommodate backplane impedances if the dc recommended I_{OL} ratings are not exceeded.
- (4) V_{REF} can be adjusted to optimize noise margins, but normally is two-thirds V_{TT} .

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54GTL16612			SN74GTL16612			UNIT		
				MIN	TYP ⁽¹⁾	MAX	MIN	TYP ⁽¹⁾	MAX			
V _{IK}		V _{CC} (3.3 V) = 3.15 V, V _{CC} (5 V) = 4.75 V	I _I = −18 mA			−1.2			−1.2	V		
V _{OH}	A port	V _{CC} (3.3 V) = 3.15 V to 3.45 V, V _{CC} (5 V) = 4.75 V to 5.25 V	I _{OH} = −100 μA			V _{CC} (3.3 V) − 0.2			V _{CC} (3.3 V) − 0.2	V		
		V _{CC} (3.3 V) = 3.15 V, V _{CC} (5 V) = 4.75 V	I _{OH} = −8 mA			2.4			2.4			
			I _{OH} = −32 mA			2			2			
V _{OL}	A port	V _{CC} (3.3 V) = 3.15 V, V _{CC} (5 V) = 4.75 V	I _{OL} = 100 μA						0.2	V		
			I _{OL} = 16 mA						0.4			
			I _{OL} = 32 mA						0.5			
			I _{OL} = 64 mA						0.6			
	B port	V _{CC} (3.3 V) = 3.15 V, V _{CC} (5 V) = 4.75 V, I _{OL} = 40 mA						0.5			0.4	
I _I	Control inputs	V _{CC} (3.3 V) = 0 or 3.45 V, V _{CC} (5 V) = 0 or 5.25 V	V _I = 5.5 V						10	μA		
	A port	V _{CC} (3.3 V) = 3.45 V, V _{CC} (5 V) = 5.25 V	V _I = 5.5 V					1000			20	
			V _I = V _{CC} (3.3 V)						1			1
			V _I = 0						−30			−30
	B port	V _{CC} (3.3 V) = 3.45 V, V _{CC} (5 V) = 5.25 V	V _I = V _{CC} (3.3 V)					5			5	
			V _I = 0						−5			−5
I _{off}		V _{CC} = 0,	V _I or V _O = 0 to 4.5 V					1000		100	μA	
I _{I(hold)}	A port	V _{CC} (3.3 V) = 3.15 V, V _{CC} (5 V) = 4.75 V	V _I = 0.8 V			75			75	μA		
			V _I = 2 V			−75			−75			
			V _I = 0 to V _{CC} (3.3 V) ⁽²⁾					±500			±500	
I _{OZH}	A port	V _{CC} (3.3 V) = 3.45 V, V _{CC} (5 V) = 5.25 V, V _O = 3 V				1			1	μA		
	B port	V _{CC} (3.3 V) = 3.45 V, V _{CC} (5 V) = 5.25 V, V _O = 1.2 V				10			10			
I _{OZL}	A port	V _{CC} (3.3 V) = 3.45 V, V _{CC} (5 V) = 5.25 V, V _O = 0.5 V				−1			−1	μA		
	B port	V _{CC} (3.3 V) = 3.45 V, V _{CC} (5 V) = 5.25 V, V _O = 0.4 V				−10			−10			
I _{CC} (3.3 V)	A or B port	V _{CC} (3.3 V) = 3.45 V, V _{CC} (5 V) = 5.25 V, I _O = 0, V _I = V _{CC} (3.3 V) or GND	Outputs high			1			1	mA		
			Outputs low			5			5			
			Outputs disabled			1			1			
I _{CC} (5 V)	A or B port	V _{CC} (3.3 V) = 3.45 V, V _{CC} (5 V) = 5.25 V, I _O = 0, V _I = V _{CC} (3.3 V) or GND	Outputs high			120			120	mA		
			Outputs low			120			120			
			Outputs disabled			120			120			
ΔI _{CC} ⁽³⁾		V _{CC} (3.3 V) = 3.45 V, V _{CC} (5 V) = 5.25 V, A-port or control inputs at V _{CC} (3.3 V) or GND, One input at 2.7 V				1			1	mA		
C _i	Control inputs	V _I = 3.15 V or 0				3.5			3.5	pF		
C _{io}	A port	V _O = 3.15 V or 0				12			12	pF		
	B port					10			5			

(1) All typical values are at V_{CC} (3.3 V) = 3.3 V, V_{CC} (5 V) = 5 V, $T_A = 25^\circ\text{C}$.

(2) This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

(3) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

SN54GTL16612, SN74GTL16612

18-BIT LVTTL-TO-GTL/GTL+ UNIVERSAL BUS TRANSCEIVERS

SCBS480K–JUNE 1994–REVISED JULY 2005



Timing Requirements

over recommended ranges of supply voltage and operating free-air temperature,
 $V_{TT} = 1.2\text{ V}$ and $V_{REF} = 0.8\text{ V}$ for GTL (unless otherwise noted) (see [Figure 1](#))

			SN54GTL16612		SN74GTL16612		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency			95		95	MHz
t_w	Pulse duration	LEAB or LEBA high	3.3		3.3		ns
		CLKAB or CLKBA high or low	5.6		5.6		
t_{su}	Setup time	A before CLKAB $\uparrow$	1.3		1.3		ns
		B before CLKBA $\uparrow$	3.4		2.5		
		A before LEAB $\downarrow$	1.2		0		
		B before LEBA $\downarrow$	1		1		
		$\overline{\text{CEAB}}$ before CLKAB $\uparrow$	2.1		2		
		$\overline{\text{CEBA}}$ before CLKBA $\uparrow$	2.6		2.2		
t_h	Hold time	A after CLKAB $\uparrow$	2.9		1.6		ns
		B after CLKBA $\uparrow$	4.1		0.3		
		A after LEAB $\downarrow$	4.5		4		
		B after LEBA $\downarrow$	4.3		3.6		
		$\overline{\text{CEAB}}$ after CLKAB $\uparrow$	2		0.8		
		$\overline{\text{CEBA}}$ after CLKBA $\uparrow$	1.1		1.1		

Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature,
 $V_{TT} = 1.2\text{ V}$ and $V_{REF} = 0.8\text{ V}$ for GTL (see [Figure 1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54GTL16612			SN74GTL16612			UNIT
			MIN	TYP ⁽¹⁾	MAX	MIN	TYP ⁽¹⁾	MAX	
f _{max}			95			95			MHz
t _{PLH}	A	B	1	2.8	4.5	1.5	2.8	4.1	ns
t _{PHL}			1	2.5	4.5	1.3	2.5	4	
t _{PLH}	LEAB	B	1	3.6	5.5	2	3.6	5.3	ns
t _{PHL}			1	3.5	6	1.9	3.5	5.4	
t _{PLH}	CLKAB	B	1	3.7	5.5	2.3	3.7	5.3	ns
t _{PHL}			1	3.4	5.5	1.9	3.4	5.4	
t _{en}	$\overline{\text{OEAB}}$	B	1	3.3	5.5	2	3.3	5.5	ns
t _{dis}			1	3.4	5.5	2	3.4	5.1	
t _r	Transition time, B outputs (0.5 V to 1 V)		1.3			1.3			ns
t _f	Transition time, B outputs (1 V to 0.5 V)		0.5			0.5			ns
t _{PLH}	B	A	2	4.1	6.9	2.1	4.1	6.3	ns
t _{PHL}			1	2.9	5.1	1.2	2.9	4.6	
t _{PLH}	LEBA	A	2	3.7	6.1	2.3	3.7	5.7	ns
t _{PHL}			1	3	5.1	1.8	3	4.8	
t _{PLH}	CLKBA	A	2	3.8	6.4	2.5	3.8	6.1	ns
t _{PHL}			2	3.3	5.6	2.3	3.3	5.2	
t _{en}	$\overline{\text{OEBA}}$	A	1	5	7.5	2.3	5	7.4	ns
t _{dis}			2	4.3	6.9	2.5	4.3	6.4	

(1) All typical values are at V_{CC} (3.3 V) = 3.3 V, V_{CC} (5 V) = 5 V, $T_A = 25^\circ\text{C}$.

Timing Requirements

over recommended ranges of supply voltage and operating free-air temperature,
 $V_{TT} = 1.5\text{ V}$ and $V_{REF} = 1\text{ V}$ for GTL+ (unless otherwise noted) (see [Figure 1](#))

			SN54GTL16612		SN74GTL16612		UNIT
			MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency		95		95		MHz
t _w	Pulse duration	LEAB or LEBA high	3.3		3.3		ns
		CLKAB or CLKBA high or low	5.6		5.6		
t _{su}	Setup time	A before CLKAB↑	1.3		1.3		ns
		B before CLKBA↑	3.2		2.3		
		A before LEAB↓	1.2		0		
		B before LEBA↓	1.3		1.3		
		$\overline{\text{CEAB}}$ before CLKAB↑	2.1		2		
		$\overline{\text{CEBA}}$ before CLKBA↑	2.6		2.2		
t _h	Hold time	A after CLKAB↑	2.9		1.6		ns
		B after CLKBA↑	4.4		0.3		
		A after LEAB↓	4.5		4		
		B after LEBA↓	4.3		3.6		
		$\overline{\text{CEAB}}$ after CLKAB↑	2		0.8		
		$\overline{\text{CEBA}}$ after CLKBA↑	1.1		1.1		

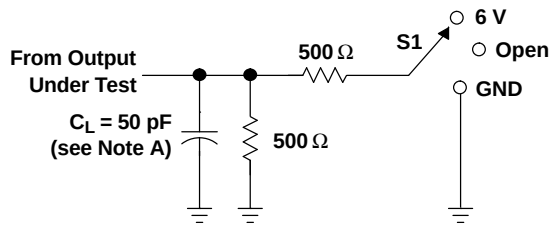
Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature,
 $V_{TT} = 1.5\text{ V}$ and $V_{REF} = 1\text{ V}$ for GTL+ (see [Figure 1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54GTL16612			SN74GTL16612			UNIT
			MIN	TYP ⁽¹⁾	MAX	MIN	TYP ⁽¹⁾	MAX	
f _{max}			95			95			MHz
t _{PLH}	A	B	1	2.8	4.5	1.5	2.8	4.1	ns
t _{PHL}			1	2.5	4.6	1.3	2.5	4.1	
t _{PLH}	LEAB	B	1	3.6	5.5	2	3.6	5.3	ns
t _{PHL}			1	3.5	6.1	1.9	3.5	5.5	
t _{PLH}	CLKAB	B	1	3.7	5.5	2.3	3.7	5.3	ns
t _{PHL}			1	3.4	5.6	1.9	3.4	5.5	
t _{PLH}	$\overline{\text{OEAB}}$	B	1	3.4	5.5	2	3.4	5.1	ns
t _{PHL}			1	3.3	5.6	2	3.3	5.6	
t _r	Transition time, B outputs (0.5 V to 1 V)		1.5			1.5			ns
t _f	Transition time, B outputs (1 V to 0.5 V)		0.8			0.8			ns
t _{PLH}	B	A	1.9	4	6.9	2	4	6.3	ns
t _{PHL}			0.9	2.8	4.9	1.1	2.8	4.4	
t _{PLH}	LEBA	A	2	3.7	6.1	2.3	3.7	5.7	ns
t _{PHL}			1	3	5.1	1.8	3	4.8	
t _{PLH}	CLKBA	A	2	3.8	6.4	2.5	3.8	6.1	ns
t _{PHL}			2	3.3	5.6	2.3	3.3	5.2	
t _{en}	$\overline{\text{OEBA}}$	A	1	5	7.5	2.3	5	7.4	ns
t _{dis}			2	4.3	6.9	2.5	4.3	6.4	

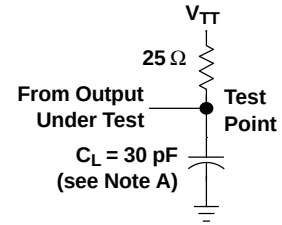
(1) All typical values are at V_{CC} (3.3 V) = 3.3 V, V_{CC} (5 V) = 5 V, $T_A = 25^\circ\text{C}$.

PARAMETER MEASUREMENT INFORMATION
 $V_{TT} = 1.2 \text{ V}$, $V_{REF} = 0.8 \text{ V}$ for GTL and $V_{TT} = 1.5 \text{ V}$, $V_{REF} = 1 \text{ V}$ for GTL+

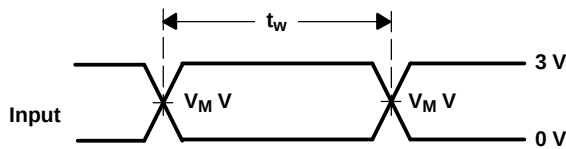


LOAD CIRCUIT FOR A OUTPUTS

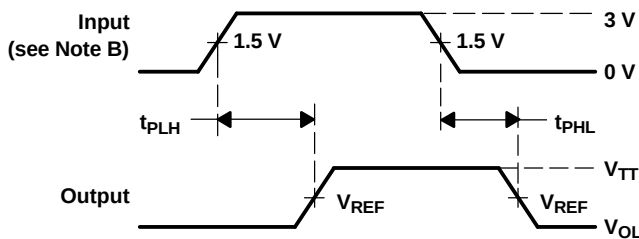
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



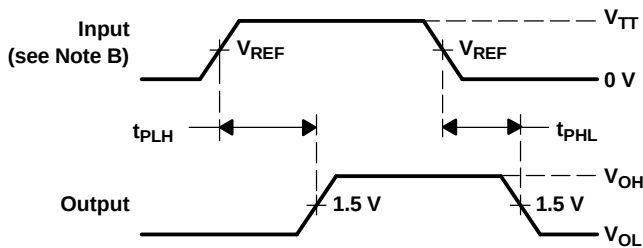
LOAD CIRCUIT FOR B OUTPUTS



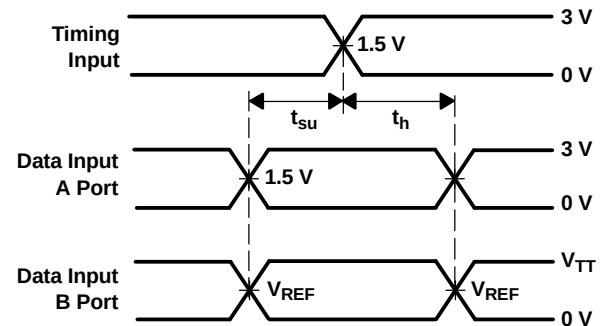
VOLTAGE WAVEFORMS
PULSE DURATION
($V_M = 1.5 \text{ V}$ for A port and V_{REF} for B port)⁽¹⁾



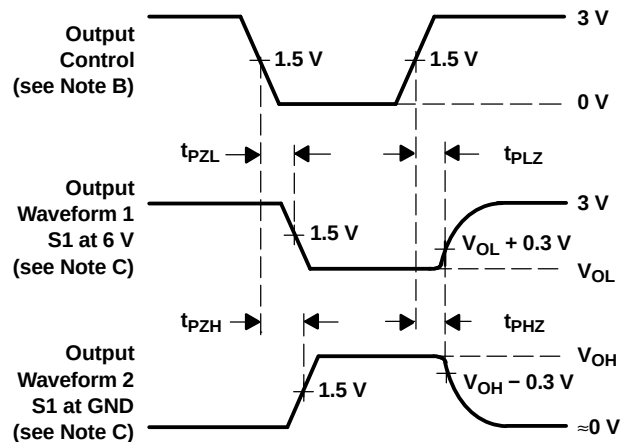
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(A port to B port)⁽¹⁾



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(B port to A port)⁽¹⁾



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
(A port)

⁽¹⁾ All control inputs are TTL levels.

NOTES: A. C_L includes probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.

C. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.

Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.

D. The outputs are measured one at a time, with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74GTL16612DGGR	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	GTL16612	Samples
SN74GTL16612DL	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	GTL16612	Samples
SNJ54GTL16612WD	LIFEBUY	CFP	WD	56		TBD	Call TI	Call TI	-55 to 125	5962-9689001QX A SNJ54GTL16612W D	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

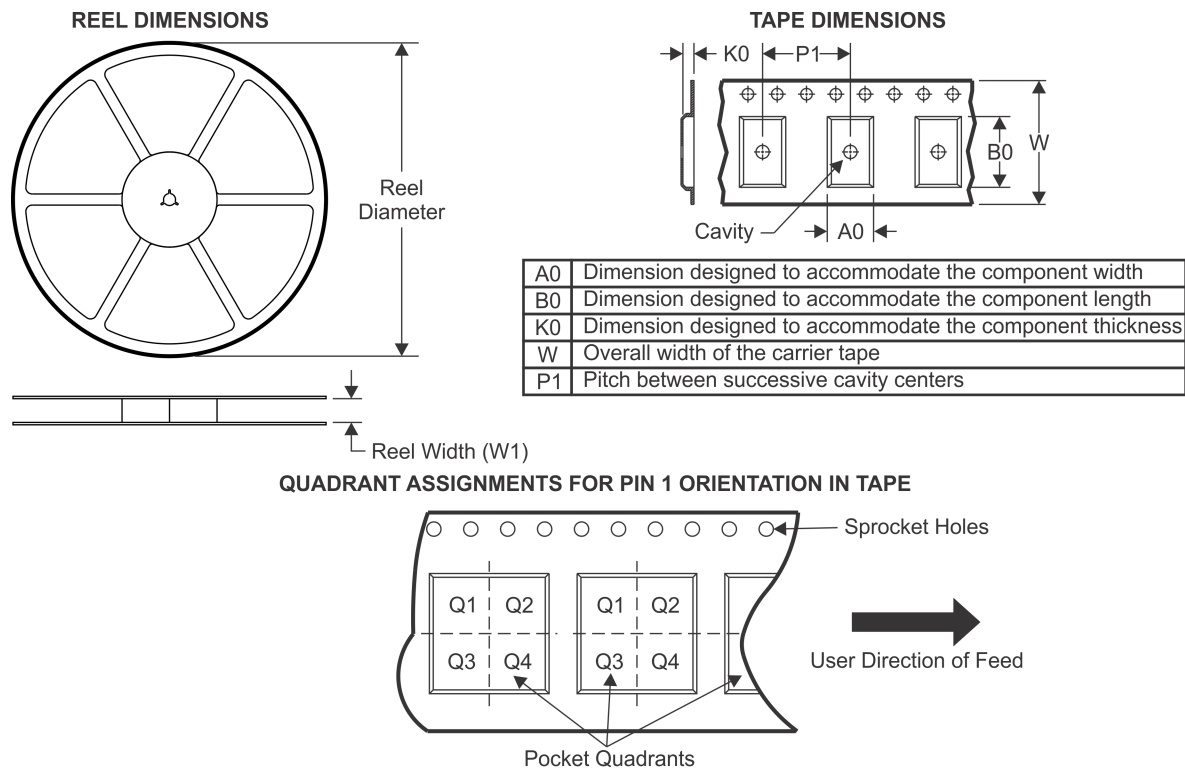
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54GTL16612, SN74GTL16612 :

- Catalog: [SN74GTL16612](#)
- Military: [SN54GTL16612](#)

NOTE: Qualified Version Definitions:

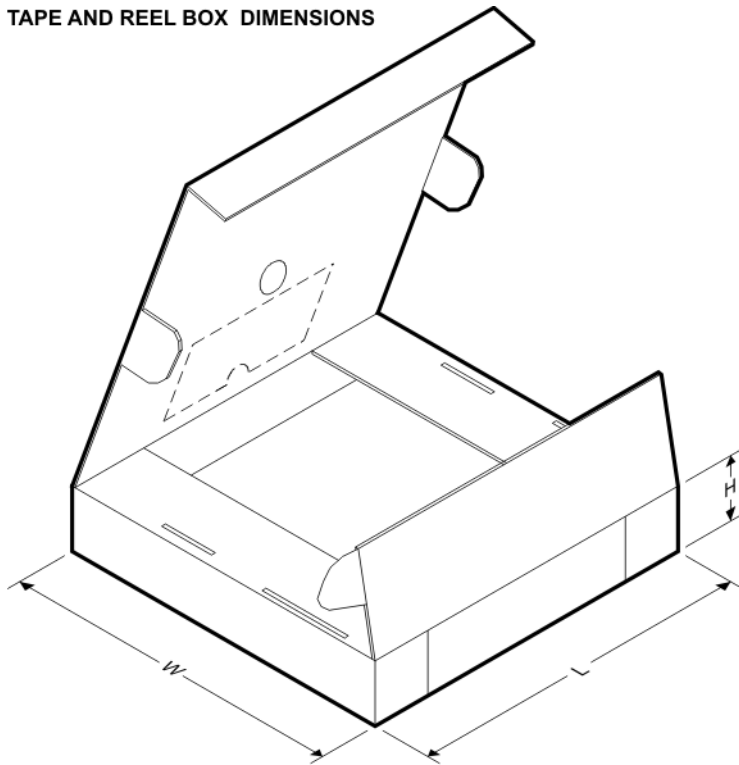
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74GTL16612DGGR	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



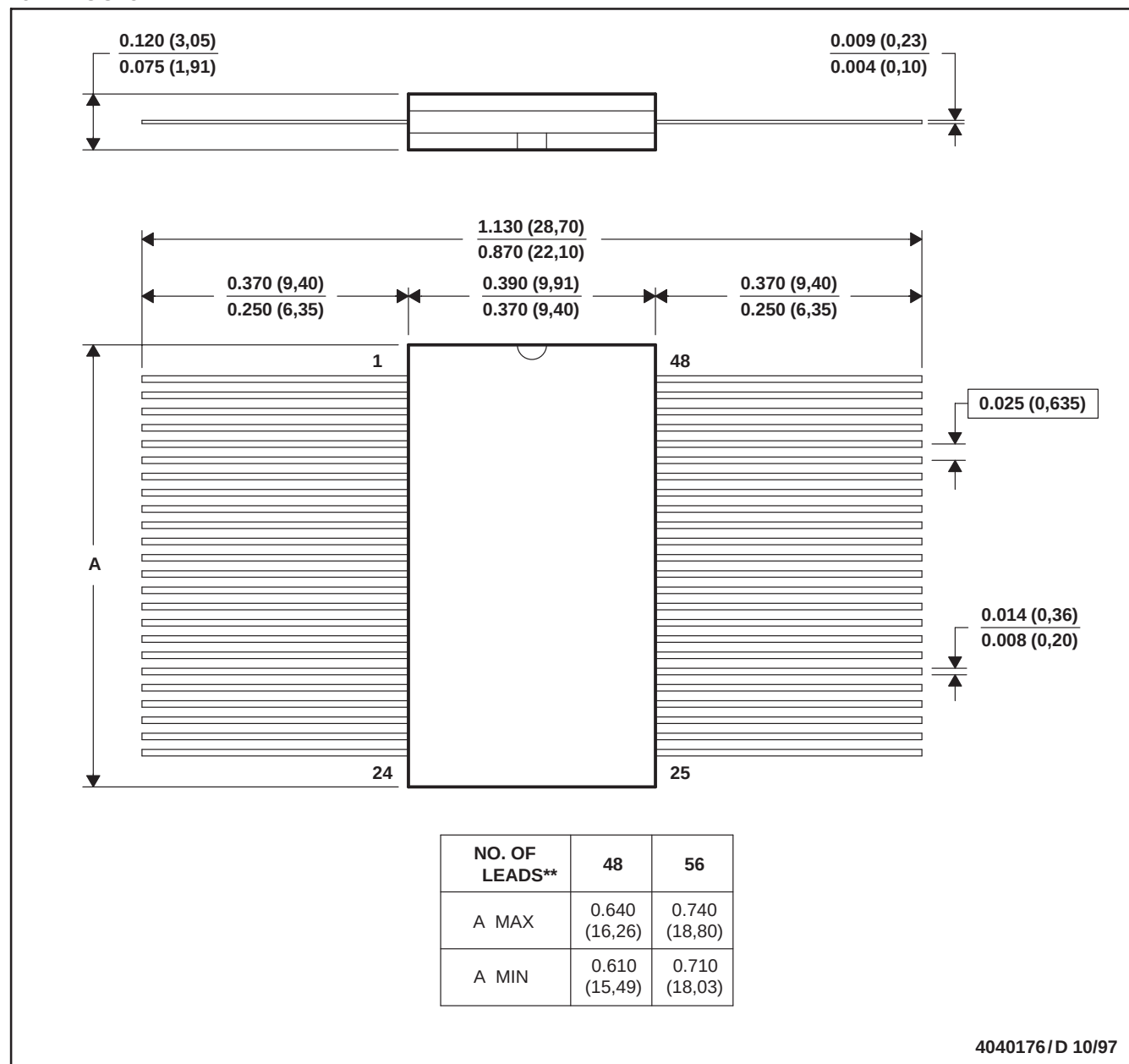
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74GTL16612DGGR	TSSOP	DGG	56	2000	367.0	367.0	45.0

WD (R-GDFP-F**)

CERAMIC DUAL FLATPACK

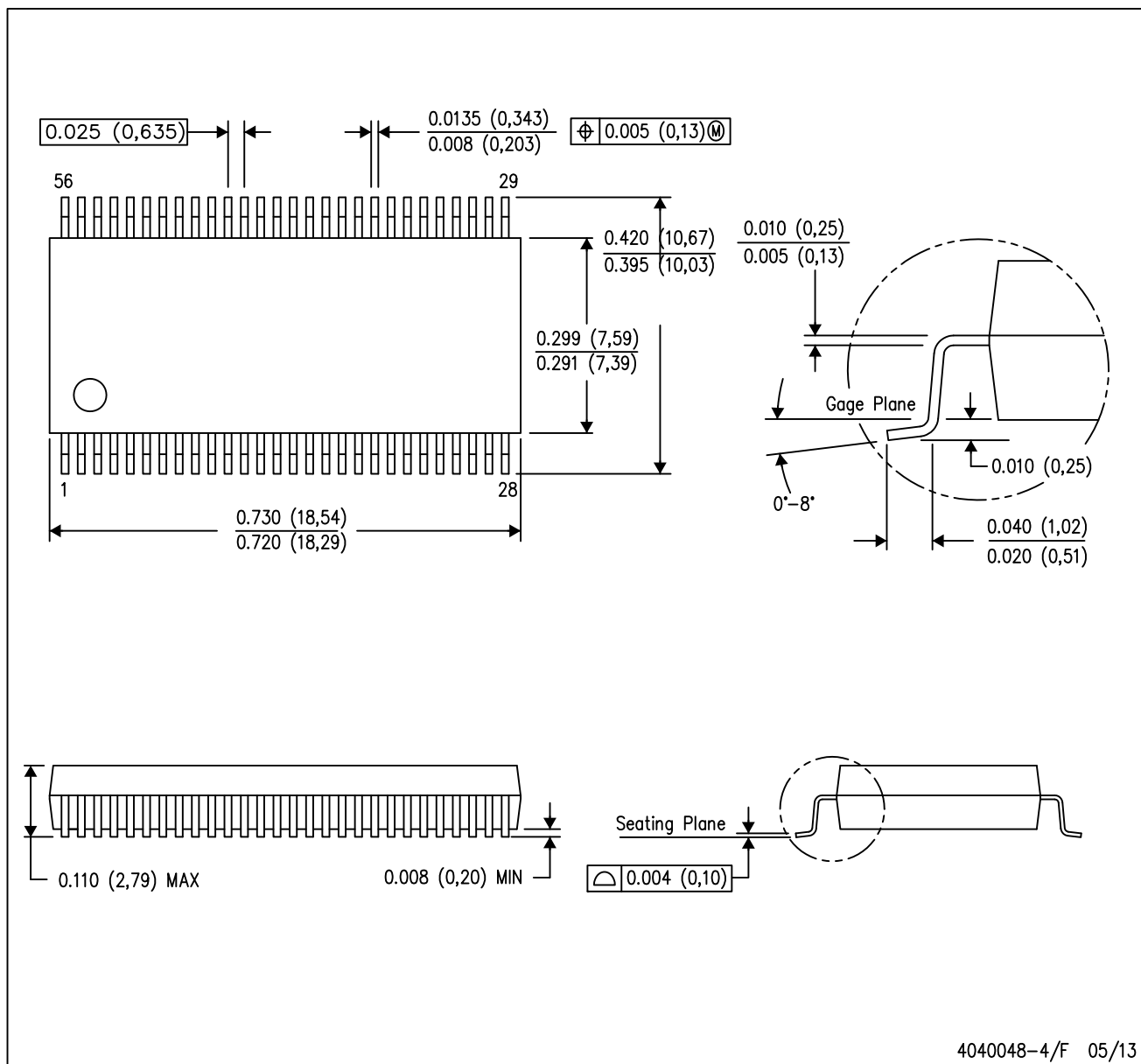
48 LEADS SHOWN



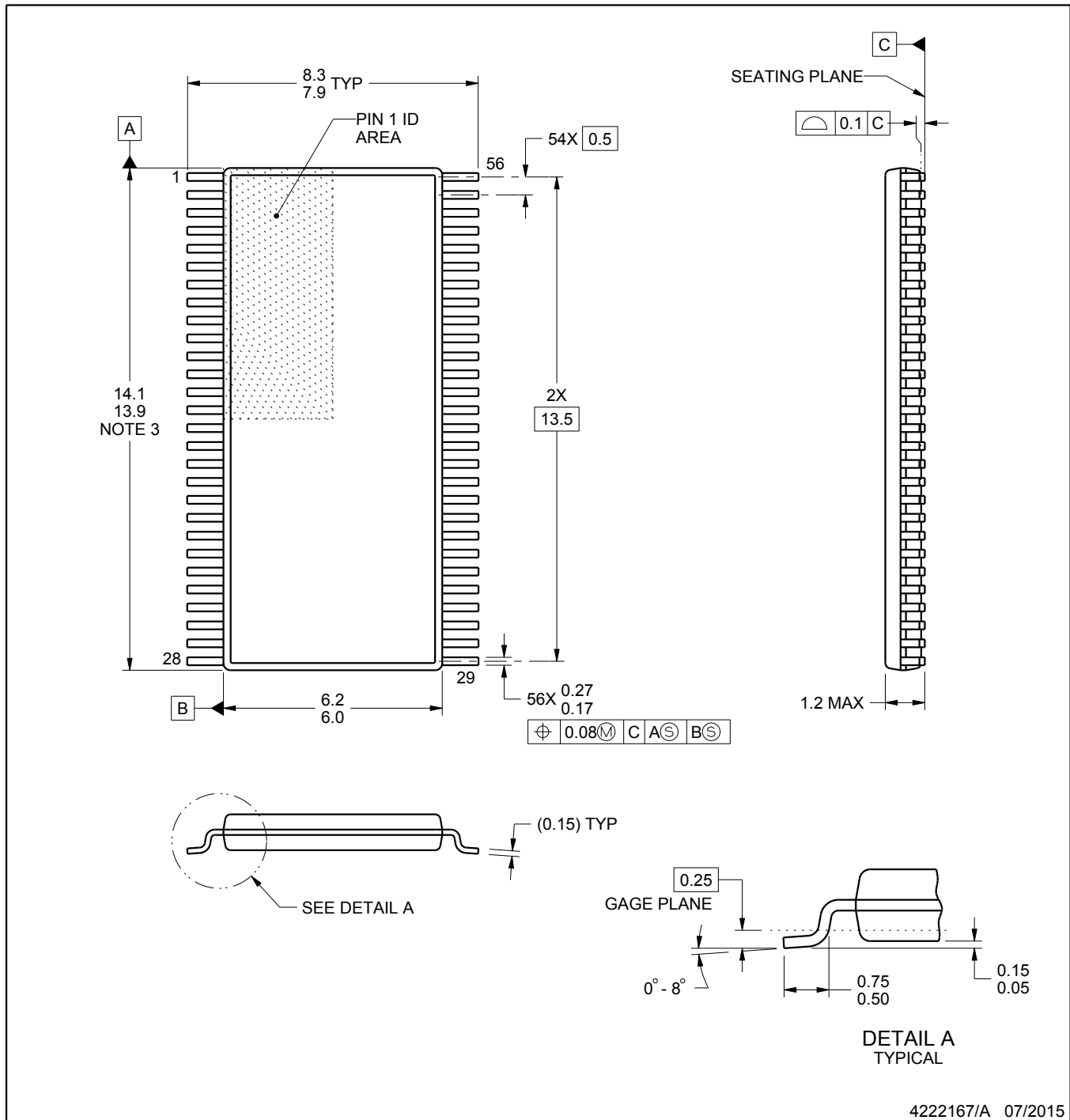
- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only
 - Falls within MIL STD 1835: GDFP1-F48 and JEDEC MO-146AA
GDFP1-F56 and JEDEC MO-146AB

DL (R-PDSO-G56)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MO-118



4222167/A 07/2015

NOTES:

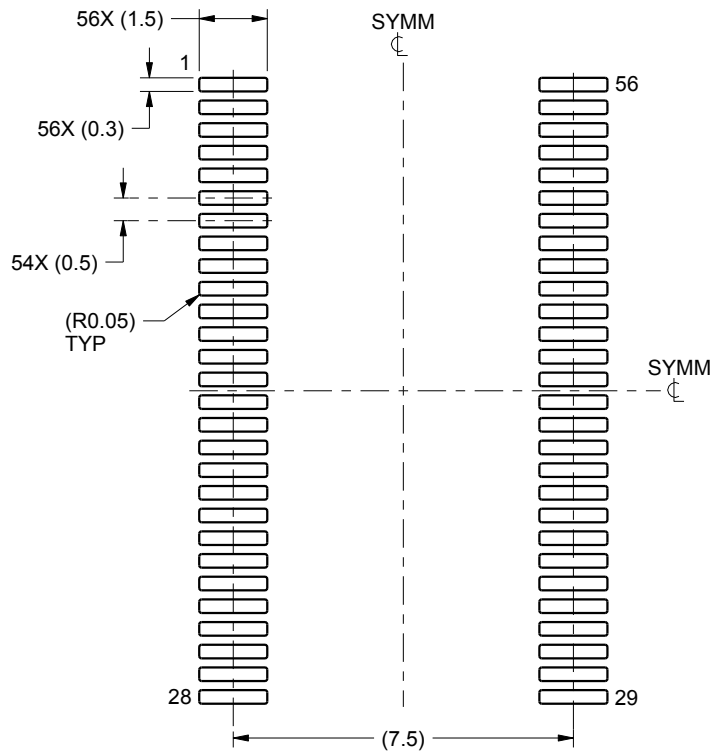
- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

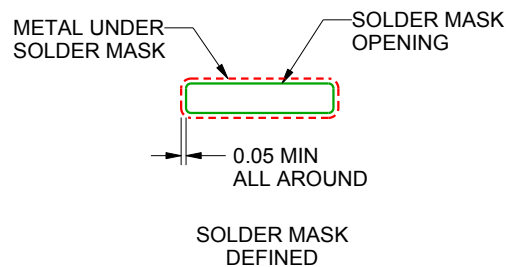
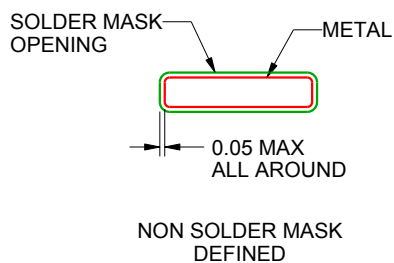
DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4222167/A 07/2015

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

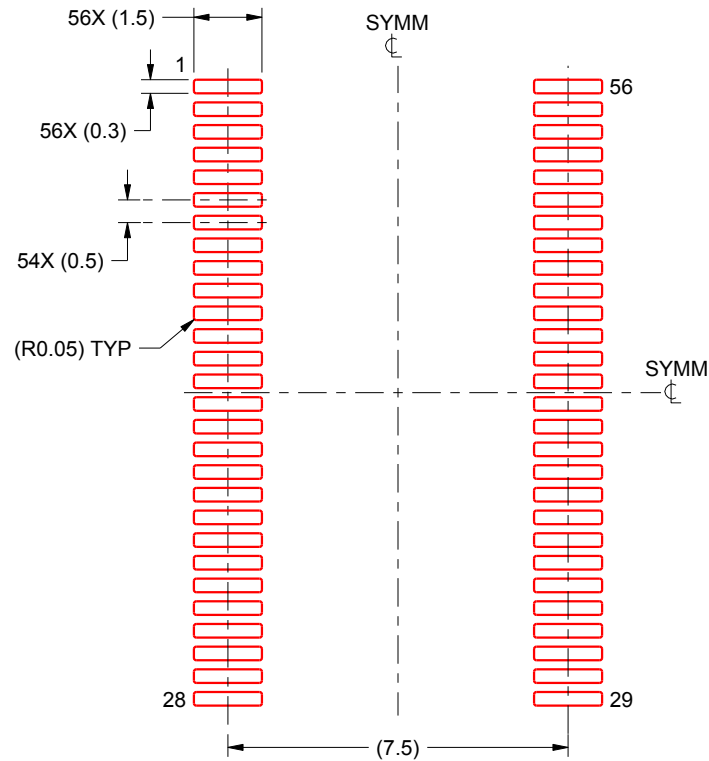
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4222167/A 07/2015

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2019, Texas Instruments Incorporated