

SI7148DP-VB Datasheet

N-Channel 80 V (D-S) MOSFET

PRODUCT SUMMARY			
V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A) ^a	Q _g (Typ.)
80	0.0048 at V _{GS} = 10 V	60	25 nC
	0.0050 at V _{GS} = 7.5 V	60	
	0.0064 at V _{GS} = 4.5 V	60	

FEATURES

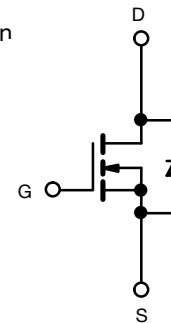
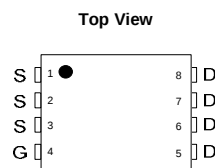
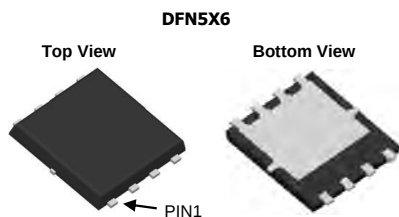
- TrenchFET® power MOSFET
- 100 % R_g and UIS tested

APPLICATIONS

- Primary side switching
- Synchronous rectification
- DC/AC inverters



RoHS
COMPLIANT
HALOGEN
FREE



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, unless otherwise noted)				
Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V _{DS}	80	V
Gate-Source Voltage		V _{GS}	± 20	
Continuous Drain Current (T _J = 150 °C)	T _C = 25 °C	I _D	60 ^a	A
	T _C = 70 °C		60 ^a	
	T _A = 25 °C		23.8 ^{b, c}	
	T _A = 70 °C		19 ^{b, c}	
Pulsed Drain Current (t = 300 μs)		I _{DM}	100	
Continuous Source-Drain Diode Current	T _C = 25 °C	I _S	60 ^a	
	T _A = 25 °C		5.6 ^{b, c}	
Single Pulse Avalanche Current	L = 0.1 mH	I _{AS}	35	mJ
Single Pulse Avalanche Energy		E _{AS}	61	
Maximum Power Dissipation	T _C = 25 °C	P _D	104	W
	T _C = 70 °C		66.6	
	T _A = 25 °C		6.25 ^{b, c}	
	T _A = 70 °C		4 ^{b, c}	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	-55 to 150	°C
Soldering Recommendations (Peak Temperature) ^{d, e}			260	

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{b, f}	t ≤ 10 s	R _{thJA}	15	20	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R _{thJC}	0.9	1.2	

Notes

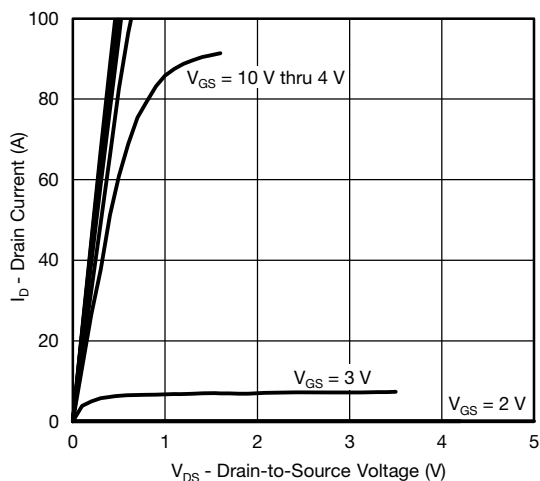
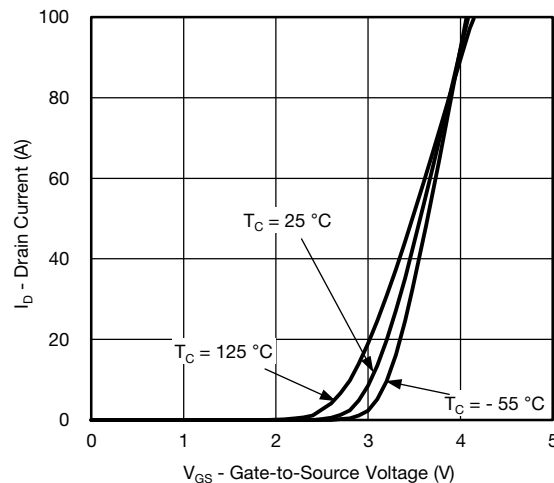
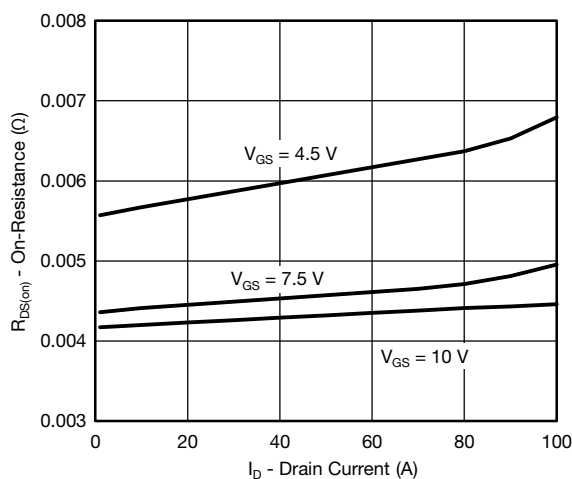
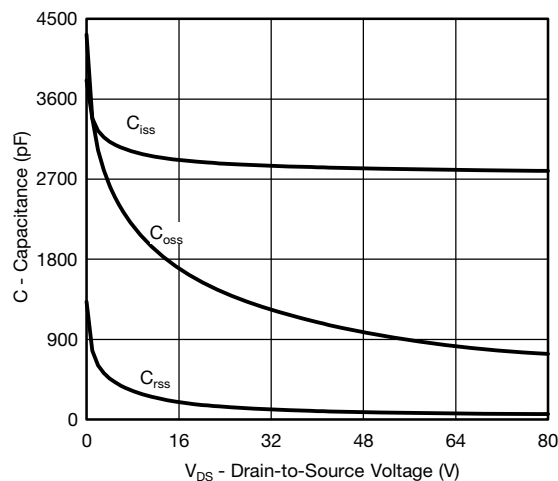
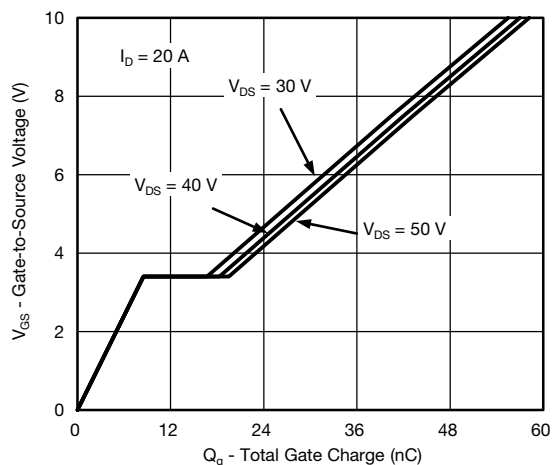
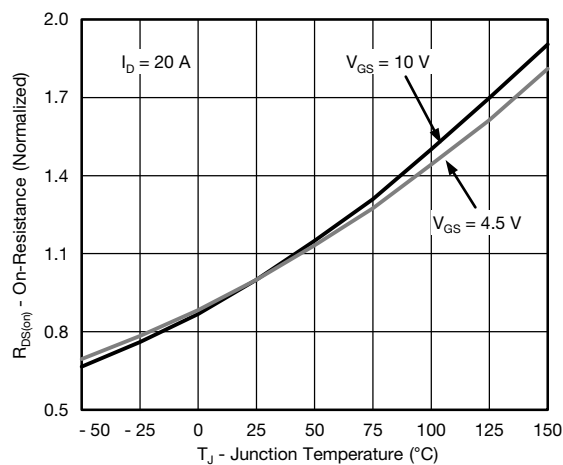
- Package limited.
- Surface mounted on 1" x 1" FR4 board.
- t = 10 s.
- The DFN 5X6 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework conditions: Manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under steady state conditions is 54 °C/W.

SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	80	-	-	V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	I _D = 250 μA	-	47	-	mV/°C
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)} /T _J		-	-5.7	-	
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1.2	-	2.8	V
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V	-	-	± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 80 V, V _{GS} = 0 V	-	-	1	μA
		V _{DS} = 80 V, V _{GS} = 0 V, T _J = 55 °C	-	-	10	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	30	-	-	A
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 20 A	-	0.0048	-	Ω
		V _{GS} = 7.5 V, I _D = 20 A	-	0.0050	-	
		V _{GS} = 4.5 V, I _D = 15 A	-	0.0064	-	
Forward Transconductance ^a	g _{fs}	V _{DS} = 10 V, I _D = 20 A	-	68	-	S
Dynamic ^b						
Input Capacitance	C _{iss}	V _{DS} = 40 V, V _{GS} = 0 V, f = 1 MHz	-	2800	-	pF
Output Capacitance	C _{oss}		-	1100	-	
Reverse Transfer Capacitance	C _{rss}		-	93	-	
Total Gate Charge	Q _g	V _{DS} = 40 V, V _{GS} = 10 V, I _D = 20 A	-	57	86	nC
		V _{DS} = 40 V, V _{GS} = 7.5 V, I _D = 20 A	-	42	63	
		V _{DS} = 40 V, V _{GS} = 4.5 V, I _D = 20 A	-	25	38	
Gate-Source Charge	Q _{gs}		-	8.5	-	
Gate-Drain Charge	Q _{gd}		-	10	-	
Output Charge	Q _{oss}	V _{DS} = 40 V, V _{GS} = 0 V	-	70	105	
Gate Resistance	R _g	f = 1 MHz	0.3	0.95	1.9	Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = 40 V, R _L = 2 Ω I _D ≅ 20 A, V _{GEN} = 10 V, R _g = 1 Ω	-	9	18	ns
Rise Time	t _r		-	12	24	
Turn-Off Delay Time	t _{d(off)}		-	34	68	
Fall Time	t _f		-	7	14	
Turn-On Delay Time	t _{d(on)}	V _{DD} = 40 V, R _L = 2 Ω I _D ≅ 20 A, V _{GEN} = 7.5 V, R _g = 1 Ω	-	16	32	
Rise Time	t _r		-	15	30	
Turn-Off Delay Time	t _{d(off)}		-	32	64	
Fall Time	t _f		-	8	16	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C	-	-	60	A
Pulse Diode Forward Current ^a	I _{SM}		-	-	100	
Body Diode Voltage	V _{SD}	I _S = 5 A	-	0.73	1.1	V
Body Diode Reverse Recovery Time	t _{rr}	I _F = 20 A, dI/dt = 100 A/μs, T _J = 25 °C	-	53	105	ns
Body Diode Reverse Recovery Charge	Q _{rr}		-	65	130	nC
Reverse Recovery Fall Time	t _a		-	25	-	ns
Reverse Recovery Rise Time	t _b		-	28	-	

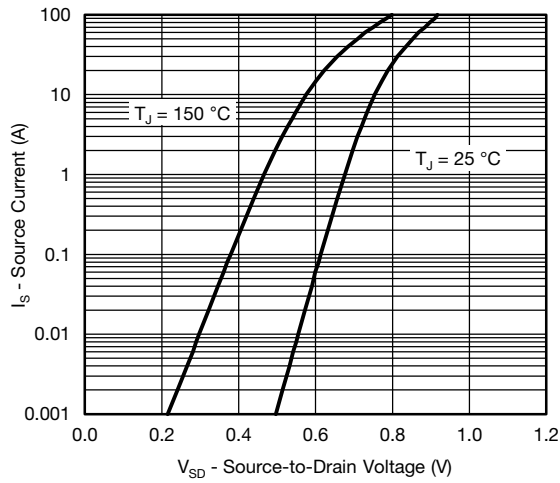
Notes

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
 b. Guaranteed by design, not subject to production testing.

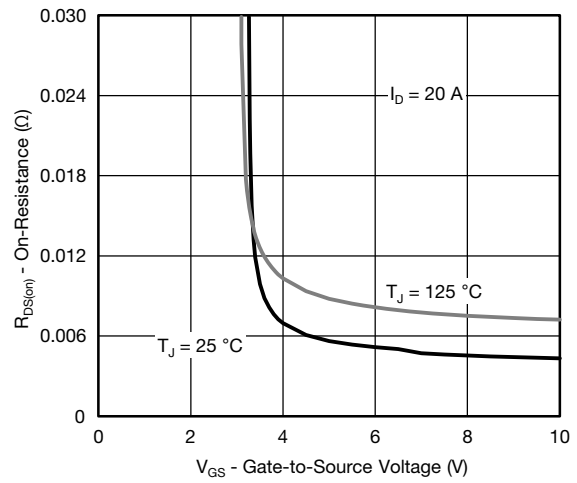
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Output Characteristics

Transfer Characteristics

On-Resistance vs. Drain Current

Capacitance

Gate Charge

On-Resistance vs. Junction Temperature

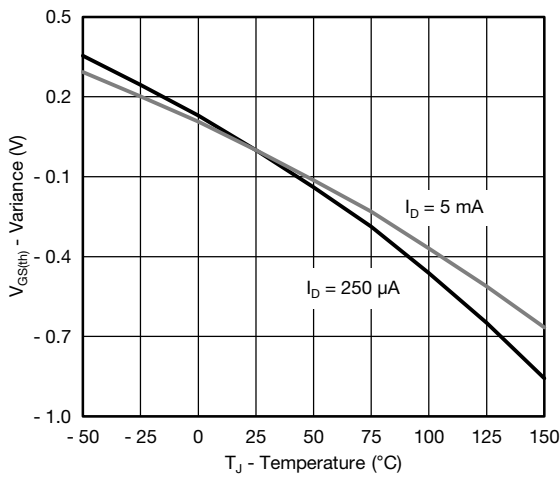
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



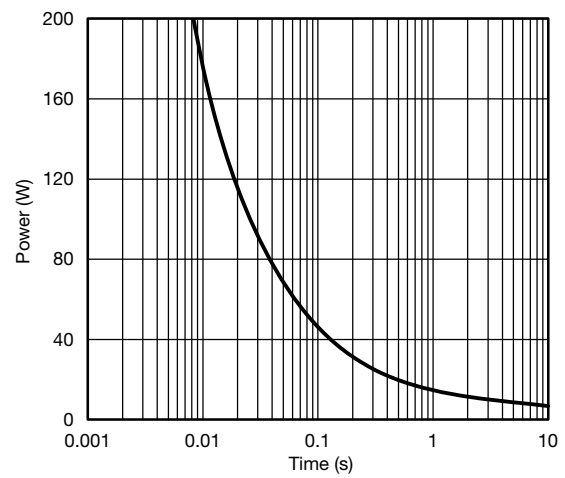
Source-Drain Diode Forward Voltage



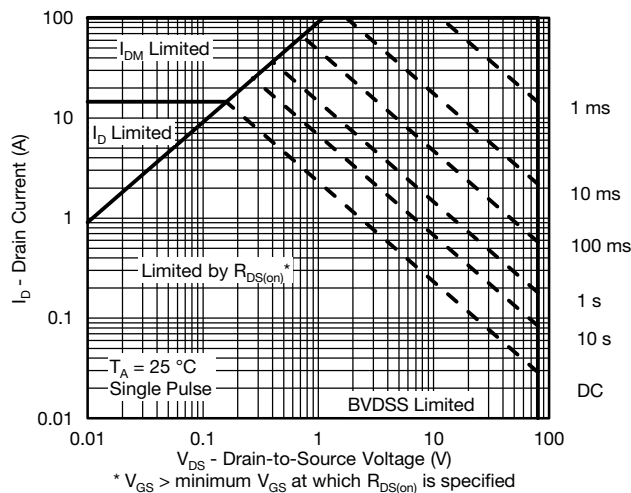
On-Resistance vs. Gate-to-Source Voltage



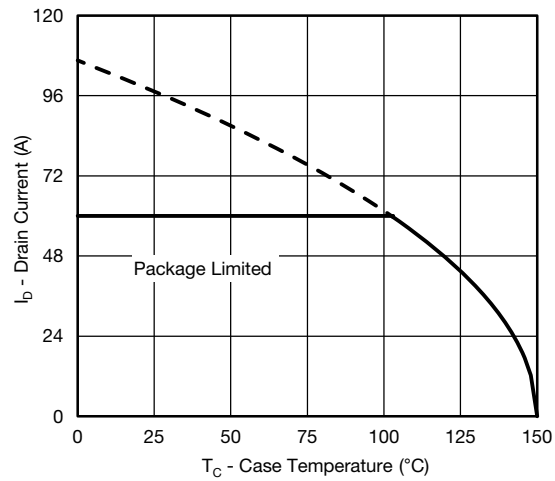
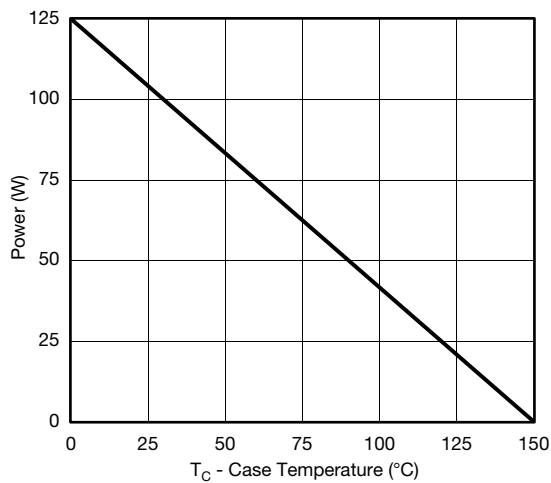
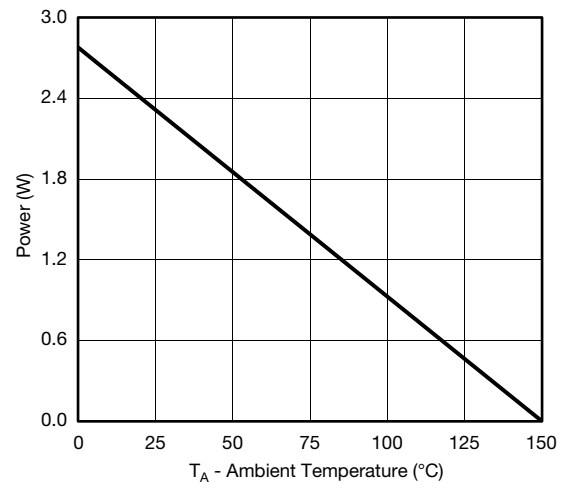
Threshold Voltage



Single Pulse Power, Junction-to-Ambient

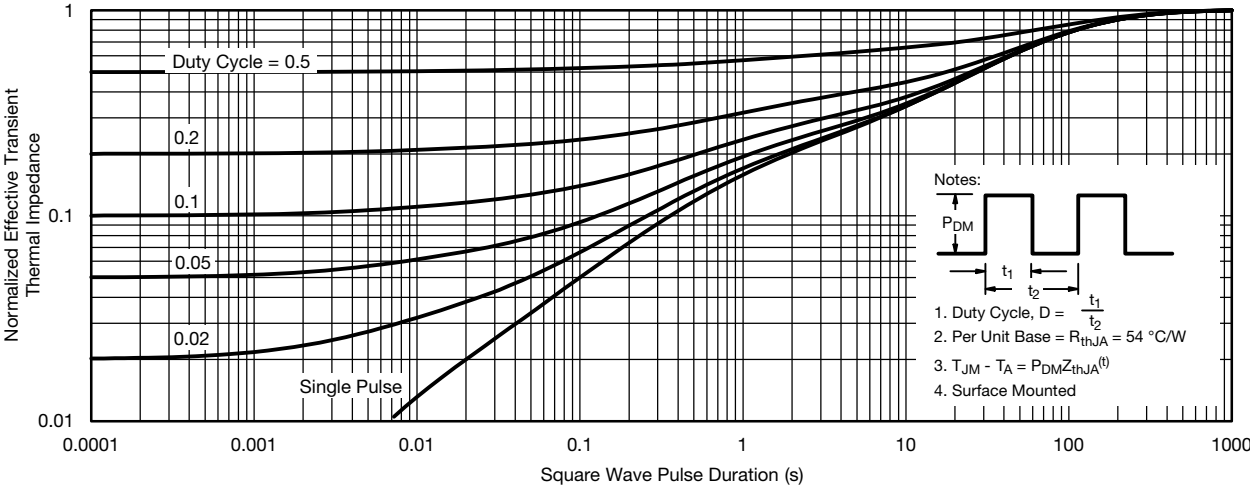


Safe Operating Area, Junction-to-Ambient

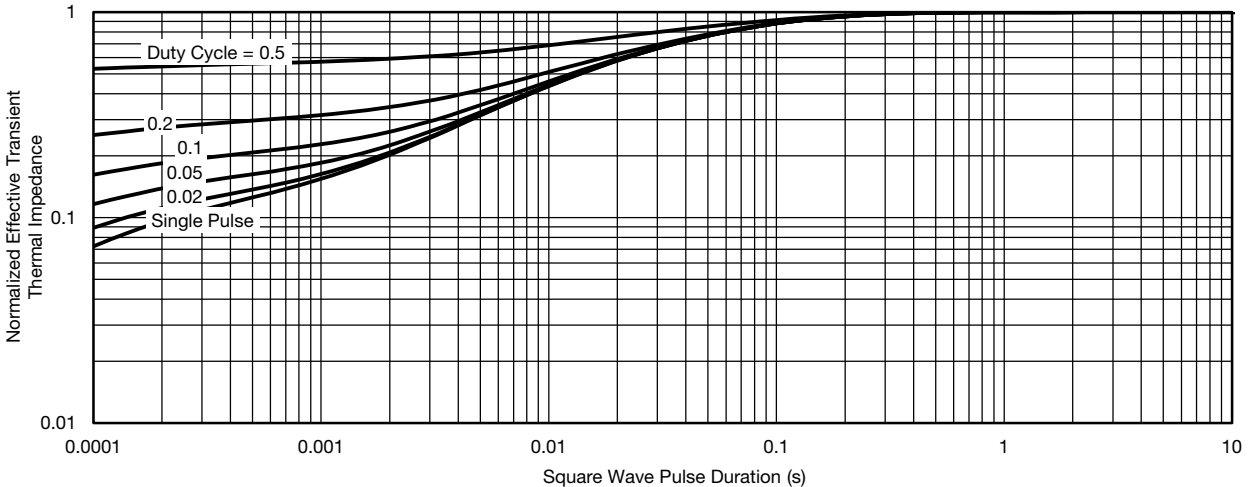
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Current Derating*

Power, Junction-to-Case

Power, Junction-to-Ambient

* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient

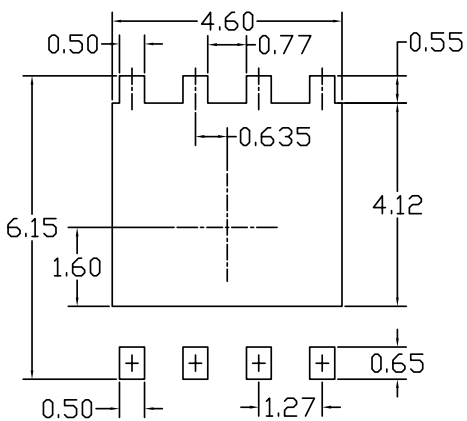


Normalized Thermal Transient Impedance, Junction-to-Case

DFN5x6_8L_EP1_P PACKAGE OUTLIN



RECOMMENDED LAND PATTERN



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.85	0.95	1.00	0.033	0.037	0.039
A1	0.00	---	0.05	0.000	---	0.002
b	0.30	0.40	0.50	0.012	0.016	0.020
c	0.15	0.20	0.25	0.006	0.008	0.010
D	5.10	5.20	5.30	0.201	0.205	0.209
D1	4.25	4.35	4.45	0.167	0.171	0.175
E	5.45	5.55	5.65	0.215	0.219	0.222
E1	5.95	6.05	6.15	0.234	0.238	0.242
E2	3.525	3.625	3.725	0.139	0.143	0.147
E3	1.175	1.275	1.375	0.046	0.050	0.054
e	1.27 BSC			0.050 BSC		
L	0.45	0.55	0.65	0.018	0.022	0.026
L1	0	---	0.15	0	---	0.006
L2	0.68 REF			0.027 REF		
θ	0°	---	10°	0°	---	10°

UNIT: mm

NOTE

1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
MOLD FLASH AT THE NON-LEAD SIDES SHOULD BE LESS THAN 6 MILS EACH.
2. CONTROLLING DIMENSION IS MILLIMETER.
CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.

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