1.0mΩ, 40V, N-Channel Power MOSFET SRT04N010LC

General Description

The Sanrise SRT04N010LC is a low voltage power MOSFET, fabricated using advanced split gate trench technology. The resulting device has extremely low on resistance, low gate charge and fast switching time, making it especially suitable for applications which require superior power density and synchronous rectification.

The SRT04N010LC break down voltage is 40V and it has a high rugged avalanche characteristics.

The SRT04N010LC is available in PDFN5*6 package.

Features

- Ultra Low $R_{DS(ON)\_TYP}$ = 0.72mΩ @V_{GS} = 10V.
- Ultra Low Gate Charge, Qg=105nC typ.
- Fast switching capability
- Robust design with better EAS performance
- EMI Improved
- Non-automotive Qualified

Application

- Server/Telecom
- DC/DC Converter
- High Power Supply
- E-Tools
- BMS

Symbol

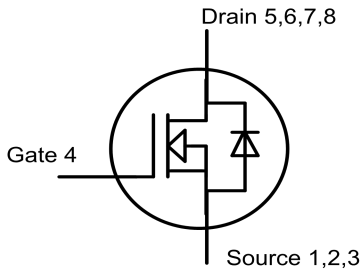
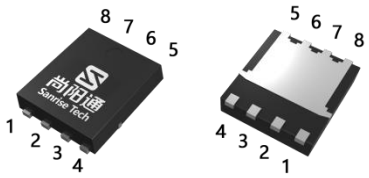


Figure 1 Symbol of SRT04N010LC

Package Type



PDFN5*6

Figure 2 Package Type of SRT04N010LC

Ordering Information

SRT04N010LC□□–□

Circuit Type

Package

C56: PDFN5*6 Clip

E: Lead Free

G: Green

Blank: Tube

TR: Tape & Reel

Package	Part Number	Marking ID	Packing Type
PDFN5*6	SRT04N010LC56TR-G	SRT04N010LC56G	Tape & Reel

1.0mΩ, 40V, N-Channel Power MOSFET SRT04N010LC

Absolute Maximum Ratings

Parameter		Symbol	Rating	Unit
Drain-Source Voltage		V_{DSS}	40	V
Gate-Source Voltage		V_{GSS}	±20	V
Continuous Drain Current, Silicon	T_C=25ºC	I_D	304	A
	T_C=100ºC		215	
Pulsed Drain Current (Note 3)		I_{DM}	1216	A
Power Dissipation (T_C = 25°C)		P_D	166	W
Avalanche Destructive Energy, Single Pulse (Note 5)		E_{AS_Limit}	841	mJ
Avalanche Energy, Single Pulse (Note 4)		E_{AS}	306	mJ
Avalanche Current, Repetitive (Note 3)		I_{AR}	50.0	A
Continuous Diode Forward Current		I_S	304	A
Diode Pulse Current		$I_{S.PULSE}$	1216	A
Operating Junction Temperature		T_J	175	ºC
Storage Temperature		T_{STG}	-55 to 175	ºC
Lead Temperature (Soldering, 10 sec)		T_{LEAD}	260	ºC

Note:

1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. Current Limited by Package.
3. Repetitive Rating: Pulse width limited by maximum junction temperature
4. I_{AS}= 35A, V_{DD}= 20V, R_G= 25Ω, Starting T_J= 25°C
5. I_{AS_Limit}= 58.0A, V_{DD}= 20V, R_G= 25Ω, Starting T_J= 25°C

Thermal Resistance

Parameter		Symbol	Min	Typ	Max	Unit
Thermal Resistance，Junction-to-Case	PDFN5*6	R_{thJC}			0.90	ºC/W
Thermal Resistance，Junction-to-Ambient	PDFN5*6	R_{thJA}			50	

Electrical Characteristics

1.0mΩ, 40V, N-Channel Power MOSFET SRT04N010LC

T_J = 25℃, unless otherwise specified.

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Statistic Characteristics							
Drain-Source Breakdown Voltage		BV_{DSS}	V_{GS}=0V, I_D=250uA	40			V
Zero Gate Voltage Drain Current		I_{DSS}	V_{DS}=40V, V_{GS}=0V			1	uA
Gate-Body Leakage Current	Forward	I_{GSSF}	V_{GS}=20V, V_{DS}=0V			200	nA
	Reverse	I_{GSSR}	V_{GS}=-20V, V_{DS}=0V			-200	
Gate Threshold Voltage		$V_{GS(TH)}$	V_{DS}=V_{GS}, I_D=0.25mA	1.2	1.8	2.4	V
Static Drain-Source On-Resistance		$R_{DS(ON)}$	V_{GS}=10V, I_D=60A		0.72	0.95	mΩ
			V_{GS}=4.5V, I_D=30A		1.25	2.00	
Gate Resistance		R_G	f=1MHz, Open Drain		1.6		Ω
Dynamic Characteristics							
Input Capacitance		C_{ISS}	V_{DS}=20V, V_{GS}=0V, f=1MHz		7.4		nF
Output Capacitance		C_{OSS}			2.0		nF
Reverse Transfer Capacitance		C_{RSS}			160		pF
Effective output capacitance, energy related NOTE5		$C_{O(er)}$	V_{GS}=0V, V_{DS}=0…32V		3.1		nF
Effective output capacitance, time related NOTE6		$C_{O(tr)}$			3.8		
Turn-on Delay Time		$t_{d(on)}$	V_{DD}=20V, I_D=60A R_G=1.6Ω, V_{GS}=10V		19		ns
Rise Time		t_r			57		
Turn-off Delay Time		$t_{d(off)}$			62		
Fall Time		t_f			13		
Gate Charge Characteristics							
Gate to Source Charge		Q_{gs}	V_{DD}=20V, I_D=60A V_{GS}=0 to 10V		16		nC
Gate to Drain Charge		Q_{gd}			12		
Gate Charge Total		Q_g			105		
Gate Plateau Voltage		$V_{plateau}$			2.4		V
Gate Charge Total, sync FET		Q_g	V_{DD}=0.1V, V_{GS}=0 to 10V		99		nC
Reverse Diode Characteristics							
Drain-Source Diode Forward Voltage		V_{SD}	V_{GS}=0V, I_{SD}=60A		0.84	1.0	V
Reverse Recovery Time		t_{rr}	V_R=20V, I_F=60A dI$_F$/dt=100A/us		62		ns
Reverse Recovery Charge		Q_{rr}			130		nC
Peak Reverse Recovery Current		I_{rrm}			4.3		A

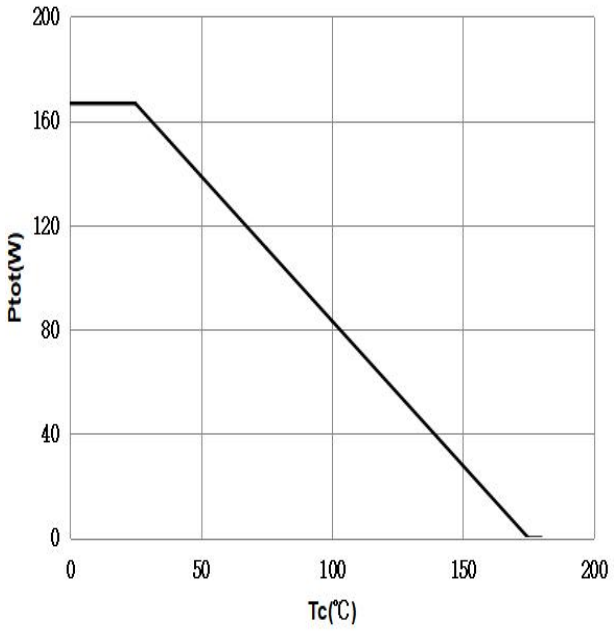
Note:

5. $C_{O(er)}$ is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 32V

6. $C_{O(tr)}$ is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 32V

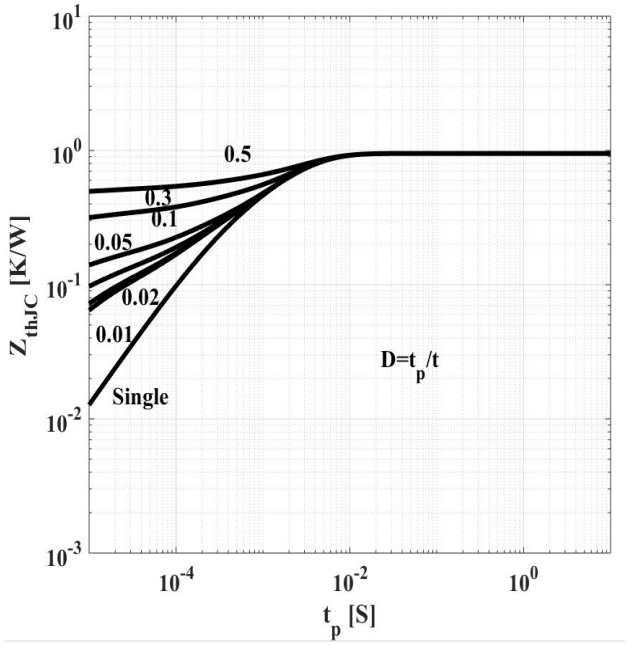
Typical Performance Characteristics

Figure 3: Power Dissipation



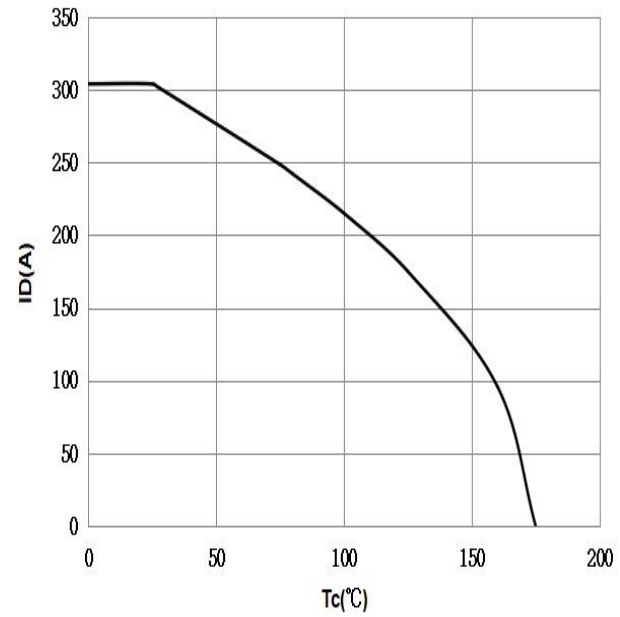
$P_{tot}=f(T_c)$

Figure 4: Max. Transient Thermal Impedance



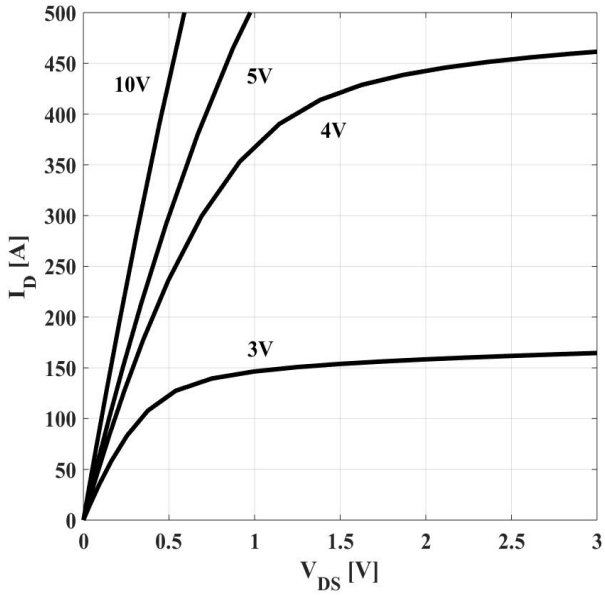
$Z_{(thJC)}=f(t_p)$; parameter: $D=t_p/T$

Figure5: Drain Current



$I_D=f(T_C)$;$V_{GS}\geq 10V$

Figure6: Typ. Output Characteristics



$I_D=f(V_{DS})$;Tj=25ºC; parameter: V_{GS}

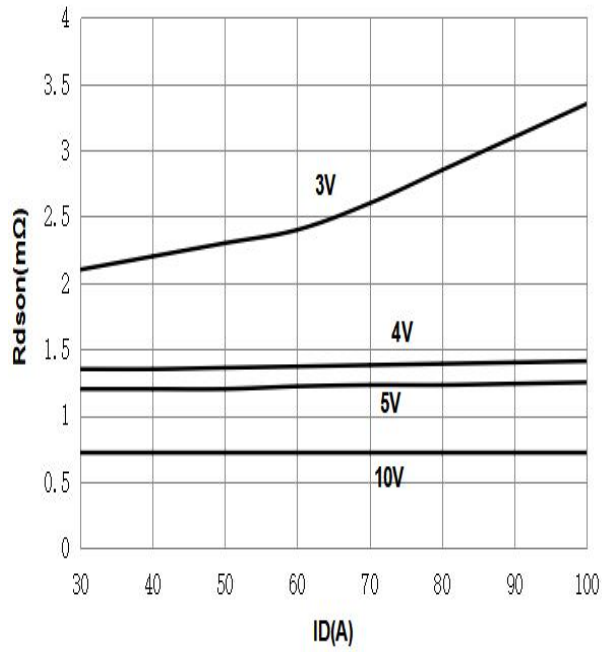
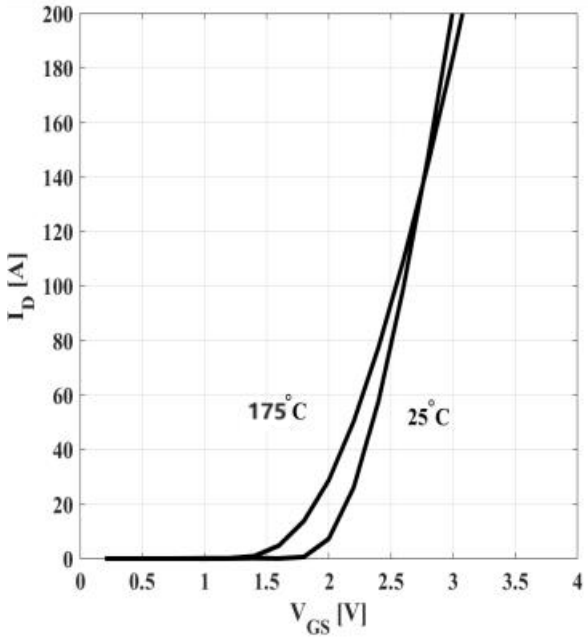
Figure7: Typ. Drain-Source On-State Resistance	Figure8: Typ. Transfer Characteristics
	
$R_{DS(ON)}$=f(I_D);T_j=25ºC; parameter: V_{GS}	I_D=f(V_{GS}); |V_{DS}|>2|I_D|$R_{DS(on)max}$; parameter: T_j

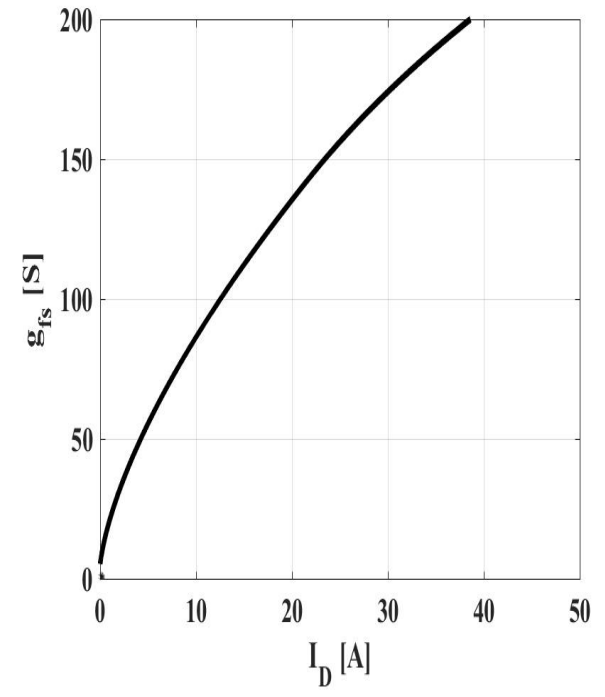
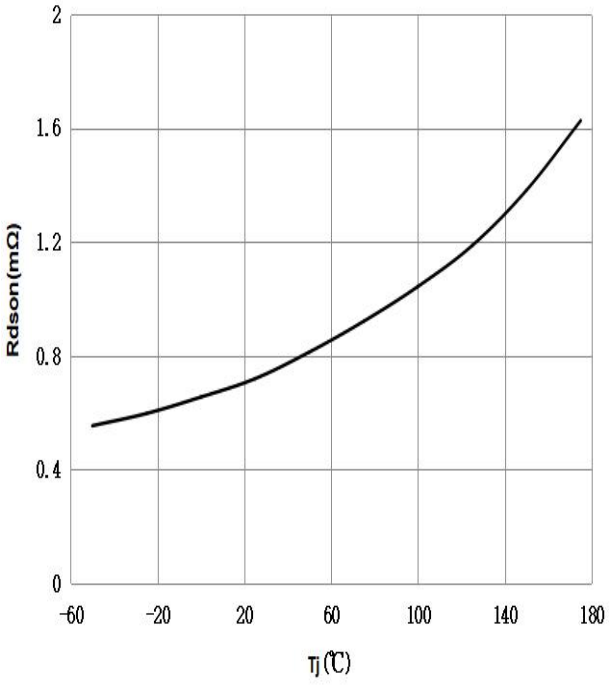
Figure9: Typ. Forward Transconductance	Figure10: Typ. Drain-Source On-State Resistance
	
g_{fs}=f(I_D); T_j=25°C	$R_{DS(ON)}$=f(T_j);I_D=60A;V_{GS}=10V

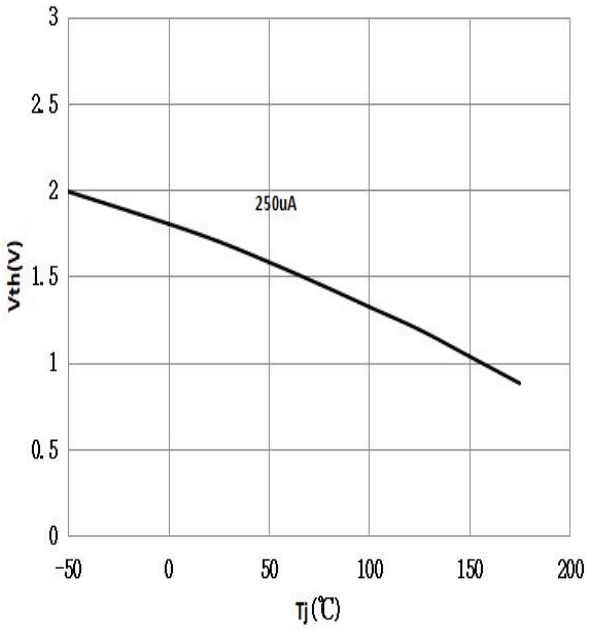
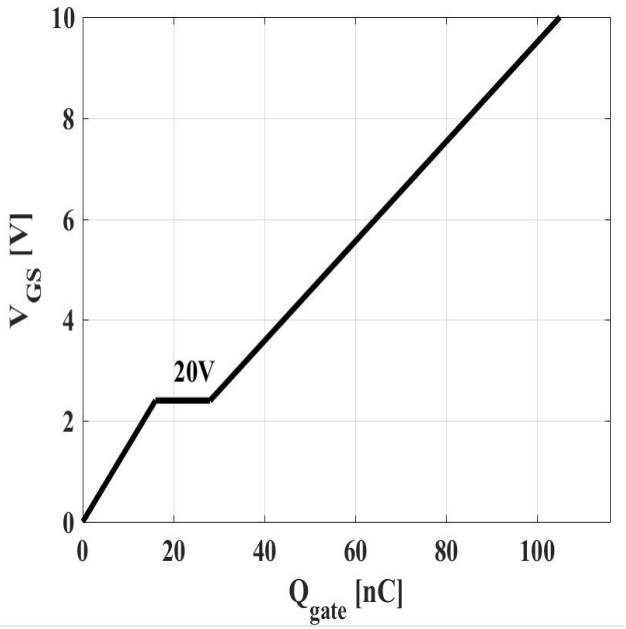
Figure11: Typ. Gate Threshold Voltage	Figure 12: Typ. Gate Charge
	
$V_{GS(th)}=f(T_j)$; $V_{GS}=V_{DS}$; $I_{DS}=250\mu A$	$V_{GS}= f(Q_{gate})$, $I_D=60A$ pulsed

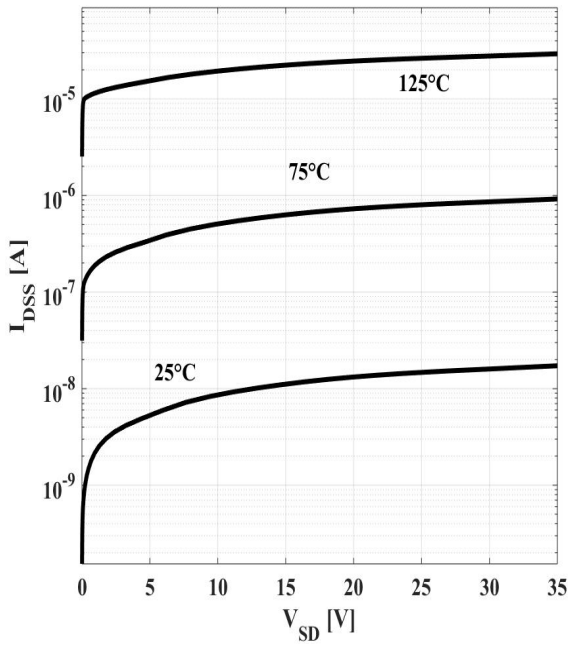
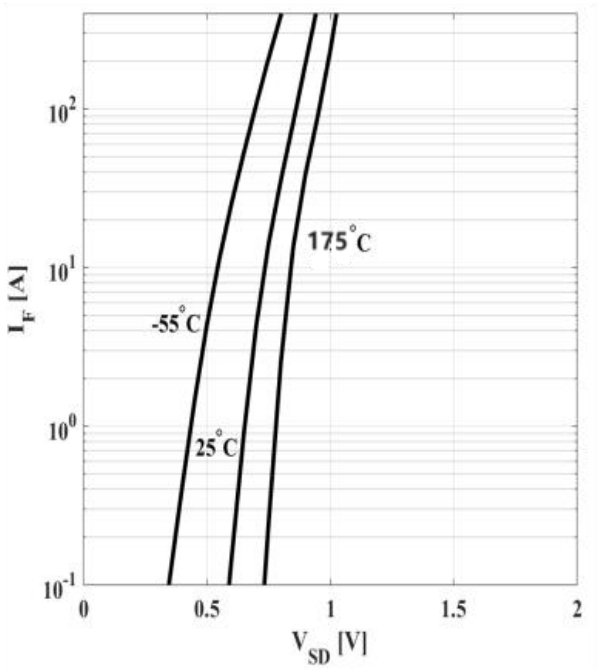
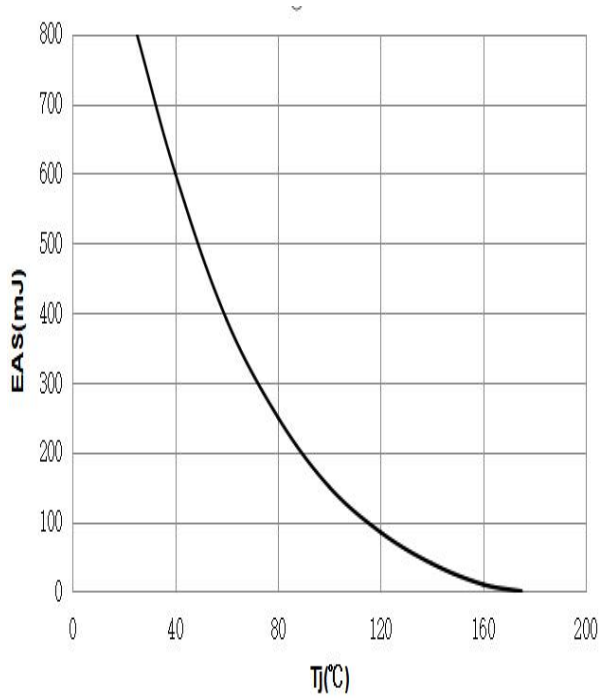
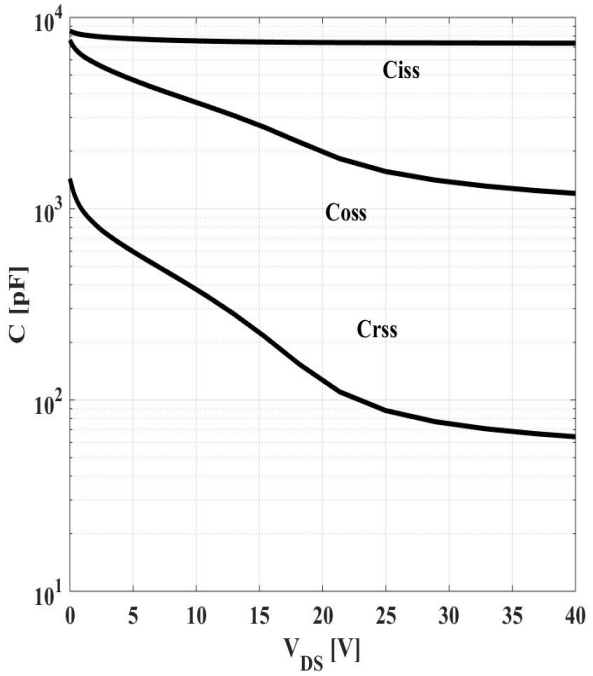
Figure 13: Drain-Source Leakage Current	Figure 14: Forward Characteristics of Reverse Diode
	
$I_{DSS}=f(V_{DS})$; $V_{GS}=0V$; parameter: T_j	$I_F=f(V_{SD})$; parameter: T_j

Figure 15: Avalanche Energy



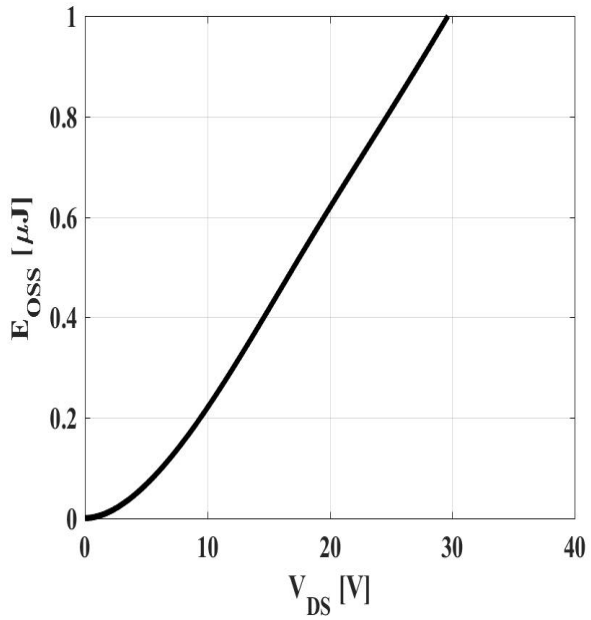
$E_{AS}=f(T_j)$;I_D=50.0A; V_{DD}=20V

Figure 16: Typ. Capacitances



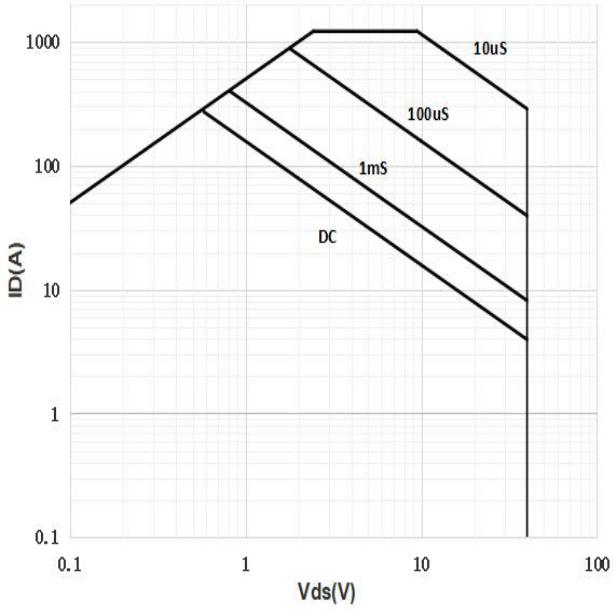
C=f(V_{DS}); V_{GS}=0; f=1MHz

Figure 17: C_{OSS} Stored Energy



$E_{OSS}=f(V_{DS})$

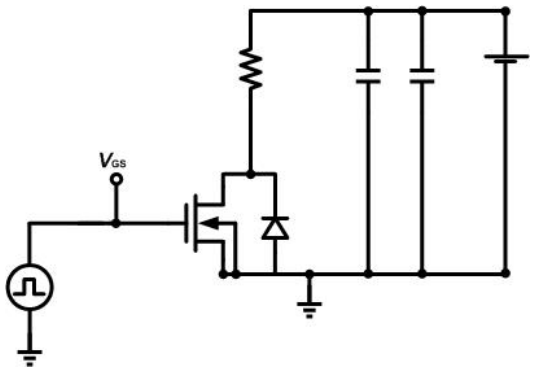
Figure 18: Safe Operating Area

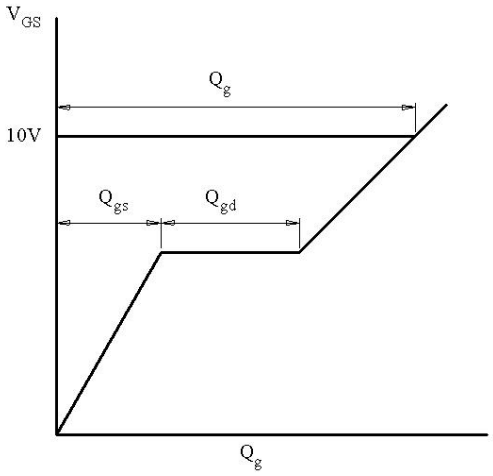


I_D = f(V_{DS}); T_c= 25ºC; V_{GS}>7V; parameter t_p

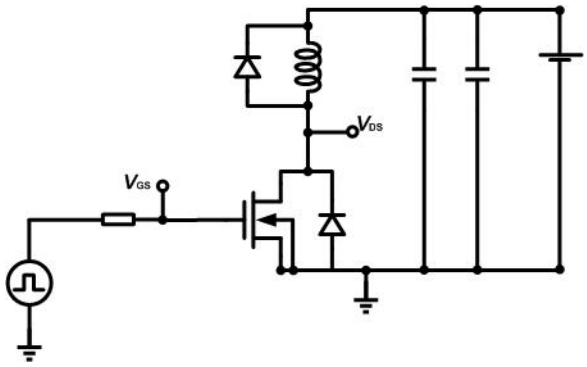
Test Circuits

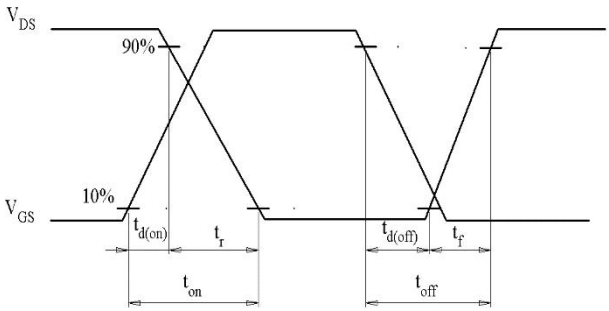
1. Gate Charge Test Circuit & Waveform



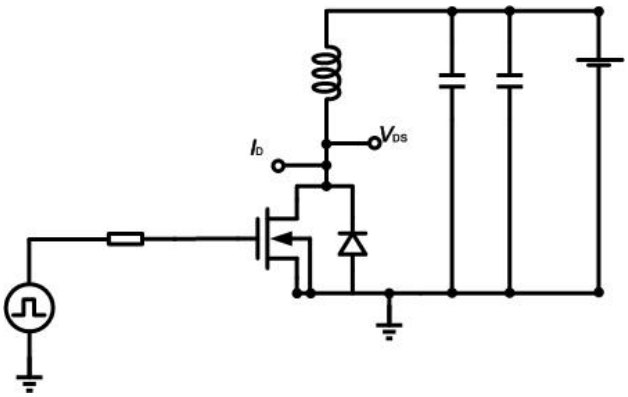


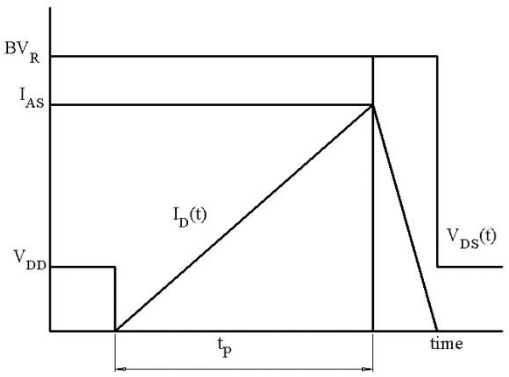
2. Switch Time Test Circuit



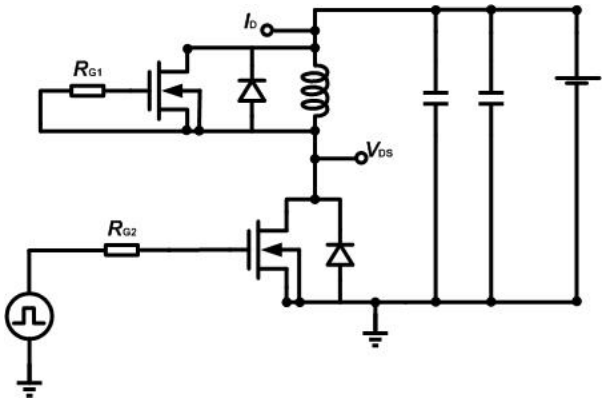


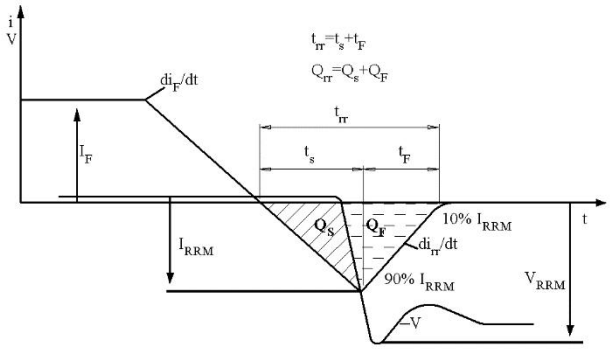
3. Unclamped Inductive Switching Test Circuit & Waveforms





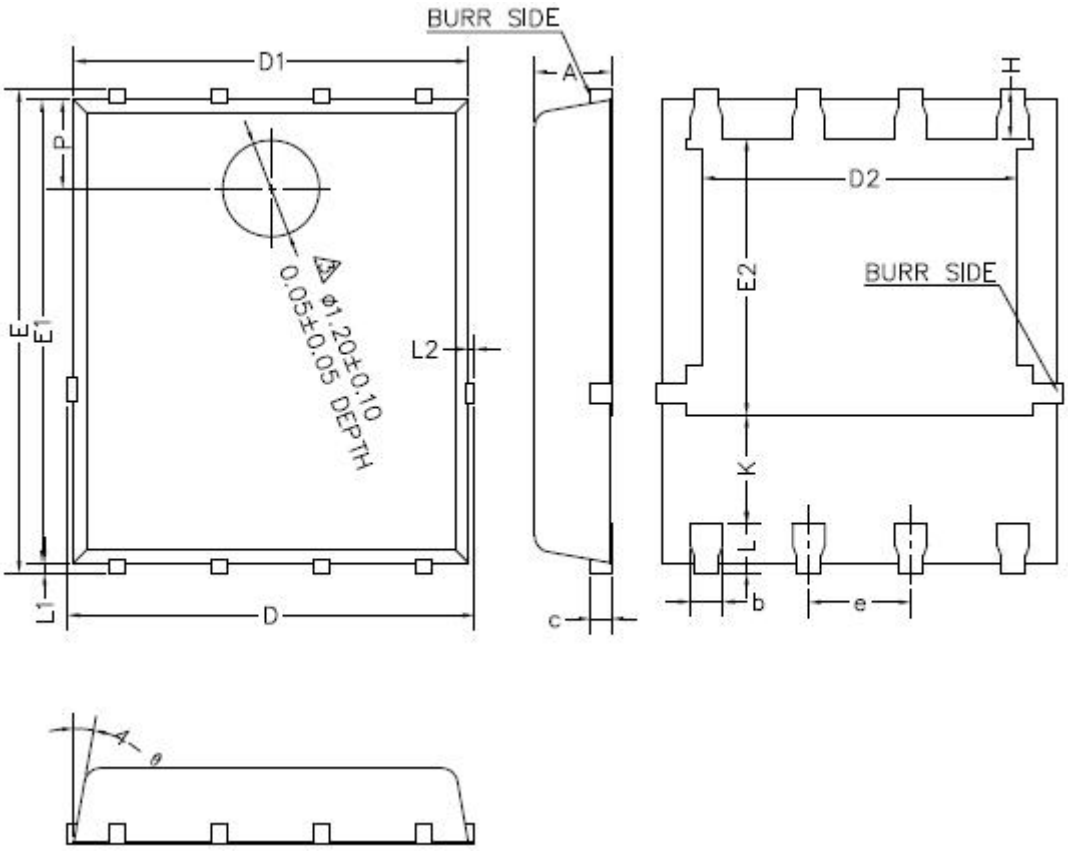
4. Test Circuit and Waveform for Diode Characteristics





Mechanical Dimension

PDFN5*6-8 **Unit: mm**



Symbol	Dimensions(mm)		
	Min.	Typ.	Max.
A	0.90	1.10	1.20
b	0.35	0.40	0.45
c	0.21	0.25	0.34
D			5.10
D1	4,80	4.90	5.00
D2	3.91	4.01	4.11
e	1.17	1.27	1.37
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.34	3.44	3.54
H	0.51	0.61	0.71
K	1.10		
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
L2			0.10
P	1.00	1.10	1.20
θ	8°	10°	12°

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Sanrise Technology Limited Company

http://www.sanrise-tech.com

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