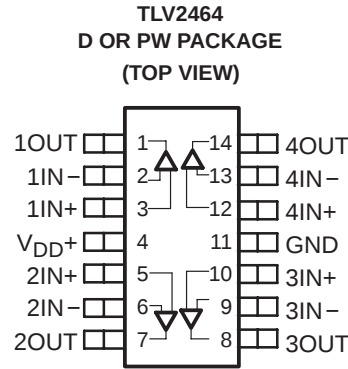
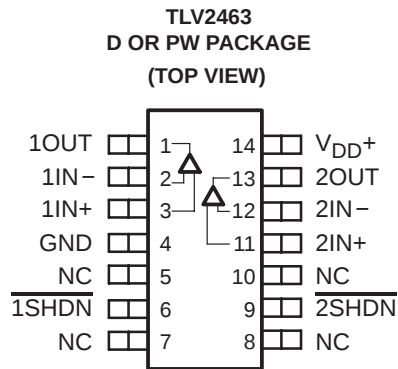
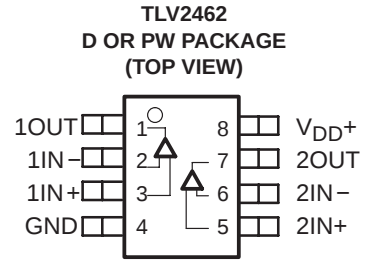
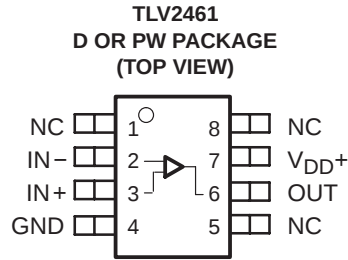
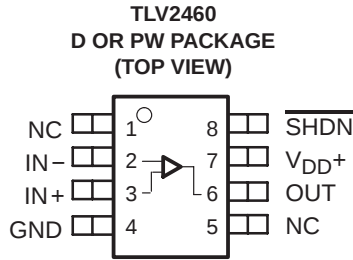


TLV246x-Q1, TLV246xA-Q1 LOW-POWER RAIL-TO-RAIL INPUT/OUTPUT OPERATIONAL AMPLIFIERS WITH SHUTDOWN

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- Qualified for Automotive Applications
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Rail-to-Rail Output Swing
- Gain Bandwidth Product . . . 6.4 MHz
- ± 80 -mA Output Drive Capability
- Supply Current . . . 500 μ A/Channel
- Input Offset Voltage . . . 100 μ V
- Input Noise Voltage . . . 11 nV/ $\sqrt{\text{Hz}}$
- Slew Rate . . . 1.6 V/ μ s
- Micropower Shutdown Mode (TLV2460/TLV2463) . . . 0.3 μ A/Channel
- Universal Operational Amplifier EVM



NC – No internal connection

description

The devices in the TLV246x family of low-power rail-to-rail input/output operational amplifiers are specifically designed for portable applications. The input common-mode voltage range extends beyond the supply rails for maximum dynamic range in low-voltage systems. The amplifier output has rail-to-rail performance with high-output-drive capability, solving one of the limitations of older rail-to-rail input/output operational amplifiers. This rail-to-rail dynamic range and high output drive make the TLV246x ideal for buffering analog-to-digital converters.

The operational amplifier has 6.4-MHz bandwidth and 1.6-V/ μ s slew rate with only 500- μ A supply current, providing good ac performance with low power consumption. Devices are available with an optional shutdown terminal, which places the amplifier in an ultralow supply-current mode ($I_{DD} = 0.3 \mu\text{A/channel}$). While in shutdown, the operational amplifier output is placed in a high-impedance state. DC applications are also well served with an input noise voltage of 11 nV/ $\sqrt{\text{Hz}}$ and input offset voltage of 100 μ V.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

UNLESS OTHERWISE NOTED this document contains PRODUCTION DATA information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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TLV246x-Q1, TLV246xA-Q1

LOW-POWER RAIL-TO-RAIL INPUT/OUTPUT OPERATIONAL AMPLIFIERS WITH SHUTDOWN

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ORDERING INFORMATION[†]

T _A	V _{IO} MAX AT 25°C	PACKAGE [‡]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 125°C	2000 μ V	SOP – D	Reel of 2500	TLV2460QDRQ1	2460Q1
		TSSOP – PW	Reel of 2000	TLV2460QPWRQ1	2460Q1
		SOP – D	Reel of 2500	TLV2461QDRQ1	2461Q1
		TSSOP – PW	Reel of 2000	TLV2461QPWRQ1	2461Q1
		SOP – D	Reel of 2500	TLV2462QDRQ1	2462Q1
		TSSOP – PW	Reel of 2000	TLV2462QPWRQ1	2462Q1
		SOP – D	Reel of 2500	TLV2463QDRQ1	TLV2463Q1
		TSSOP – PW	Reel of 2000	TLV2463QPWRQ1	2463Q1
		SOP – D	Reel of 2500	TLV2464QDRQ1 [§]	2464Q1
		TSSOP – PW	Reel of 2000	TLV2464QPWRQ1 [§]	2464Q1
	1500 μ V	SOP – D	Reel of 2500	TLV2460AQDRQ1	2460AQ
		TSSOP – PW	Reel of 2000	TLV2460AQPWRQ1	2460AQ
		SOP – D	Reel of 2500	TLV2461AQDRQ1	2461AQ
		TSSOP – PW	Reel of 2000	TLV2461AQPWRQ1	2461AQ
		SOP – D	Reel of 2500	TLV2462AQDRQ1	2462AQ
		TSSOP – PW	Reel of 2000	TLV2462AQPWRQ1	2462AQ
		SOP – D	Reel of 2500	TLV2463AQDRQ1	TLV2463AQ1
		TSSOP – PW	Reel of 2000	TLV2463AQPWRQ1	V2463AQ
		SOP – D	Reel of 2500	TLV2464AQDRQ1 [§]	V2464AQ
		TSSOP – PW	Reel of 2000	TLV2464AQPWRQ1	V2464AQ

[†] For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

[‡] Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

[§] Product preview



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TLV246x-Q1, TLV246xA-Q1

LOW-POWER RAIL-TO-RAIL INPUT/OUTPUT OPERATIONAL AMPLIFIERS WITH SHUTDOWN

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage [‡] , V_{DD}	6 V
Differential input voltage range, V_{ID}	-0.2 V to $V_{DD} + 0.2$ V
Input current, I_I (any input)	± 200 mA
Output current, I_O	± 175 mA
Total input current, I_I (into V_{DD+})	175 mA
Total output current, I_O (out of GND)	175 mA
Operating free-air temperature range, T_A	-40°C to 125°C
Maximum junction temperature, T_J	150°C
Thermal impedance, junction to ambient [§] , θ_{JA} : D (8 pin)	176°C/W
D (14 pin)	123°C/W
PW (8 pin)	259°C/W
PW (14 pin)	174°C/W
Storage temperature range, T_{stg}	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

[‡] All voltage values, except differential voltages, are with respect to GND.

[§] Package thermal impedance is calculated in accordance with JESD 51-5.

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}	Single supply	2.7	6	V
	Split supply	± 1.35	± 3	
Common-mode input voltage range, V_{ICR}		-0.2	$V_{DD} + 0.2$	V
Operating free-air temperature, T_A		-40	125	°C
Shutdown on/off voltage level [†]	V_{IH}	2		V
	V_{IL}		0.7	

[†] Relative to voltage on the GND terminal of the device



TLV246x-Q1, TLV246xA-Q1

LOW-POWER RAIL-TO-RAIL INPUT/OUTPUT OPERATIONAL AMPLIFIERS WITH SHUTDOWN

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electrical characteristics at specified free-air temperature, $V_{DD} = 3\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	$T_A^\dagger$	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{DD} = 3\text{ V}$, $V_{IC} = 1.5\text{ V}$, $V_O = 1.5\text{ V}$, $R_S = 50\ \Omega$	TLV246x	25°C	100	2000	μV
				Full range		2200	
		TLV246xA	25°C		150	1500	
				Full range		1700	
α_{VIO}	Temperature coefficient of input offset voltage	$V_{DD} = 3\text{ V}$, $V_{IC} = 1.5\text{ V}$, $V_O = 1.5\text{ V}$, $R_S = 50\ \Omega$			2		$\mu\text{V}/^\circ\text{C}$
I_{IO}	Input offset current	$V_{DD} = 3\text{ V}$, $V_{IC} = 1.5\text{ V}$, $V_O = 1.5\text{ V}$, $R_S = 50\ \Omega$	25°C		2.8	7	nA
				Full range		75	
I_{IB}	Input bias current	$V_{DD} = 3\text{ V}$, $V_{IC} = 1.5\text{ V}$, $V_O = 1.5\text{ V}$, $R_S = 50\ \Omega$	25°C		4.4	14	nA
				Full range		75	
V_{OH}	High-level output voltage	$I_{OH} = -2.5\text{ mA}$	25°C		2.9		V
				Full range	2.8		
		$I_{OH} = -10\text{ mA}$	25°C		2.7		
				Full range	2.5		
V_{OL}	Low-level output voltage	$V_{IC} = 1.5\text{ V}$, $I_{OL} = 2.5\text{ mA}$	25°C		0.1		V
				Full range		0.2	
		$V_{IC} = 1.5\text{ V}$, $I_{OL} = 10\text{ mA}$	25°C		0.3		
				Full range		0.5	
I_{OS}	Short-circuit output current	Sourcing	25°C		50		mA
				Full range	20		
		Sinking	25°C		40		
				Full range	20		
I_O	Output current	Measured 1 V from rail	25°C		± 40		mA
A_{VD}	Large-signal differential voltage amplification	$R_L = 10\text{ k}\Omega$	25°C		90	105	dB
				Full range	89		
$r_{i(d)}$	Differential input resistance		25°C		10^9		Ω
$C_{i(c)}$	Common-mode input capacitance	$f = 10\text{ kHz}$	25°C		7		pF
z_O	Closed-loop output impedance	$f = 100\text{ kHz}$, $A_V = 10$	25°C		33		Ω
CMRR	Common-mode rejection ratio	$V_{ICR} = 0\text{ V to } 3\text{ V}$, $R_S = 50\ \Omega$	25°C		66	80	dB
				Full range	60		
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 2.7\text{ V to } 6\text{ V}$, $V_{IC} = V_{DD}/2$, No load	25°C		80	85	dB
				Full range	75		
		$V_{DD} = 3\text{ V to } 5\text{ V}$, $V_{IC} = V_{DD}/2$, No load	25°C		85	95	
				Full range	80		
I_{DD}	Supply current (per channels)	$V_O = 1.5\text{ V}$, No load	25°C		0.5	0.575	mA
				Full range		0.9	
$I_{DD(SHDN)}$	Supply current in shutdown (TLV2460, TLV2463)	SHDN < 0.7 V, Per channel in shutdown	25°C		0.3		μA
				Full range		2.5	

† Full range is -40°C to 125°C .

TLV246x-Q1, TLV246xA-Q1

LOW-POWER RAIL-TO-RAIL INPUT/OUTPUT OPERATIONAL AMPLIFIERS WITH SHUTDOWN

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operating characteristics at specified free-air temperature, $V_{DD} = 3\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T _A [†]	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	V _{O(PP)} = 2 V, C _L = 160 pF, R _L = 10 kΩ		25°C	1	1.6		V/μs
				Full range	0.8			
V _n	Equivalent input noise voltage	f = 100 Hz		25°C	16			nV/√Hz
		f = 1 kHz			11			
I _n	Equivalent input noise current	f = 1 kHz		25°C	0.13			pA/√Hz
THD+N	Total harmonic distortion plus noise	V _{O(PP)} = 2 V, R _L = 10 kΩ, f = 1 kHz	A _V = 1	25°C	0.006			%
			A _V = 10		0.02			
			A _V = 100		0.08			
t _(on)	Amplifier turnon time	A _V = 1, R _L = 10 kΩ	Both channels	25°C	7.6			μs
			Channel 1 only, Channel 2 on		7.65			
t _(off)	Amplifier turnoff time	A _V = 1, R _L = 10 kΩ	Both channels	25°C	333			ns
			Channel 1 only, Channel 2 on		328			
			Channel 2 only, Channel 1 on		329			
Gain-bandwidth product		f = 10 kHz, C _L = 160 pF	R _L = 10 kΩ,	25°C	5.2			MHz
t _s	Settling time	V _{(STEP)PP} = 2 V, A _V = -1, C _L = 10 pF, R _L = 10 kΩ	0.1%	25°C	1.47			μs
			0.01%		1.78			
		V _{(STEP)PP} = 2 V, A _V = -1, C _L = 56 pF, R _L = 10 kΩ	0.1%		1.77			
			0.01%		1.98			
φ _m	Phase margin at unity gain	R _L = 10 kΩ, C _L = 160 pF		25°C	44			°
Gain margin		R _L = 10 kΩ, C _L = 160 pF		25°C	7			dB

† Full range is -40°C to 125°C .



TLV246x-Q1, TLV246xA-Q1

LOW-POWER RAIL-TO-RAIL INPUT/OUTPUT OPERATIONAL AMPLIFIERS WITH SHUTDOWN

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electrical characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	$T_A^\dagger$	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{DD} = 5\text{ V}$, $V_{IC} = 2.5\text{ V}$, $V_O = 2.5\text{ V}$, $R_S = 50\ \Omega$	TLV246x	25°C	150	2000	μV
				Full range		2200	
		TLV246xA	25°C		150	1500	
				Full range		1700	
α_{VIO}	Temperature coefficient of input offset voltage	$V_{DD} = 5\text{ V}$, $V_{IC} = 2.5\text{ V}$, $V_O = 2.5\text{ V}$, $R_S = 50\ \Omega$			2		$\mu\text{V}/^\circ\text{C}$
I_{IO}	Input offset current	$V_{DD} = 5\text{ V}$, $V_{IC} = 2.5\text{ V}$, $V_O = 2.5\text{ V}$, $R_S = 50\ \Omega$	25°C		0.3	7	nA
				Full range		60	
I_{IB}	Input bias current	$V_{DD} = 5\text{ V}$, $V_{IC} = 2.5\text{ V}$, $V_O = 2.5\text{ V}$, $R_S = 50\ \Omega$	25°C		1.3	14	nA
				Full range		60	
V_{OH}	High-level output voltage	$I_{OH} = -2.5\text{ mA}$	25°C		4.9		V
				Full range	4.8		
		$I_{OH} = -10\text{ mA}$	25°C		4.8		
				Full range	4.7		
V_{OL}	Low-level output voltage	$V_{IC} = 2.5\text{ V}$, $I_{OL} = 2.5\text{ mA}$	25°C		0.1		V
				Full range		0.2	
		$V_{IC} = 2.5\text{ V}$, $I_{OL} = 10\text{ mA}$	25°C		0.2		
				Full range		0.3	
I_{OS}	Short-circuit output current	Sourcing	25°C		145		mA
				Full range	60		
		Sinking	25°C		100		
				Full range	60		
I_O	Output current	Measured at 1 V from rail	25°C		± 80		mA
A_{VD}	Large-signal differential voltage amplification	$V_{IC} = 2.5\text{ V}$, $R_L = 10\text{ k}\Omega$, $V_O = 1\text{ V to }4\text{ V}$	25°C		92	109	dB
				Full range	90		
$r_{i(d)}$	Differential input resistance		25°C		10^9		Ω
$C_{i(c)}$	Common-mode input capacitance	$f = 10\text{ kHz}$	25°C		7		pF
z_O	Closed-loop output impedance	$f = 100\text{ kHz}$, $A_V = 10$	25°C		29		Ω
CMRR	Common-mode rejection ratio	$V_{ICR} = 0\text{ V to }5\text{ V}$, $R_S = 50\ \Omega$	25°C		71	85	dB
				Full range	60		
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 2.7\text{ V to }6\text{ V}$, $V_{IC} = V_{DD}/2$, No load	25°C		80	85	dB
				Full range	75		
		$V_{DD} = 3\text{ V to }5\text{ V}$, $V_{IC} = V_{DD}/2$, No load	25°C		85	95	dB
				Full range	80		
I_{DD}	Supply current (per channel)	$V_O = 2.5\text{ V}$, No load	25°C		0.55	0.65	mA
				Full range		1	
$I_{DD(SHDN)}$	Supply current in shutdown (TLV2460, TLV2463)	$\overline{\text{SHDN}} < 0.7\text{ V}$, Per channel in shutdown	25°C		1		μA
				Full range		3	

† Full range is -40°C to 125°C .

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operating characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T _A [†]	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	V _{O(PP)} = 2 V, R _L = 10 kΩ		C _L = 160 pF,	25°C	1	1.6	V/μs
					Full range	0.8		
V _n	Equivalent input noise voltage	f = 100 Hz		25°C	14			nV/√Hz
		f = 1 kHz			11			
I _n	Equivalent input noise current	f = 100 Hz		25°C	0.13			pA/√Hz
THD+N	Total harmonic distortion plus noise	V _{O(PP)} = 4 V, R _L = 10 kΩ, f = 10 kHz	A _V = 1	25°C	0.004			%
			A _V = 10		0.01			
			A _V = 100		0.04			
t _(on)	Amplifier turnon time	A _V = 1, R _L = 10 kΩ	Both channels	25°C	7.6			μs
			Channel 1 only, Channel 2 on		7.65			
			Channel 2 only, Channel 1 on		7.25			
t _(off)	Amplifier turnoff time	A _V = 1, R _L = 10 kΩ	Both channels	25°C	333			ns
			Channel 1 only, Channel 2 on		328			
			Channel 2 only, Channel 1 on		329			
Gain-bandwidth product		f = 10 kHz, C _L = 160 pF	R _L = 10 kΩ,	25°C	6.4			MHz
t _s	Settling time	V(STEP)PP = 2 V, A _V = -1, C _L = 10 pF, R _L = 10 kΩ	0.1%	25°C	1.53			μs
			0.01%		1.83			
		V(STEP)PP = 2 V, A _V = -1, C _L = 56 pF, R _L = 10 kΩ	0.1%		3.13			
			0.01%		3.33			
φ _m	Phase margin at unity gain	R _L = 10 kΩ, C _L = 160 pF		25°C	45			°
Gain margin		R _L = 10 kΩ, C _L = 160 pF		25°C	7			dB

† Full range is -40°C to 125°C .

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TYPICAL CHARACTERISTICS

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V_{OL}	Low-level output voltage	vs Low-level output current	7, 8
$V_{O(PP)}$	Peak-to-peak output voltage	vs Frequency	9, 10
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	Phase	vs Frequency	11, 12
A_{VD}	Differential voltage amplification	vs Load resistance	13
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Z_o	Output impedance	vs Frequency	15, 16
CMRR	Common-mode rejection ratio	vs Frequency	17
k_{SVR}	Supply-voltage rejection ratio	vs Frequency	18, 19
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SR	Slew rate	vs Supply voltage	27
V_n	Equivalent input noise voltage	vs Frequency	28, 29
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THD+N	Total harmonic distortion plus noise	vs Peak-to-peak signal amplitude	34, 35
ϕ_m	Phase margin	vs Frequency	11, 12
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TYPICAL CHARACTERISTICS

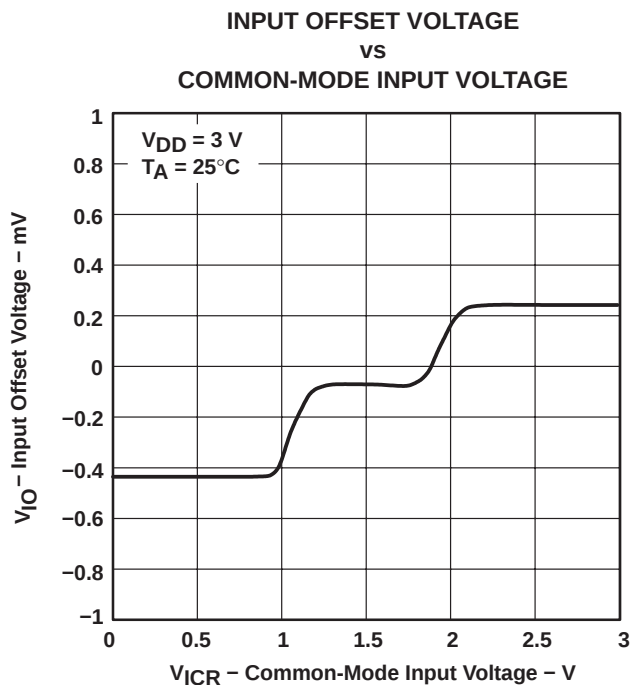


Figure 1

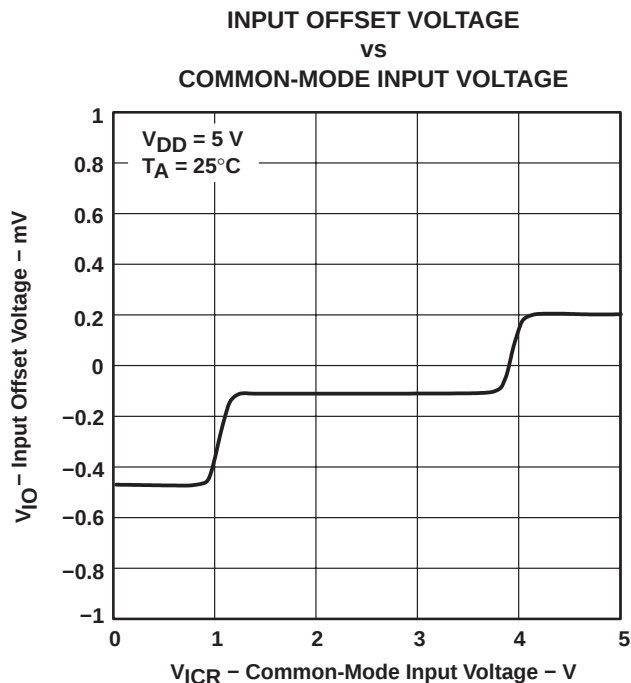


Figure 2

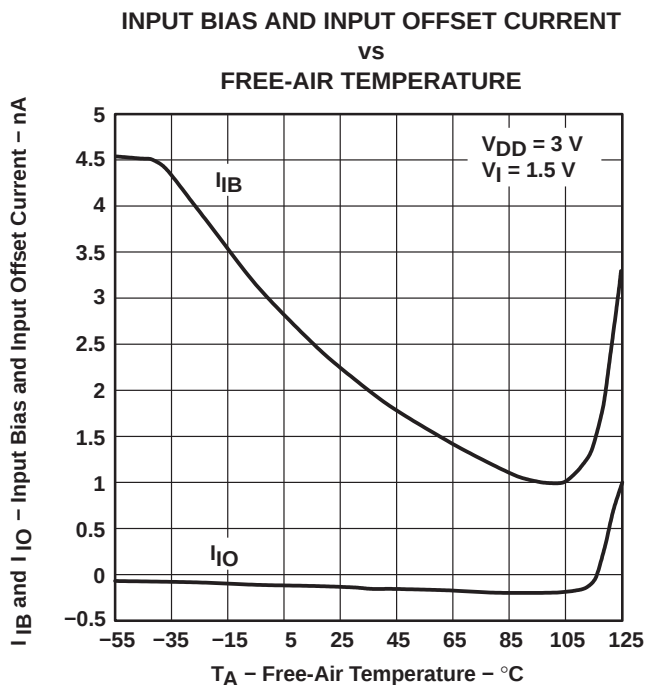


Figure 3

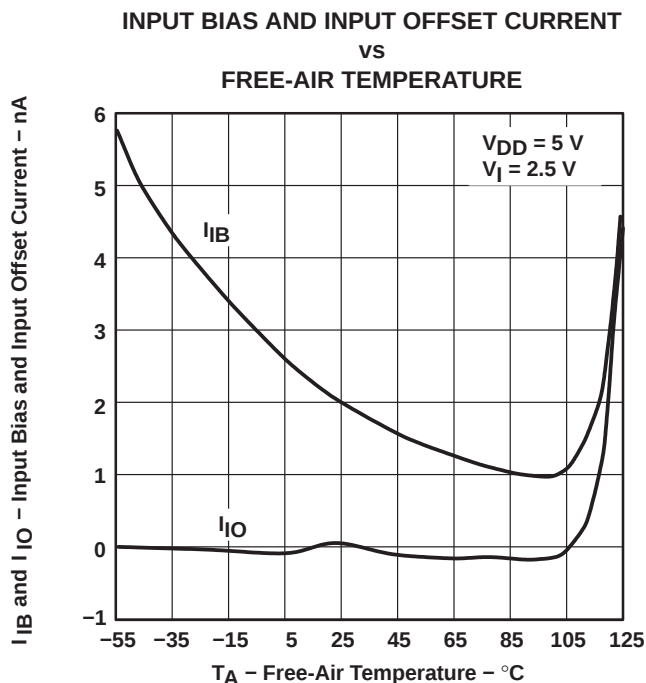


Figure 4

TLV246x-Q1, TLV246xA-Q1

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TYPICAL CHARACTERISTICS

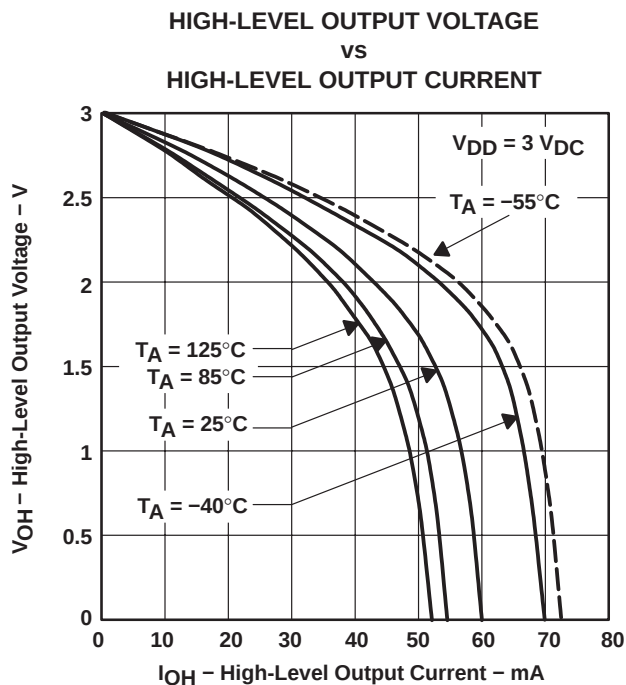


Figure 5

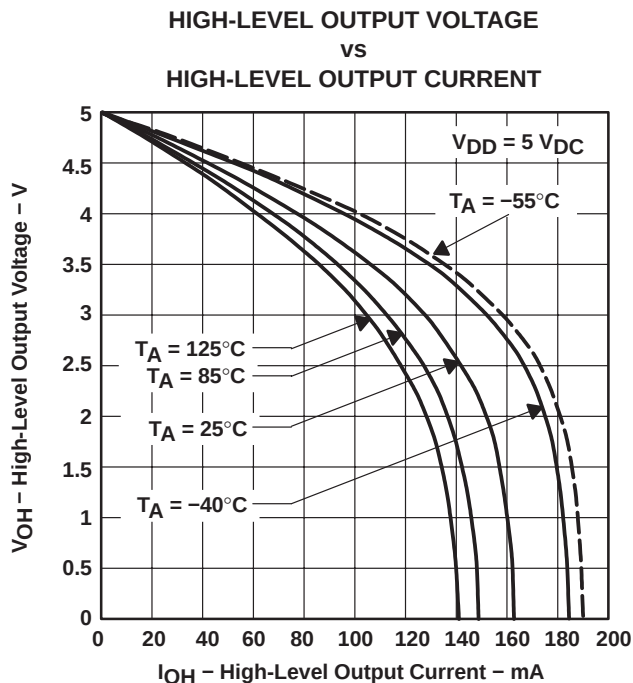


Figure 6

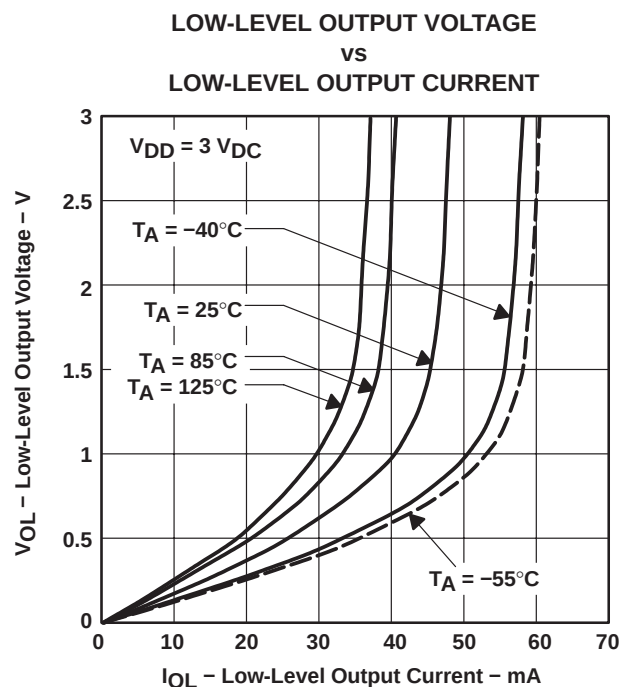


Figure 7

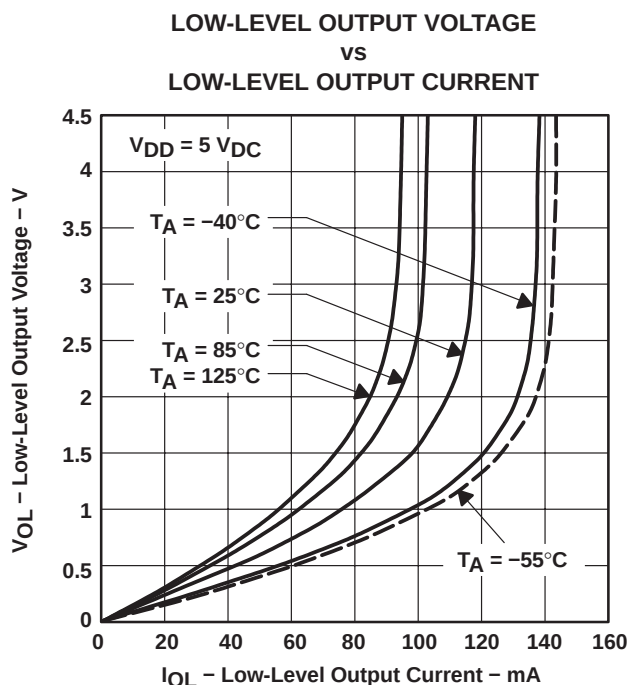


Figure 8

TLV246x-Q1, TLV246xA-Q1

LOW-POWER RAIL-TO-RAIL INPUT/OUTPUT OPERATIONAL AMPLIFIERS WITH SHUTDOWN

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TYPICAL CHARACTERISTICS

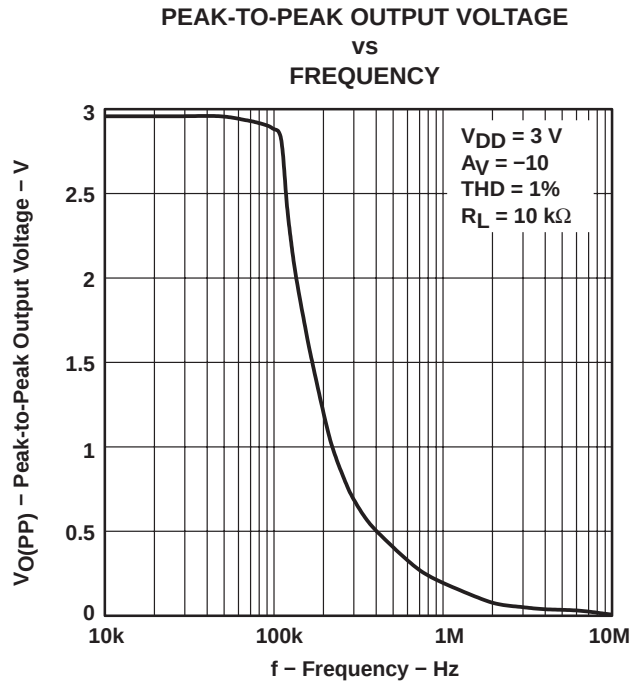


Figure 9

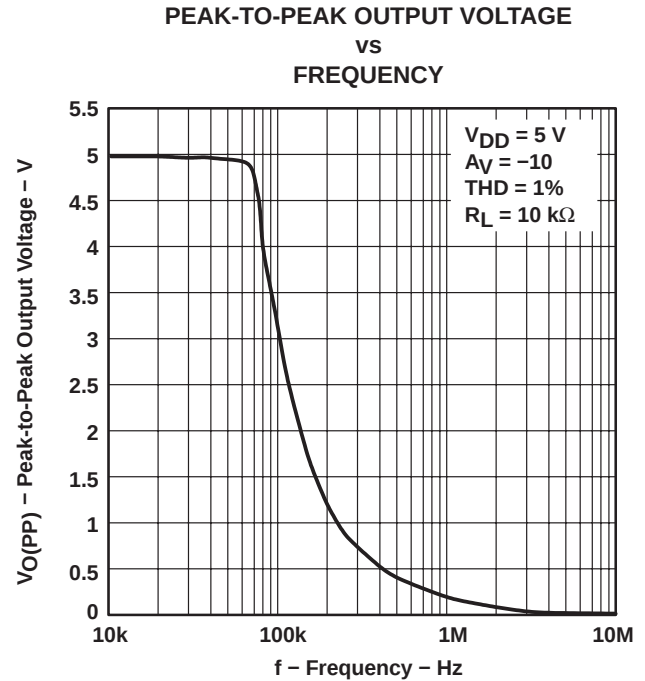


Figure 10

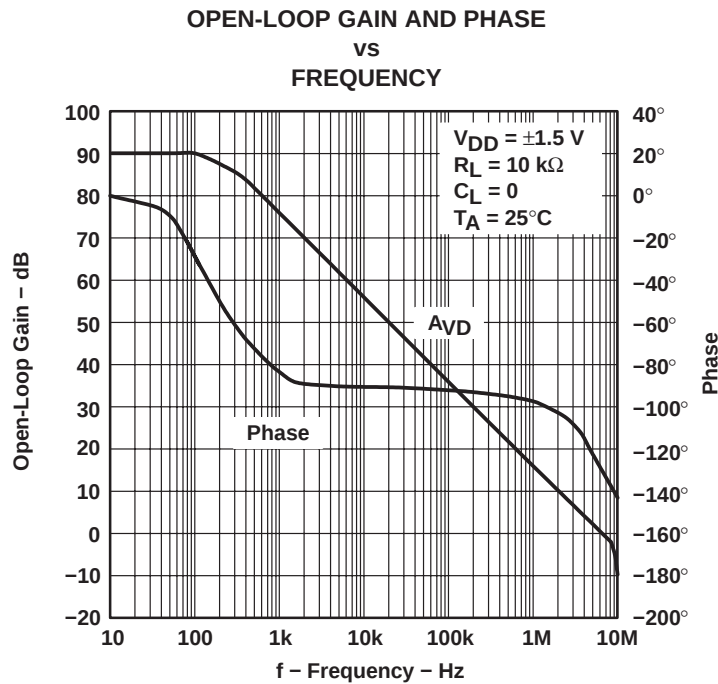


Figure 11

TLV246x-Q1, TLV246xA-Q1

LOW-POWER RAIL-TO-RAIL INPUT/OUTPUT OPERATIONAL AMPLIFIERS WITH SHUTDOWN

SGLS008C – MARCH 2003 – REVISED OCTOBER 2007

TYPICAL CHARACTERISTICS

OPEN-LOOP GAIN AND PHASE VS FREQUENCY

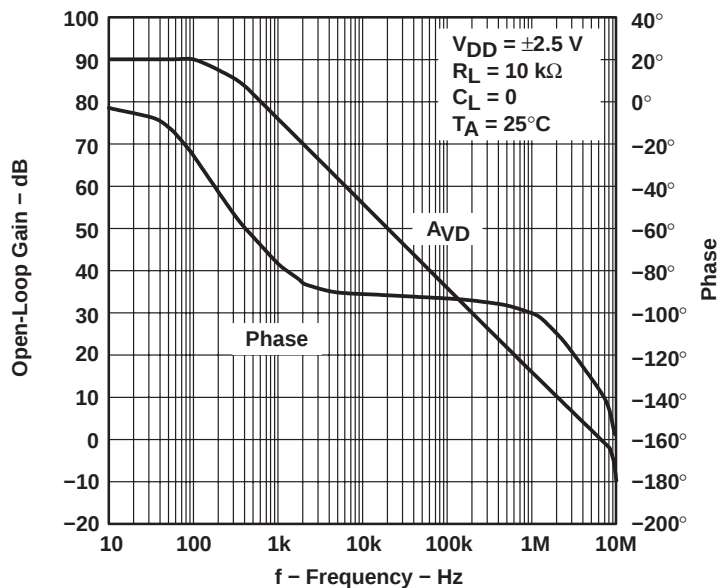


Figure 12

DIFFERENTIAL VOLTAGE AMPLIFICATION VS LOAD RESISTANCE

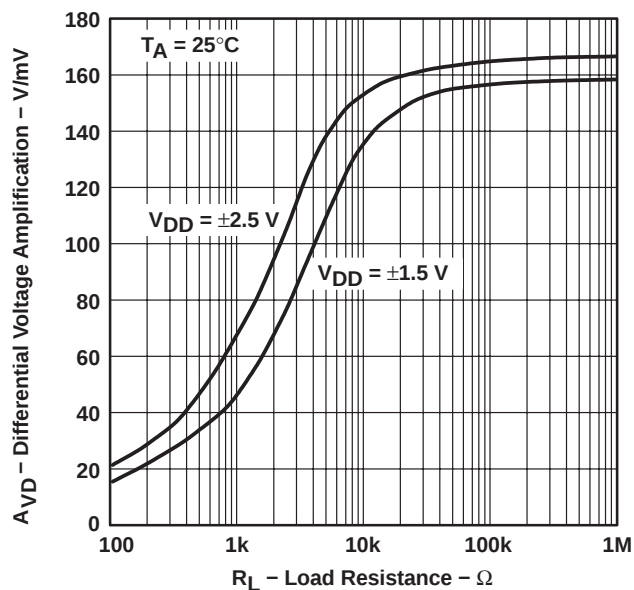


Figure 13

CAPACITIVE LOAD VS LOAD RESISTANCE

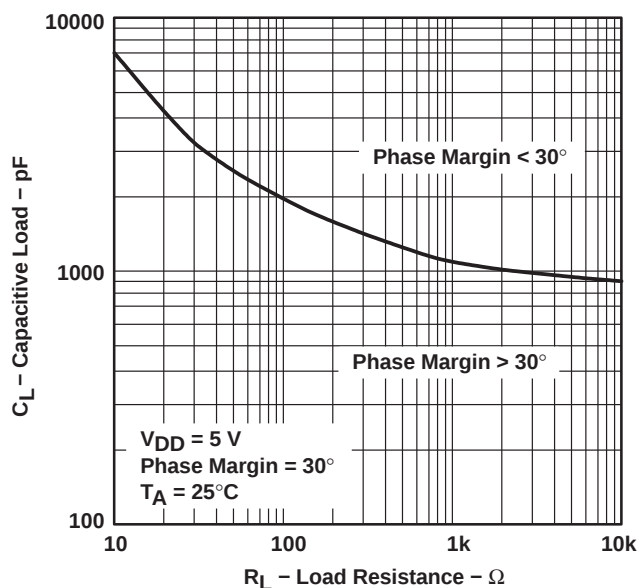


Figure 14

TLV246x-Q1, TLV246xA-Q1

LOW-POWER RAIL-TO-RAIL INPUT/OUTPUT OPERATIONAL AMPLIFIERS WITH SHUTDOWN

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TYPICAL CHARACTERISTICS

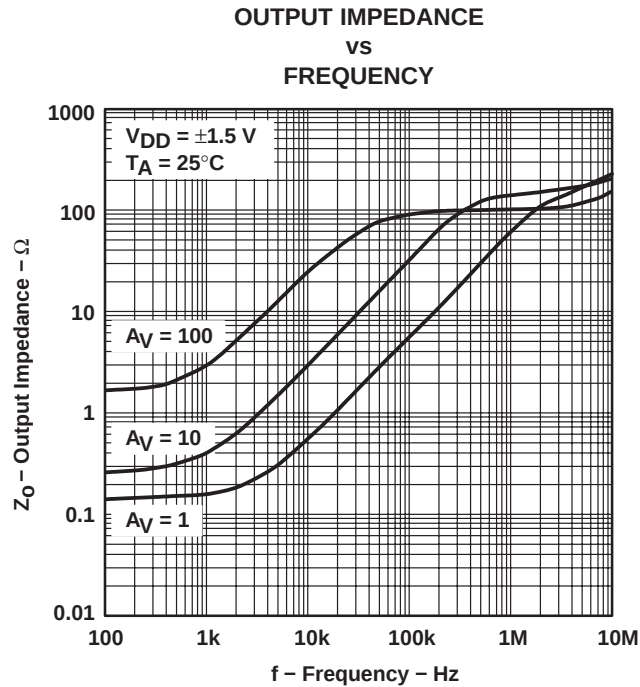


Figure 15

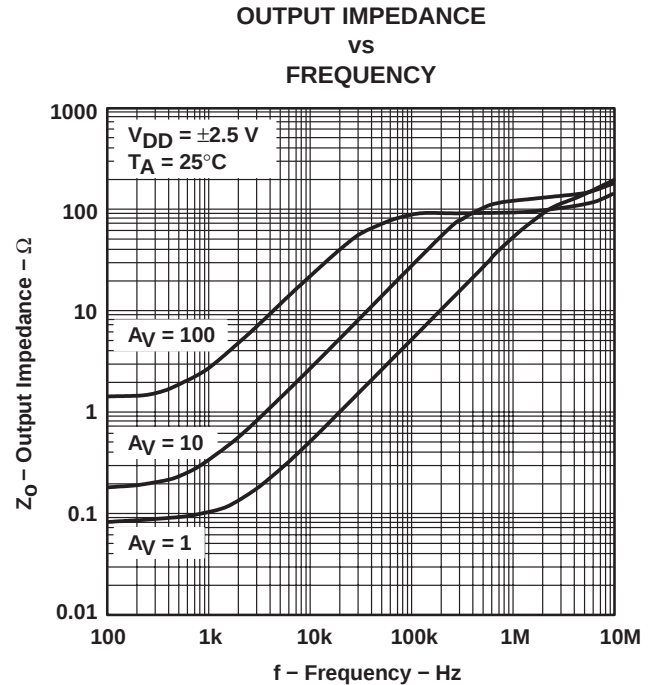


Figure 16

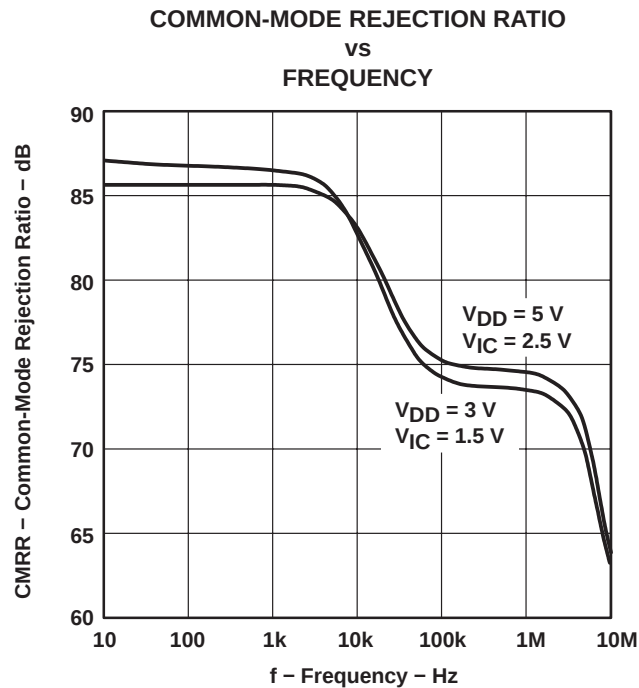


Figure 17

TLV246x-Q1, TLV246xA-Q1

LOW-POWER RAIL-TO-RAIL INPUT/OUTPUT OPERATIONAL AMPLIFIERS WITH SHUTDOWN

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TYPICAL CHARACTERISTICS

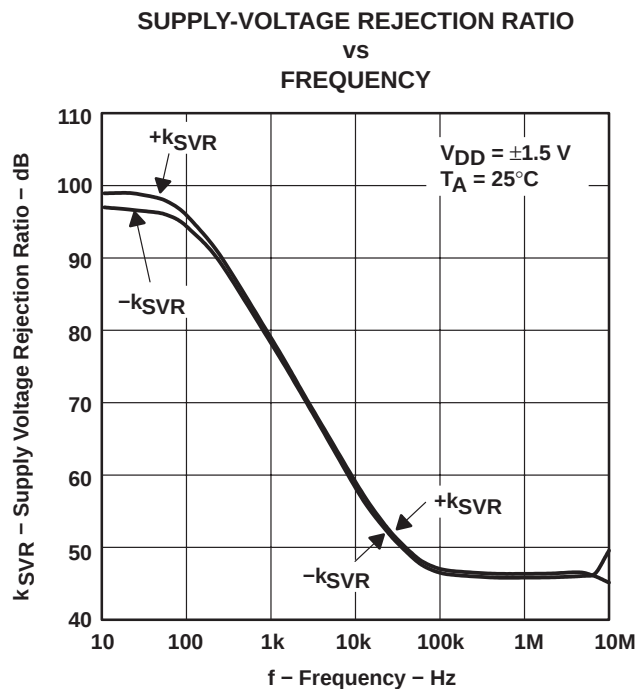


Figure 18

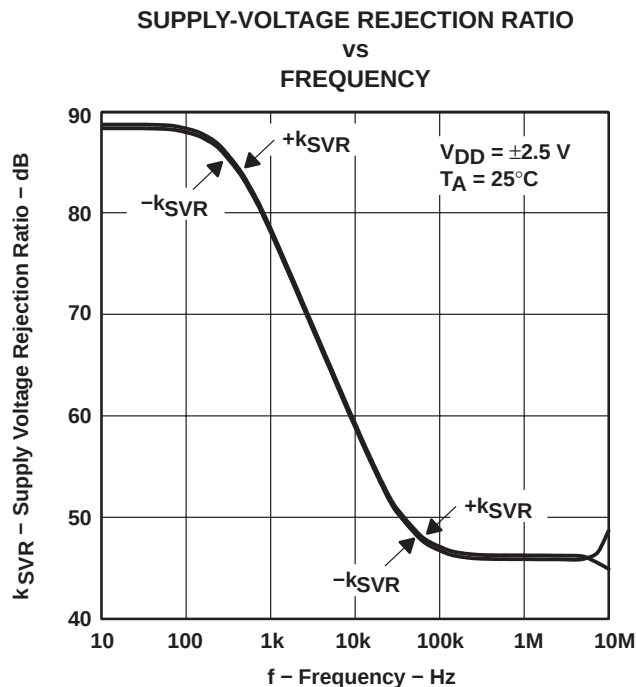


Figure 19

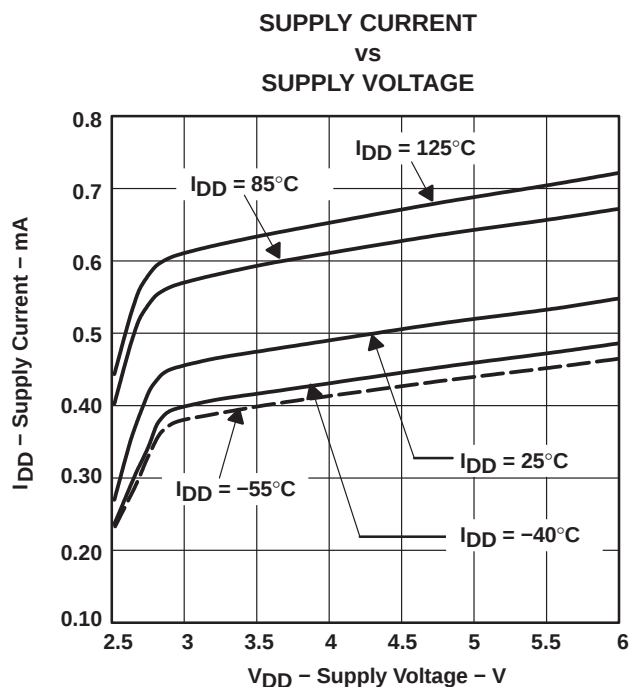


Figure 20

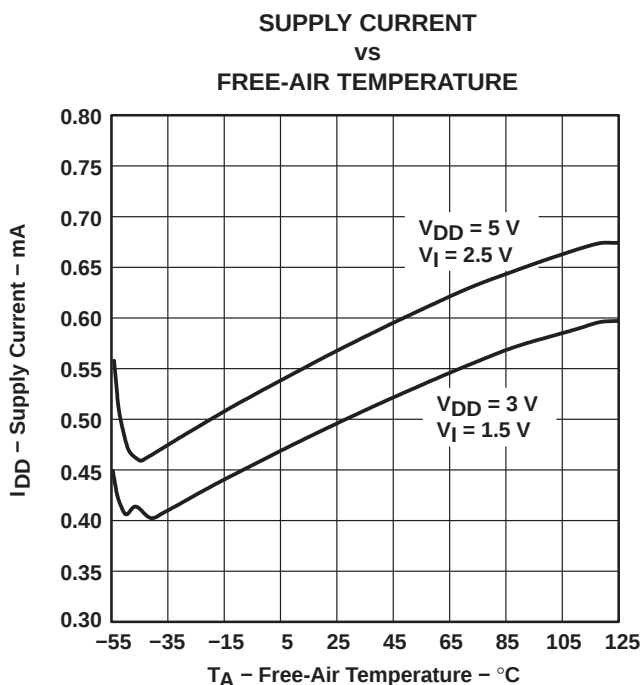


Figure 21

TLV246x-Q1, TLV246xA-Q1

LOW-POWER RAIL-TO-RAIL INPUT/OUTPUT OPERATIONAL AMPLIFIERS WITH SHUTDOWN

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TYPICAL CHARACTERISTICS

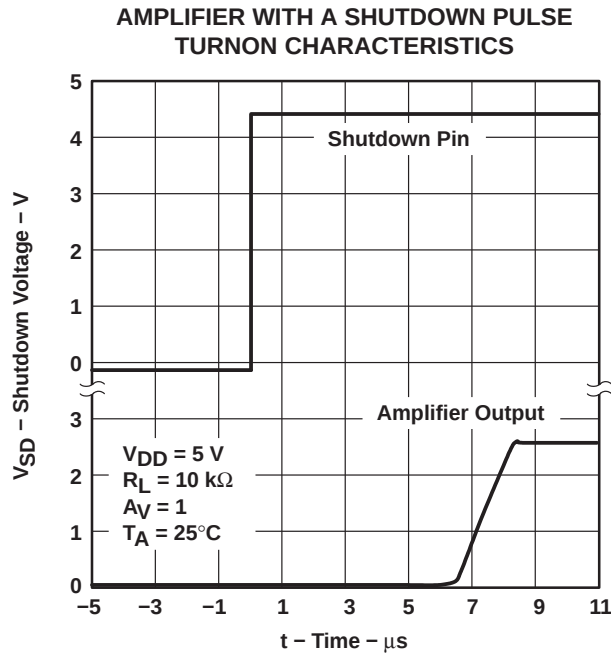


Figure 22

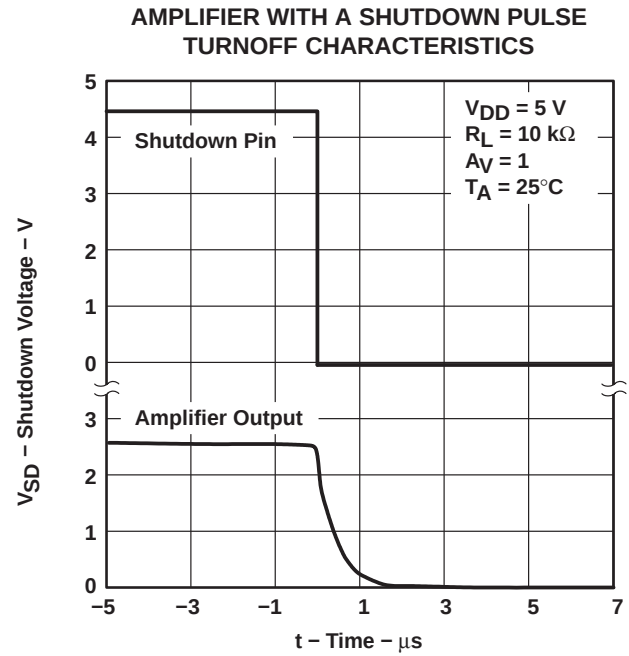


Figure 23

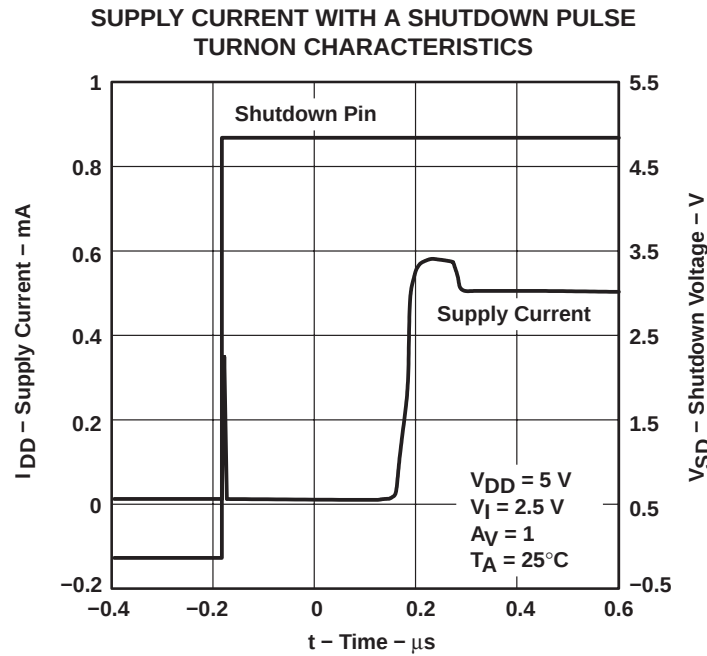


Figure 24

TLV246x-Q1, TLV246xA-Q1

LOW-POWER RAIL-TO-RAIL INPUT/OUTPUT OPERATIONAL AMPLIFIERS WITH SHUTDOWN

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TYPICAL CHARACTERISTICS

TURN-OFF SUPPLY CURRENT WITH A SHUTDOWN PULSE

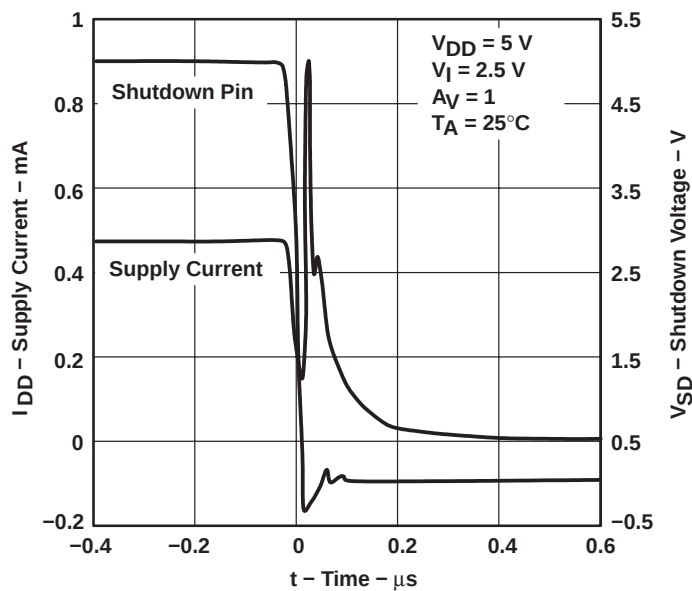


Figure 25

SHUTDOWN SUPPLY CURRENT VS FREE-AIR TEMPERATURE

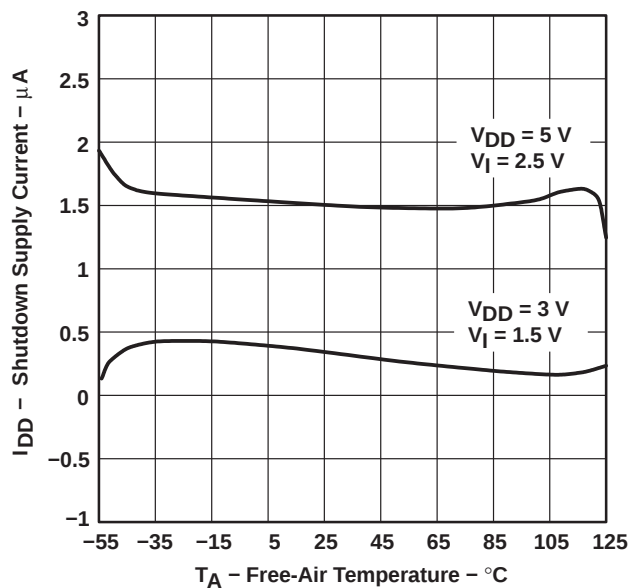


Figure 26

SLEW RATE VS SUPPLY VOLTAGE

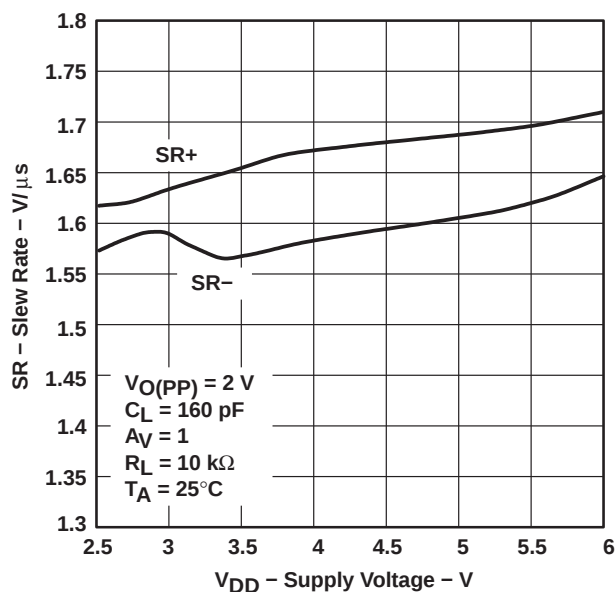


Figure 27

TLV246x-Q1, TLV246xA-Q1

LOW-POWER RAIL-TO-RAIL INPUT/OUTPUT OPERATIONAL AMPLIFIERS WITH SHUTDOWN

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TYPICAL CHARACTERISTICS

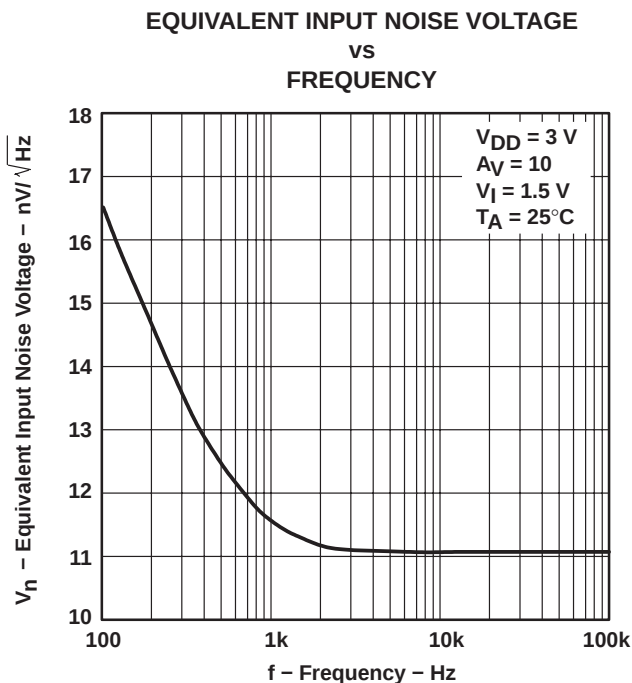


Figure 28

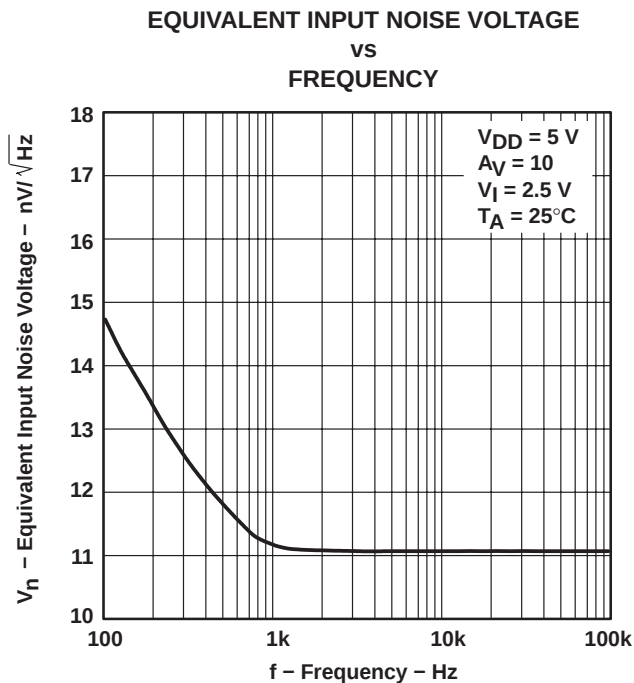


Figure 29

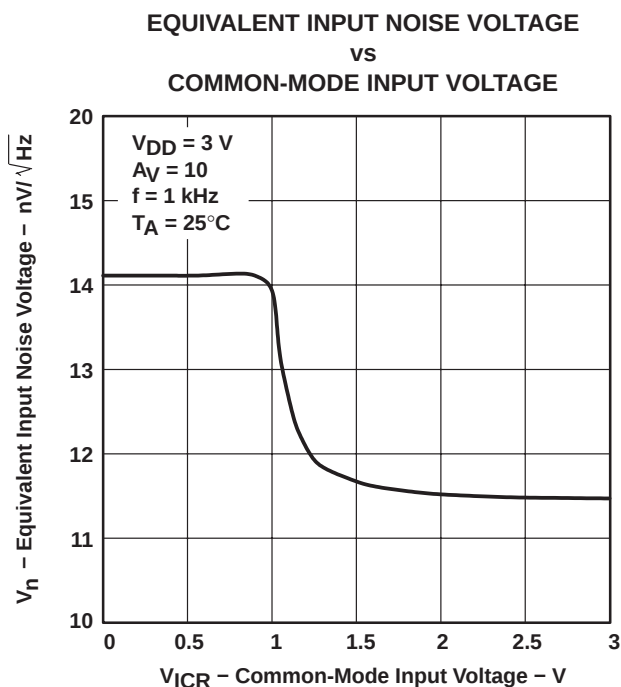


Figure 30

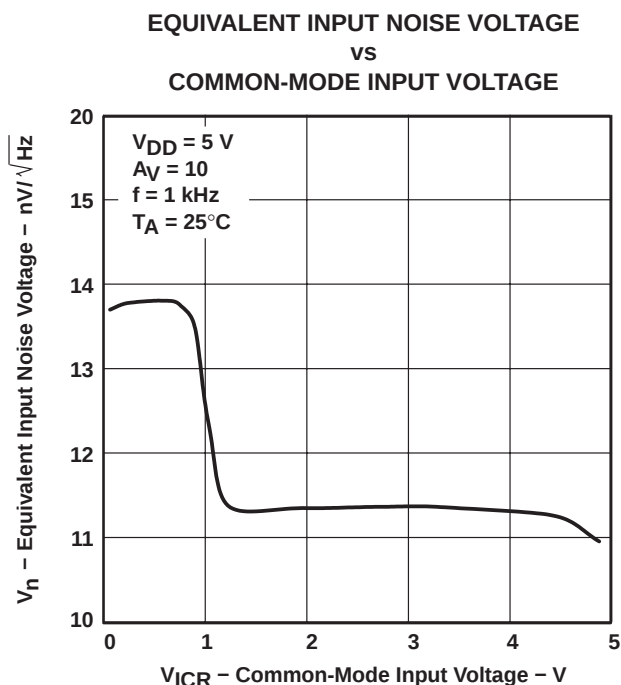


Figure 31

TLV246x-Q1, TLV246xA-Q1

LOW-POWER RAIL-TO-RAIL INPUT/OUTPUT OPERATIONAL AMPLIFIERS WITH SHUTDOWN

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TYPICAL CHARACTERISTICS

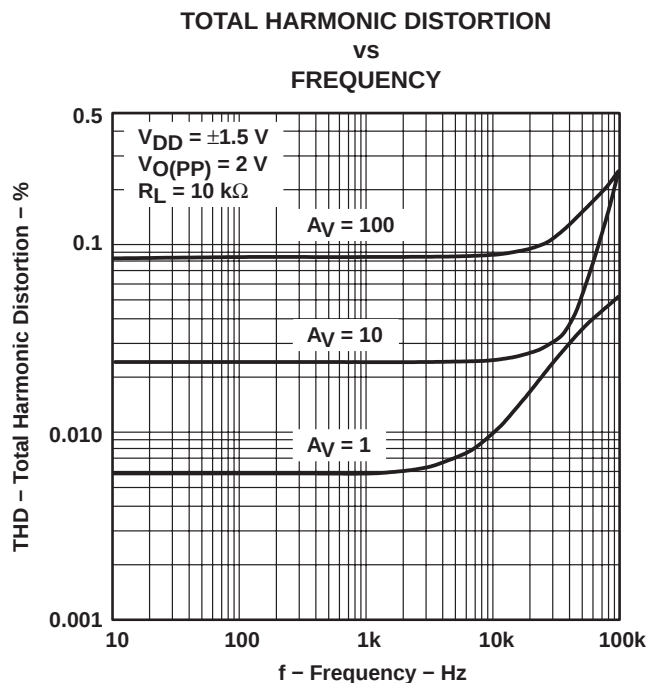


Figure 32

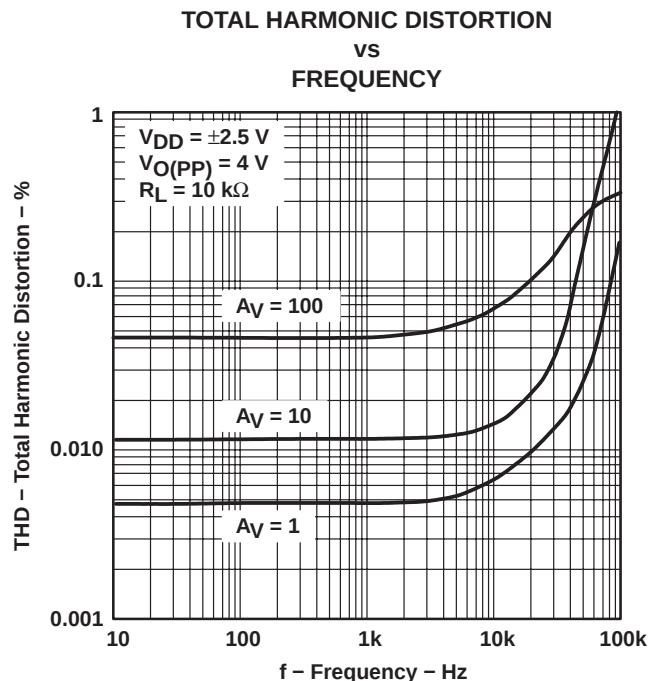


Figure 33

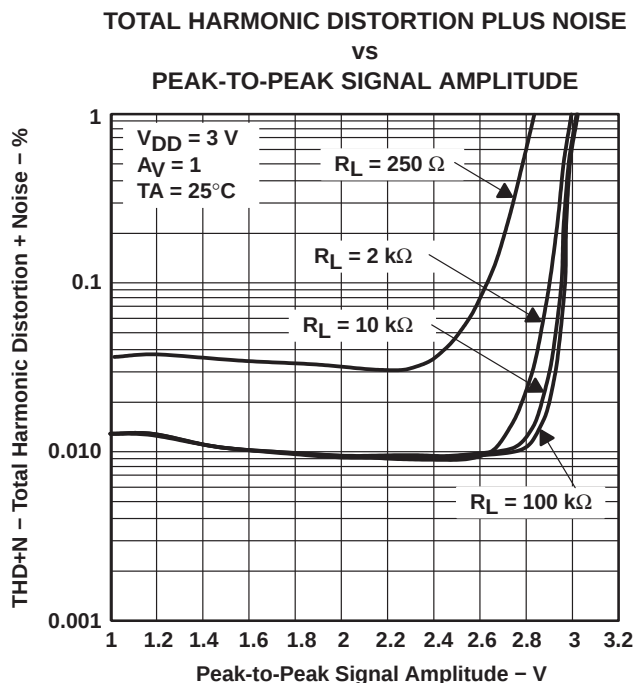


Figure 34

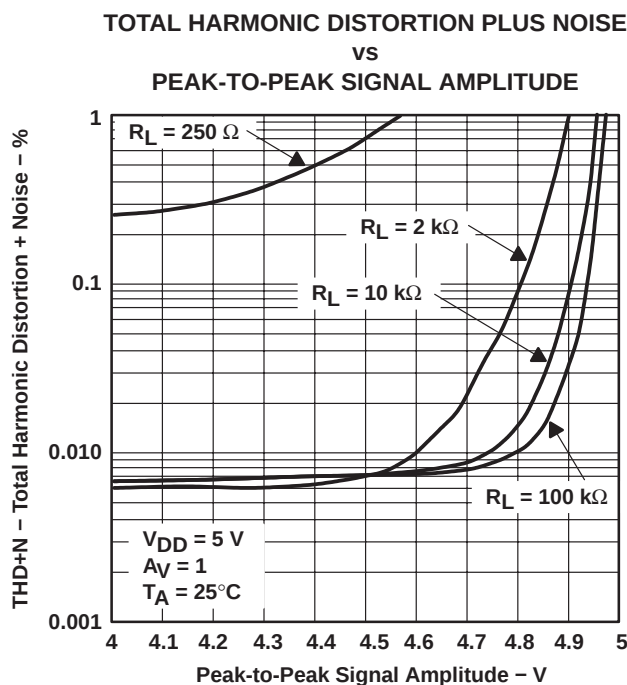


Figure 35

TLV246x-Q1, TLV246xA-Q1

LOW-POWER RAIL-TO-RAIL INPUT/OUTPUT OPERATIONAL AMPLIFIERS WITH SHUTDOWN

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TYPICAL CHARACTERISTICS

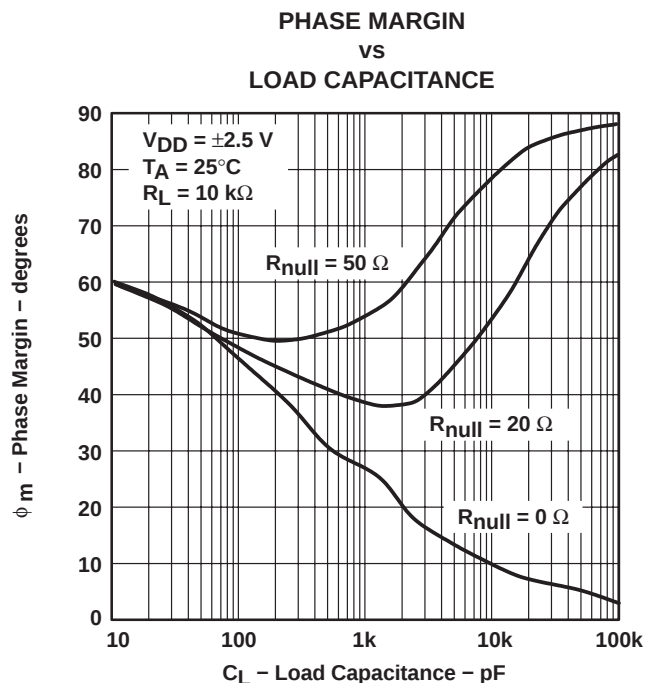


Figure 36

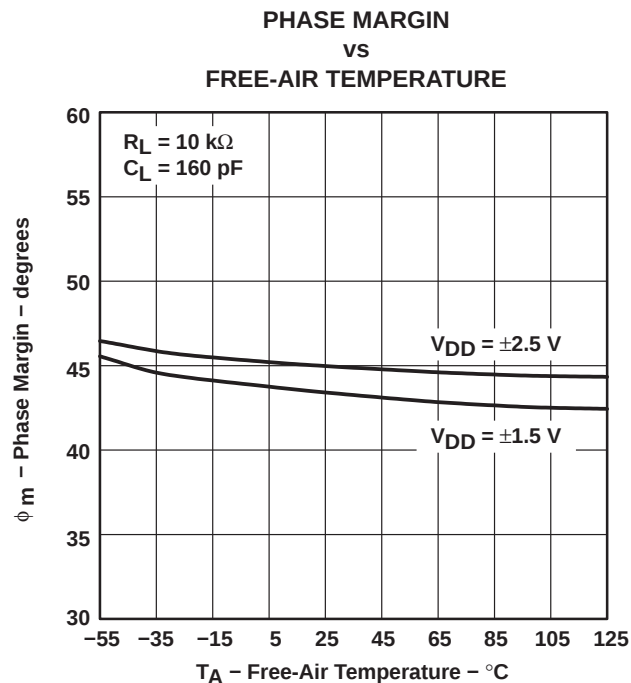


Figure 37

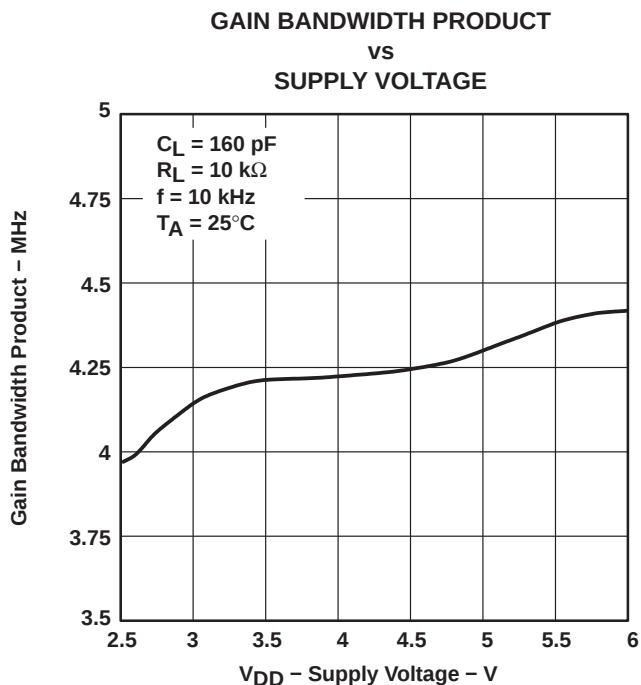


Figure 38

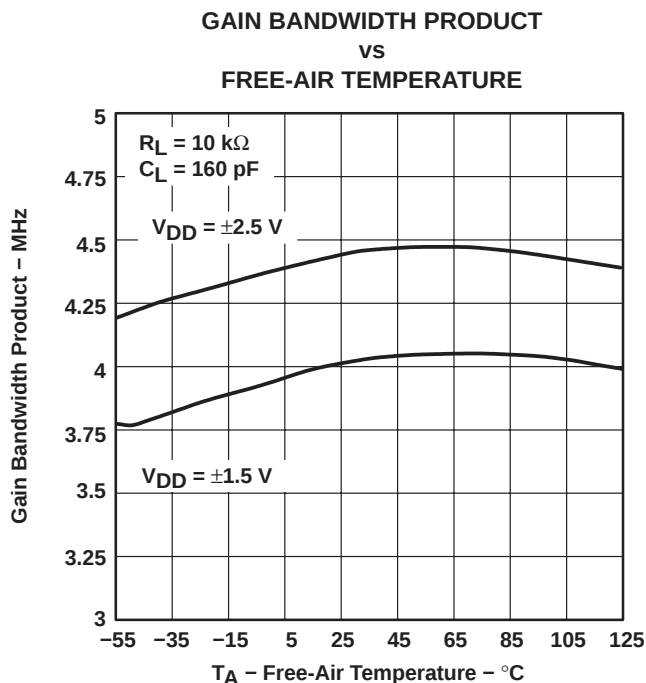


Figure 39

TLV246x-Q1, TLV246xA-Q1

LOW-POWER RAIL-TO-RAIL INPUT/OUTPUT OPERATIONAL AMPLIFIERS WITH SHUTDOWN

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TYPICAL CHARACTERISTICS

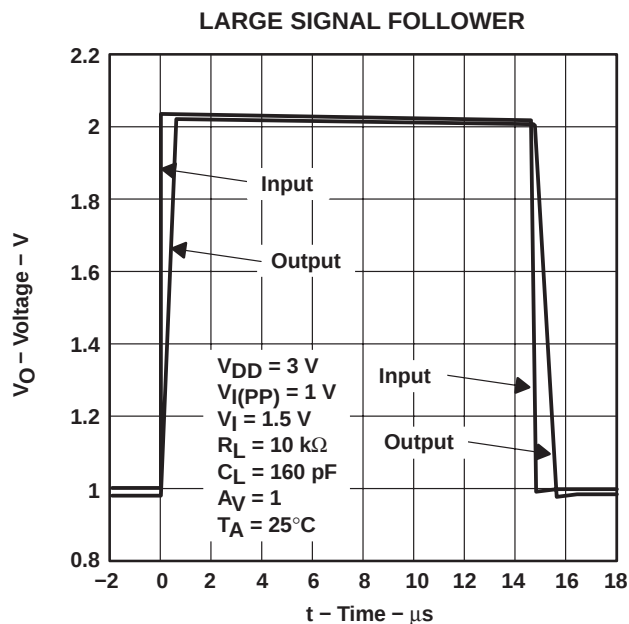


Figure 40

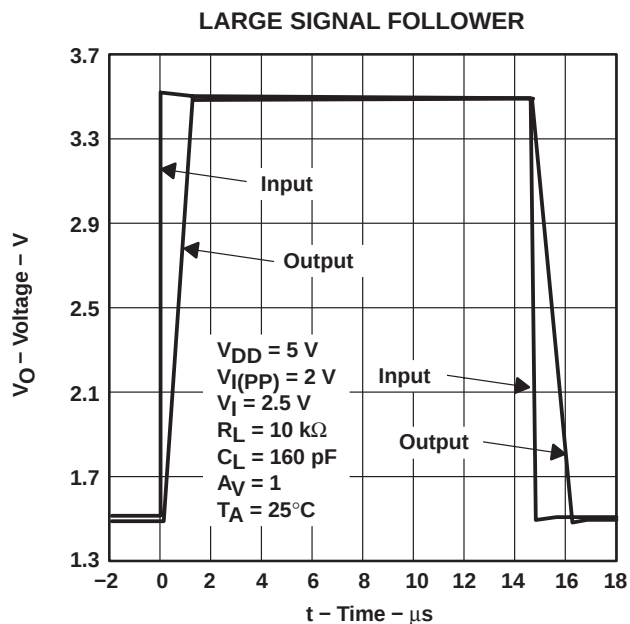


Figure 41

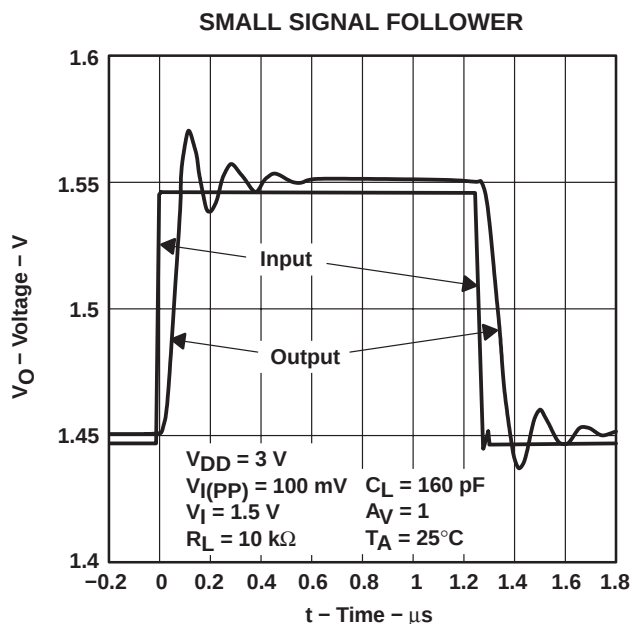


Figure 42

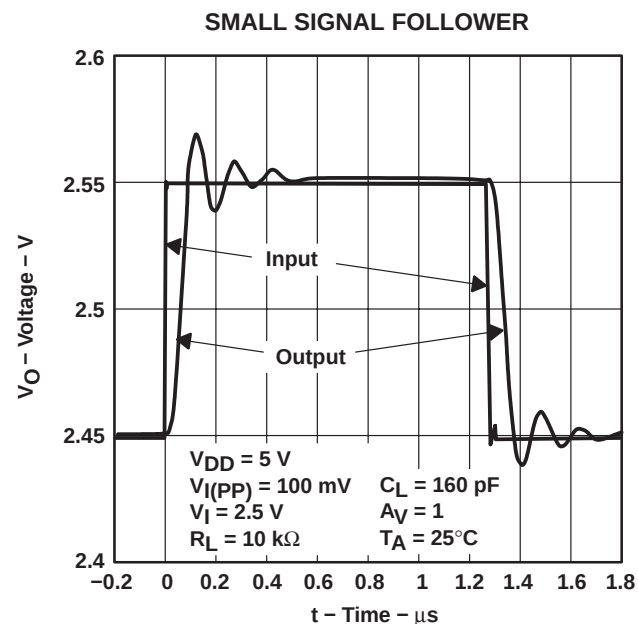


Figure 43

TLV246x-Q1, TLV246xA-Q1

LOW-POWER RAIL-TO-RAIL INPUT/OUTPUT OPERATIONAL AMPLIFIERS WITH SHUTDOWN

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TYPICAL CHARACTERISTICS

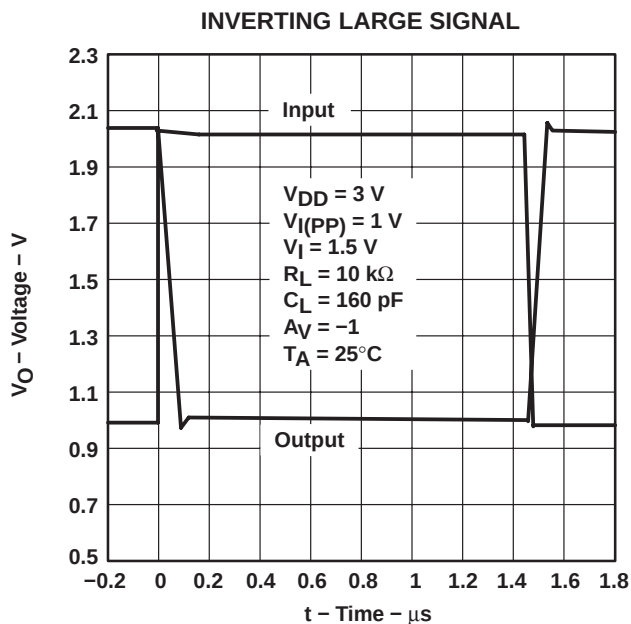


Figure 44

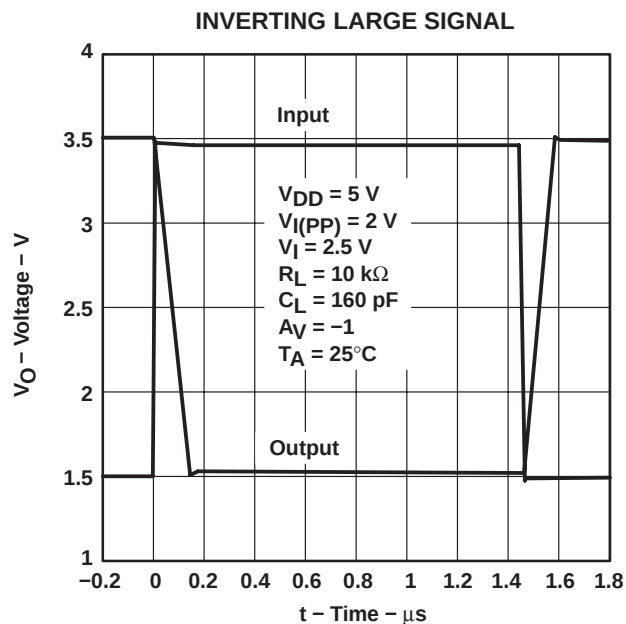


Figure 45

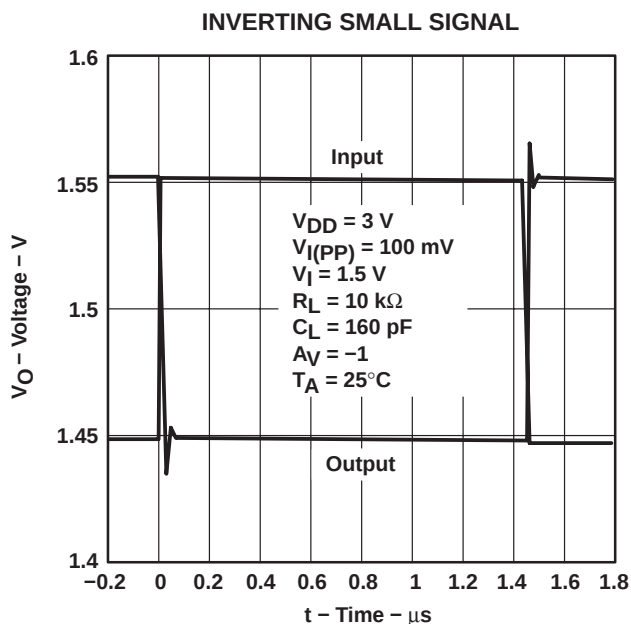


Figure 46

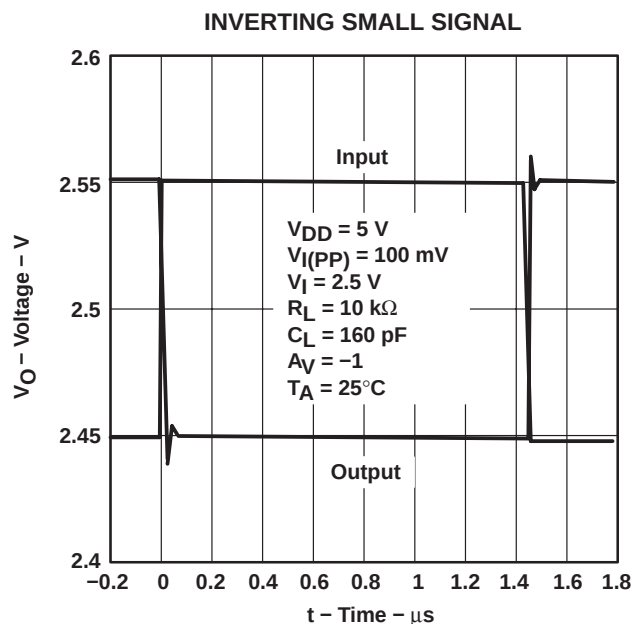


Figure 47

TLV246x-Q1, TLV246xA-Q1

LOW-POWER RAIL-TO-RAIL INPUT/OUTPUT OPERATIONAL AMPLIFIERS WITH SHUTDOWN

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PARAMETER MEASUREMENT INFORMATION

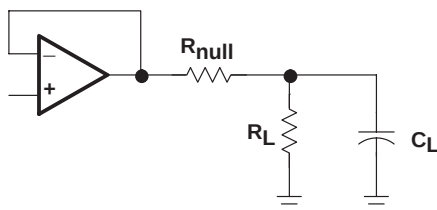


Figure 48

APPLICATION INFORMATION

driving a capacitive load

When the amplifier is configured in this manner, capacitive loading directly on the output decreases the device's phase margin leading to high frequency ringing or oscillations. Therefore, for capacitive loads of greater than 10 pF, it is recommended that a resistor be placed in series (R_{NULL}) with the output of the amplifier, as shown in Figure 49. A minimum value of 20 Ω works well for most applications.

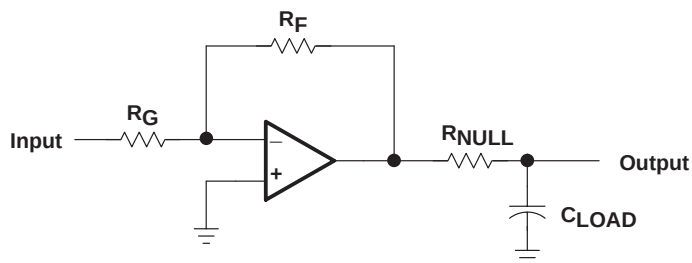


Figure 49. Driving a Capacitive Load

offset voltage

The output offset voltage (V_{OO}) is the sum of the input offset voltage (V_{IO}) and both input bias currents (I_{IB}) times the corresponding gains. The schematic and formula in Figure 50 can be used to calculate the output offset voltage.

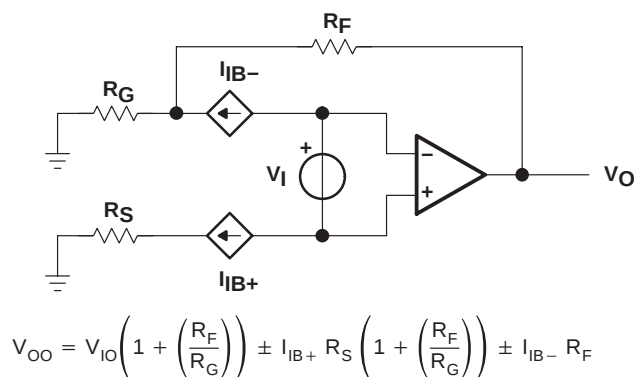


Figure 50. Output Offset Voltage Model

APPLICATION INFORMATION

general configurations

When receiving low-level signals, limiting the bandwidth of the incoming signals into the system is often required. The simplest way to accomplish this is to place an RC filter at the noninverting terminal of the amplifier (see Figure 51).

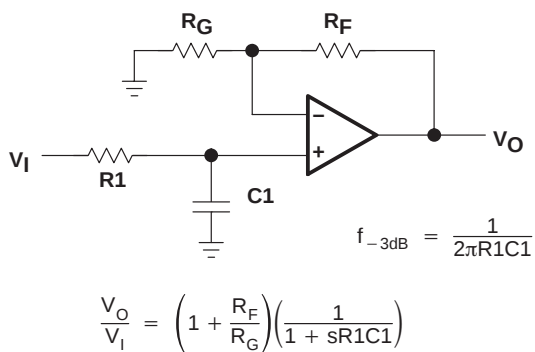


Figure 51. Single-Pole Low-Pass Filter

If even more attenuation is needed, a multiple pole filter is required. The Sallen-Key filter can be used for this task. For best results, the amplifier should have a bandwidth that is eight to ten times the filter frequency bandwidth. Failure to do this can result in phase shift of the amplifier.

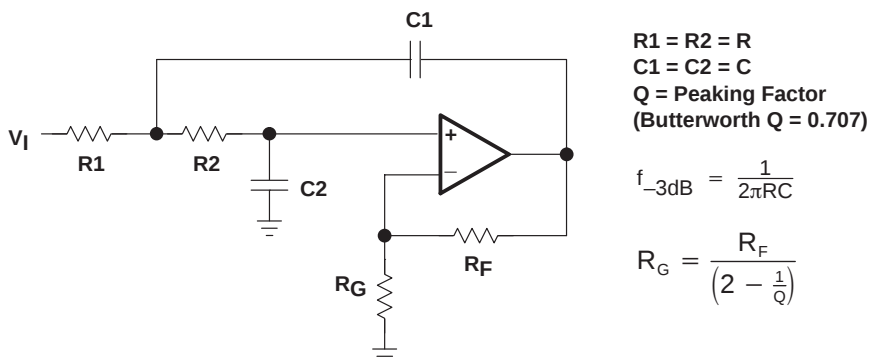


Figure 52. 2-Pole Low-Pass Sallen-Key Filter

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LOW-POWER RAIL-TO-RAIL INPUT/OUTPUT OPERATIONAL AMPLIFIERS WITH SHUTDOWN

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APPLICATION INFORMATION

shutdown function

Two members of the TLV246x family (TLV2460 and TLV2463) have a shutdown terminal for conserving battery life in portable applications. When the shutdown terminal is tied low, the supply current is reduced to 0.3 $\mu\text{A}/\text{channel}$, the amplifier is disabled, and the outputs are placed in a high-impedance mode. To enable the amplifier, the shutdown terminal can either be left floating or pulled high. When the shutdown terminal is left floating, care should be taken to ensure that parasitic leakage current at the shutdown terminal does not inadvertently place the operational amplifier into shutdown. The shutdown terminal threshold is always referenced to $V_{DD}/2$. Therefore, when operating the device with split supply voltages (e.g., $\pm 2.5\text{ V}$), the shutdown terminal must be pulled to V_{DD-} (not GND) to disable the operational amplifier.

The amplifier's output with a shutdown pulse is shown in Figures 22, 23, 24, and 25. The amplifier is powered with a single 5-V supply and configured as a noninverting configuration with a gain of 5. The amplifier turnon and turnoff times are measured from the 50% point of the shutdown pulse to the 50% point of the output waveform. The times for the single, dual, and quad are listed in the data tables.

circuit layout considerations

To achieve the levels of high performance of the TLV246x, follow proper printed-circuit board design techniques. A general set of guidelines is given in the following.

- Ground planes – It is highly recommended that a ground plane be used on the board to provide all components with a low inductive ground connection. However, in the areas of the amplifier inputs and output, the ground plane can be removed to minimize the stray capacitance.
- Proper power supply decoupling – Use a 6.8- μF tantalum capacitor in parallel with a 0.1- μF ceramic capacitor on each supply terminal. It may be possible to share the tantalum among several amplifiers depending on the application, but a 0.1- μF ceramic capacitor should always be used on the supply terminal of every amplifier. In addition, the 0.1- μF capacitor should be placed as close as possible to the supply terminal. As this distance increases, the inductance in the connecting trace makes the capacitor less effective. The designer should strive for distances of less than 0.1 inches between the device power terminals and the ceramic capacitors.
- Sockets – Sockets can be used but are not recommended. The additional lead inductance in the socket pins often leads to stability problems. Surface-mount packages soldered directly to the printed circuit board is the best implementation.
- Short trace runs/compact part placements – Optimum high performance is achieved when stray series inductance has been minimized. To realize this, the circuit layout should be made as compact as possible, thereby minimizing the length of all trace runs. Particular attention should be paid to the inverting input of the amplifier. Its length should be kept as short as possible. This minimizes stray capacitance at the input of the amplifier.
- Surface-mount passive components – Using surface-mount passive components is recommended for high-performance amplifier circuits for several reasons. First, because of the extremely low lead inductance of surface-mount components, the problem with stray series inductance is greatly reduced. Second, the small size of surface-mount components naturally leads to a more compact layout, thereby minimizing both stray inductance and capacitance. If leaded components are used, it is recommended that the lead lengths be kept as short as possible.

APPLICATION INFORMATION

general power dissipation considerations

For a given θ_{JA} , the maximum power dissipation is shown in Figure 53 and is calculated by the following formula:

$$P_D = \left(\frac{T_{MAX} - T_A}{\theta_{JA}} \right)$$

Where:

P_D = Maximum power dissipation of TLV246x (watts)

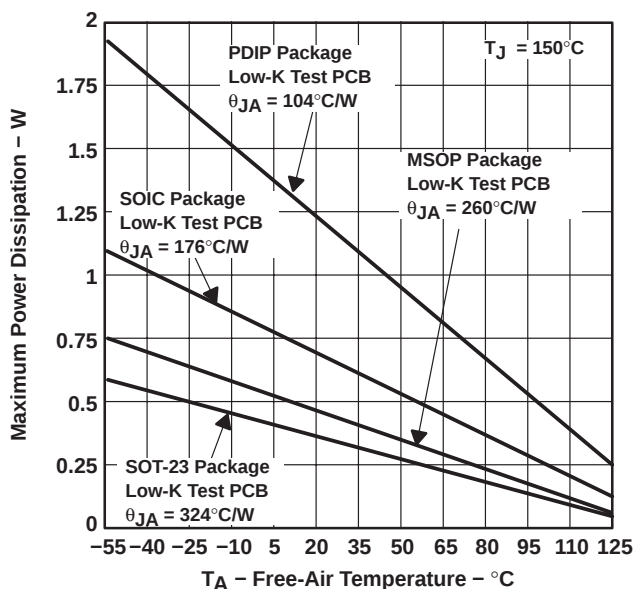
T_{MAX} = Absolute maximum junction temperature (150°C)

T_A = Ambient free-air temperature (°C)

$\theta_{JA} = \theta_{JC} + \theta_{CA}$

θ_{JC} = Thermal coefficient from junction to case

θ_{CA} = Thermal coefficient from case to ambient air (°C/W)



NOTE A: Results are with no air flow and using JEDEC Standard Low-K test PCB.

Figure 53. Maximum Power Dissipation vs Free-Air Temperature

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LOW-POWER RAIL-TO-RAIL INPUT/OUTPUT OPERATIONAL AMPLIFIERS WITH SHUTDOWN

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APPLICATION INFORMATION

macromodel information

Macromodel information provided was derived using Microsim Parts™ Release 8, the model generation software used with Microsim PSpice™. The Boyle macromodel (see Note 2) and subcircuit in Figure 54 are generated using the TLV246x typical electrical and operating characteristics at $T_A = 25^\circ\text{C}$. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

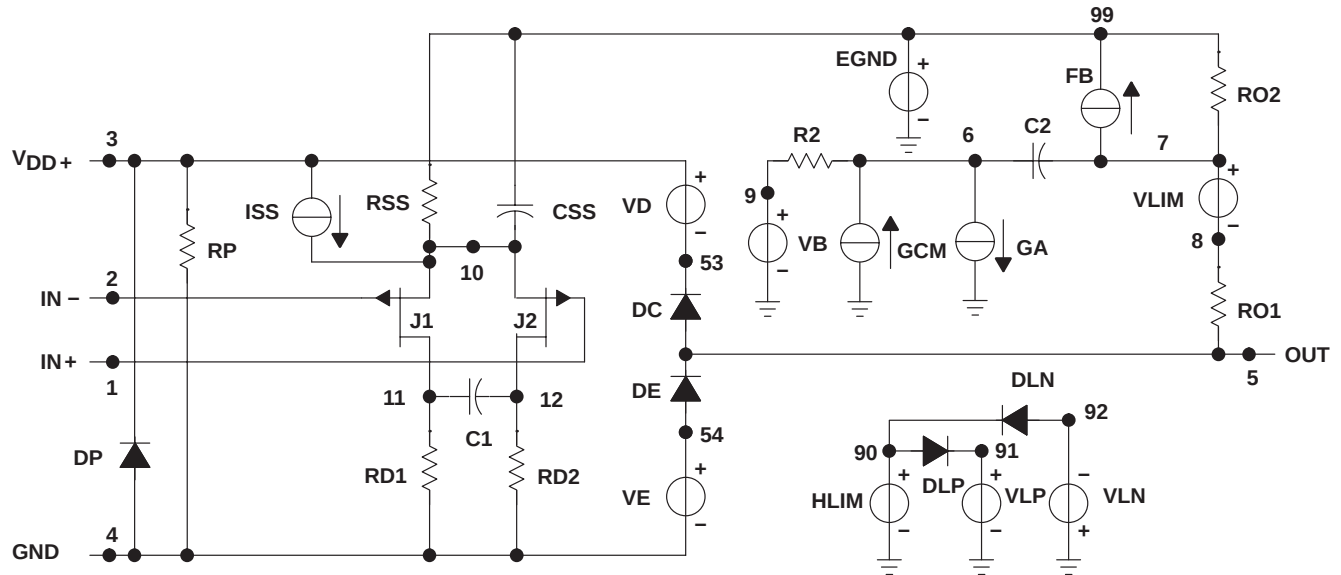
NOTE 1: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers", *IEEE Journal of Solid-State Circuits*, SC-9, 353 (1974).

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TLV246x-Q1, TLV246xA-Q1 LOW-POWER RAIL-TO-RAIL INPUT/OUTPUT OPERATIONAL AMPLIFIERS WITH SHUTDOWN

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```
.SUBCKT TLV246X 1 2 3 4 5
C1 11 12 2.46034E-12
C2 6 7 10.0000E-12
CSS 10 99 443.21E-15
DC 5 53 DY
DE 54 5 DY
DLP 90 91 DX
DLN 92 90 DX
DP 4 3 DX
EGND 99 0 POLY (2) (3,0) (4,0) 0 .5 .5
FB 7 99 POLY (5) VB VC VE VLP
+ VLN 0 21.600E6 -1E3 1E3 22E6 -22E6
GA 6 0 11 12 345.26E-6
GCM 0 6 10 99 15.4226E-9
ISS 10 4 DC 18.850E-6
HLIM 90 0 VLIM 1K
J1 11 2 10 JX1
J2 12 1 10 JX2
R2 6 9 100.00E3
```

```
RD1 3 11 2.8964E3
RD2 3 12 2.8964E3
R01 8 5 5.6000
R02 7 99 6.2000
RP 3 4 8.9127
RSS 10 99 10.610E6
VB 9 0 DC 0
VC 3 53 DC .7836
VE 54 4 DC .7436
VLIM 7 8 DC 0
VLP 91 0 DC 117
VLN 0 92 DC 117
.MODEL DX D (IS=800.00E-18)
.MODEL DY D (IS=800.00E-18 Rs=1m Cjo=10p)
.MODEL JX1 NJF (IS=1.0000E-12 BETA=6.3239E-3
+ VTO=-1)
.MODEL JX2 NJF (IS=1.0000E-12 BETA=6.3239E-3
+ VTO=-1)
.ENDS
```

```
.subckt TLV_246Y 1 2 3 4 5 6
c1 11 12 2.4603E-12
c2 72 7 10.000E-12
css 10 99 443.21E-15
dc 70 53 dy
de 54 70 dy
dlp 90 91 dx
dln 92 90 dx
dp 4 3 dx
egnd 99 0 poly(2) (3,0) (4,0) 0 .5 .5
fb 7 99 poly(5) vb vc ve vlp vln 0
21.600E6 -1E3 1E3 22E6 -22E6
ga 72 0 11 12 345.26E-6
gcm 0 72 10 99 15.422E-9
iss 74 4 dc 18.850E-6
hlim 90 0 vlum 1K
j1 11 2 10 jx1
j2 12 1 10 jx2
r2 72 9 100.00E3
rd1 3 11 2.8964E3
rd2 3 12 2.8964E3
ro1 8 70 5.6000
ro2 7 99 6.2000
```

```
rp 3 71 8.9127
rss 10 99 10.610E6
rs1 6 4 1G
rs2 6 4 1G
rs3 6 4 1G
rs4 6 4 1G
s1 71 4 6 4 s1x
s2 70 5 6 4 s1x
s3 10 74 6 4 s1x
s4 74 4 6 4 s2x
vb 9 0 dc 0
vc 3 53 dc .7836
ve 54 4 dc .7436
vlum 7 8 dc 0
vlp 91 0 dc 117
vln 0 92 dc 117
.model dx D(Is=800.00E-18)
.model dy D(Is=800.00E-18 Rs=1m Cjo=10p)
.model jx1 NJF(Is=1.0000E-12 Beta=6.3239E-3 Vto=-1)
.model jx2 NJF(Is=1.0000E-12 Beta=6.3239E-3 Vto=-1)
.model s1x VSWITCH(Roff=1E8 Ron=1.0 Voff=2.5 Von=0.0)
.model s2x VSWITCH(Roff=1E8 Ron=1.0 Voff=0 Von=2.5)
.ends
```

Figure 54. Boyle Macromodels and Subcircuit

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
TLV2460AQDRG4Q1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2460AQDRQ1	ACTIVE	SOIC	D	8	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
TLV2460AQPWRQ1	ACTIVE	TSSOP	PW	8	2000	TBD	CU NIPDAU	Level-1-220C-UNLIM
TLV2460QDRG4Q1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2460QDRQ1	ACTIVE	SOIC	D	8	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
TLV2460QPWRQ1	ACTIVE	TSSOP	PW	8	2000	TBD	CU NIPDAU	Level-1-220C-UNLIM
TLV2461AQDRG4Q1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2461AQDRQ1	ACTIVE	SOIC	D	8	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
TLV2461AQPWRQ1	ACTIVE	TSSOP	PW	8	2000	TBD	CU NIPDAU	Level-1-220C-UNLIM
TLV2461QDRG4Q1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2461QDRQ1	ACTIVE	SOIC	D	8	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
TLV2461QPWRQ1	ACTIVE	TSSOP	PW	8	2000	TBD	CU NIPDAU	Level-1-220C-UNLIM
TLV2462AQDRG4Q1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2462AQDRQ1	ACTIVE	SOIC	D	8	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
TLV2462AQPWRQ1	ACTIVE	TSSOP	PW	8	2000	TBD	CU NIPDAU	Level-1-220C-UNLIM
TLV2462QDRG4Q1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2462QDRQ1	ACTIVE	SOIC	D	8	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
TLV2462QPWRQ1	ACTIVE	TSSOP	PW	8	2000	TBD	CU NIPDAU	Level-1-220C-UNLIM
TLV2463AQDRG4Q1	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2463AQDRQ1	ACTIVE	SOIC	D	14	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
TLV2463AQPWRQ1	ACTIVE	TSSOP	PW	14	2000	TBD	CU NIPDAU	Level-1-250C-UNLIM
TLV2463QDRG4Q1	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2463QDRQ1	ACTIVE	SOIC	D	14	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
TLV2463QPWRQ1	ACTIVE	TSSOP	PW	14	2000	TBD	Call TI	Level-1-250C-UNLIM
TLV2464AQPWRQ1	ACTIVE	TSSOP	PW	14	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

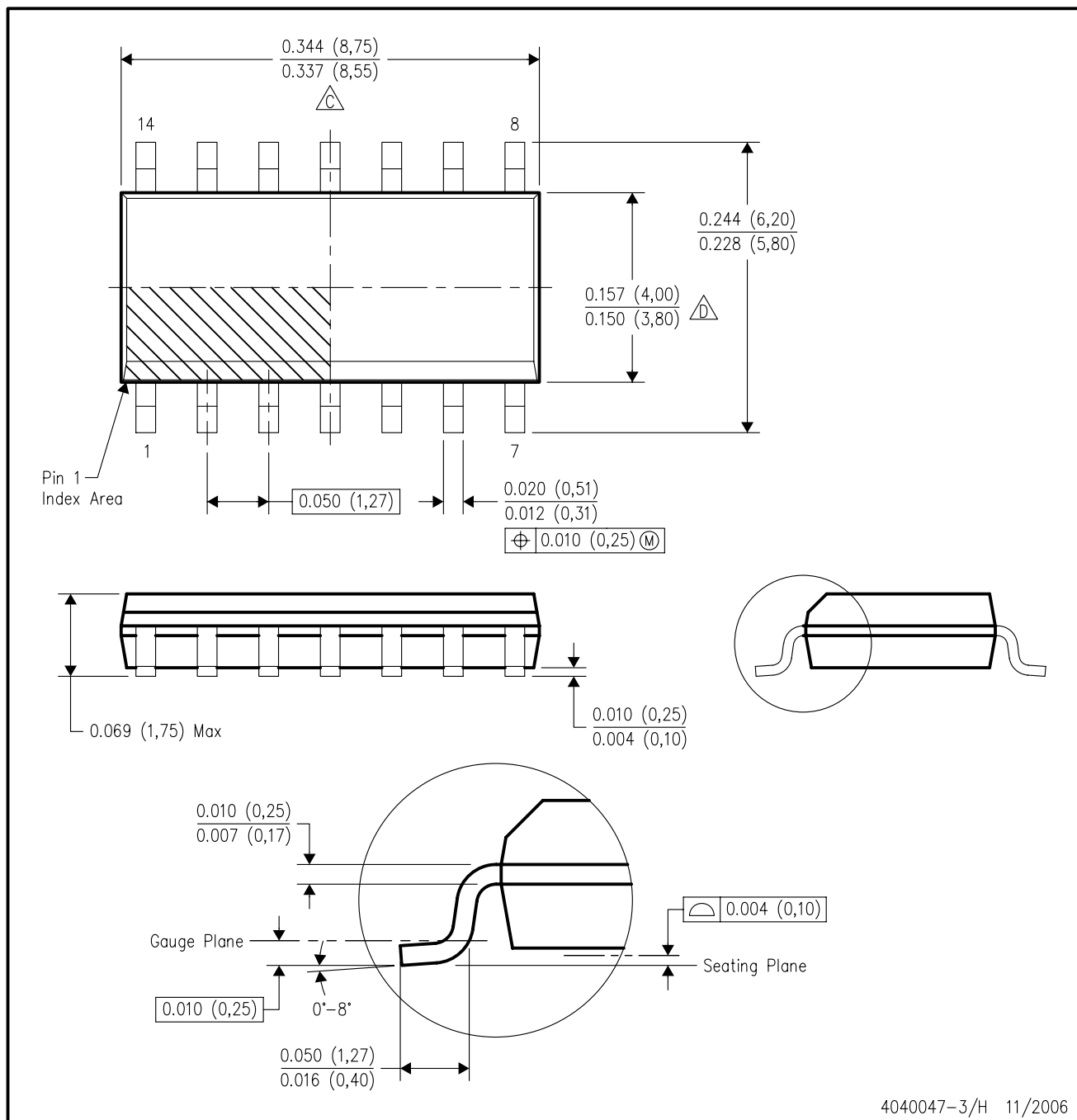
⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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D (R-PDSO-G14)

PLASTIC SMALL-OUTLINE PACKAGE



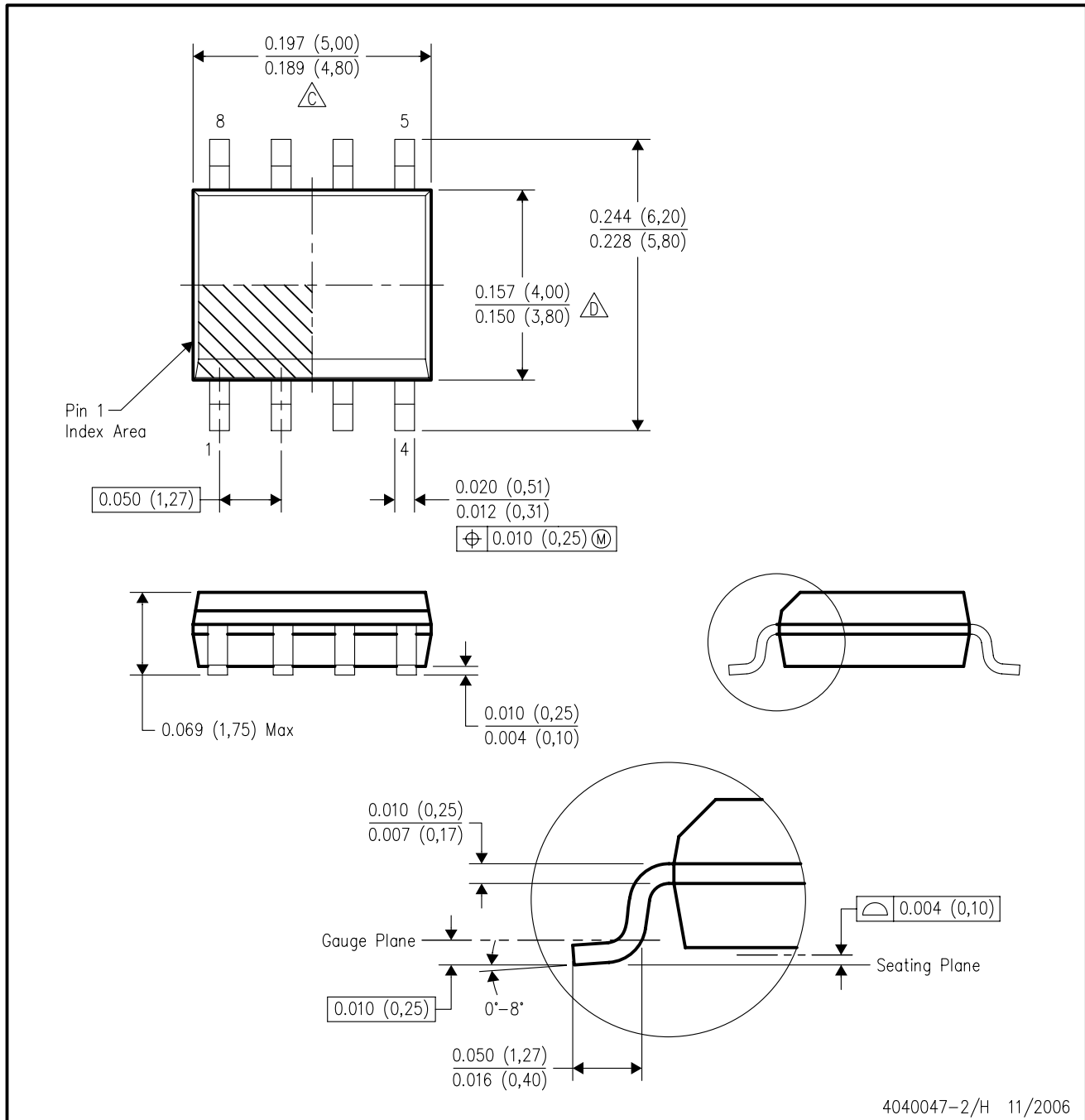
4040047-3/H 11/2006

NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
- D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
- E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



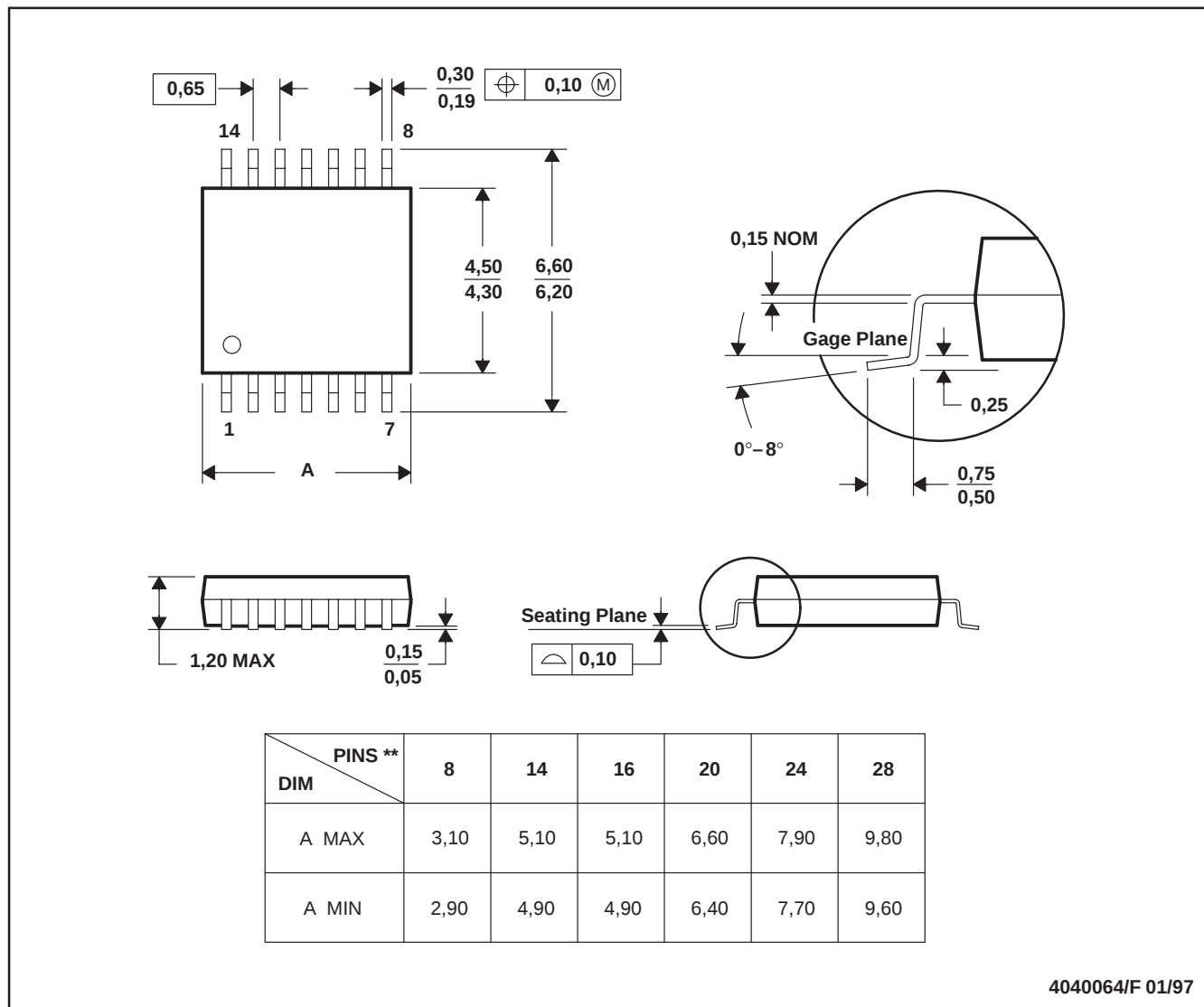
4040047-2/H 11/2006

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
 -  D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
 - E. Reference JEDEC MS-012 variation AA.

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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