



PRODUCT DATA SHEET



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Datasheet



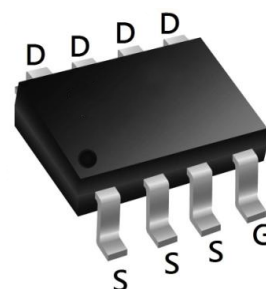
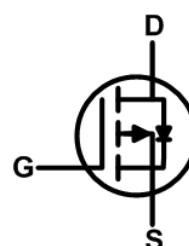
Resources



Samples

Please note: Please check the JINGAO Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.jg-semi.cn. Please email any questions regarding the system integration to JINGAO_questions@jgsemi.com.

- ★ 100% EAS Guaranteed
- ★ Green Device Available
- ★ Super Low Gate Charge
- ★ Excellent CdV/dt effect decline
- ★ Advanced high cell density Trench technology


SOP8

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$, unless otherwise noted)

Parameter		Symbol	Value	Unit
Drain-Source voltage		V_{DS}	-30	V
Gate-Source voltage		V_{GS}	± 20	V
Continuous Drain Current	$T_A = 25^\circ\text{C}$	I_D	-18	A
	$T_A = 100^\circ\text{C}$		-8.8	
Pulsed Drain Current ¹		I_{DM}	-53	A
Single Pulse Avalanche Energy ²		EAS	80	mJ
Total Power Dissipation	$T_A = 25^\circ\text{C}$	P_D	3	W
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal Resistance from Junction-to-Ambient ³	$R_{\theta JA}$	41.6	$^\circ\text{C/W}$

Electrical Characteristics ($T_J = 25^\circ\text{C}$, unless otherwise noted)

Parameter		Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static Characteristics							
Drain-Source Breakdown Voltage		$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = -250\mu A$	-30	-	-	V
Gate-body Leakage current		I_{GSS}	$V_{DS} = 0V, V_{GS} = \pm 20V$	-	-	± 100	nA
Zero Gate Voltage Drain Current	$T_J=25^{\circ}C$	I_{DSS}	$V_{DS} = -30V, V_{GS} = 0V$	-	-	-1	μA
	$T_J=100^{\circ}C$			-	-	-100	
Gate-Threshold Voltage		$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\mu A$	-1.0	-	-2.5	V
Drain-Source On-Resistance ⁴		$R_{DS(on)}$	$V_{GS} = -10V, I_D = -12A$	-	5.8	9.2	m Ω
			$V_{GS} = -4.5V, I_D = -10A$	-	8	14	
Forward Transconductance ⁴		g_{fs}	$V_{DS} = -10V, I_D = -10A$	-	50	-	S
Dynamic Characteristics ⁵							
Input Capacitance		C_{iss}	$V_{DS} = -15V, V_{GS} = 0V, f = 1MHz$	-	3100	-	pF
Output Capacitance		C_{oss}		-	430	-	
Reverse Transfer Capacitance		C_{rss}		-	358	-	
Gate Resistance		R_g	$f=1MHz$	-	9.5	-	Ω
Switching Characteristics ⁵							
Total Gate Charge		Q_g	$V_{GS} = -10V, V_{DS} = -15V, I_D = -12A$	-	35	-	nC
Gate-Source Charge		Q_{gs}		-	9.9	-	
Gate-Drain Charge		Q_{gd}		-	10.5	-	
Turn-On Delay Time		$t_{d(on)}$	$V_{GS} = -10V, V_{DD} = -15V, R_G = 3\Omega, I_D = -12A$	-	10.8	-	ns
Rise Time		t_r		-	13.2	-	
Turn-Off Delay Time		$t_{d(off)}$		-	73	-	
Fall Time		t_f		-	35	-	
Reverse Recovery Time		t_{rr}	$I_F = -12A, dI_F/dt = 100A/\mu s$	-	25	-	ns
Reverse Recovery Charge		Q_{rr}		-	10	-	nC
Drain-source body diode Characteristics							
Diode Forward Voltage ⁴		V_{SD}	$I_S = -1A, V_{GS} = 0V$	-	-	-1.2	V
Continuous Source Current	$T_A=25^{\circ}C$	I_S	-	-	-	-14	A

Notes:

1. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)} = 150^\circ\text{C}$.
2. The EAS data shows Max. rating . The test condition is $V_{DD} = -25V, V_{GS} = -10V, L = 0.1\text{mH}, I_{AS} = -40A$.
3. The data tested by surface mounted on a 1 inch2 FR-4 board with 20Z copper, The value in any given application depends on the user's specific board design.
4. The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.
5. This value is guaranteed by design hence it is not included in the production test.

Typical Characteristics

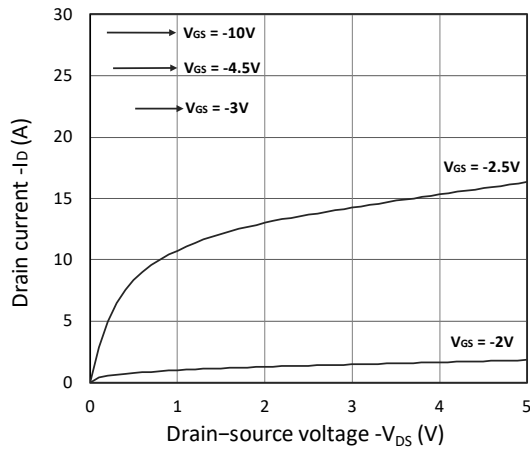


Figure 1. Output Characteristics

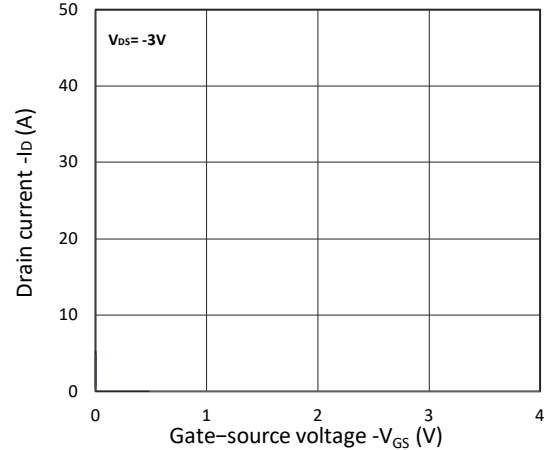


Figure 2. Transfer Characteristics

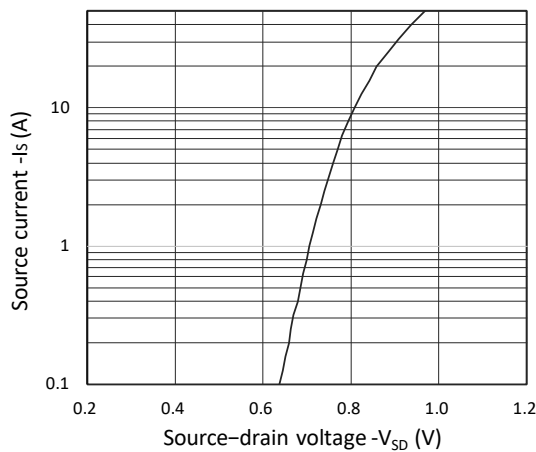


Figure 3. Forward Characteristics of Reverse

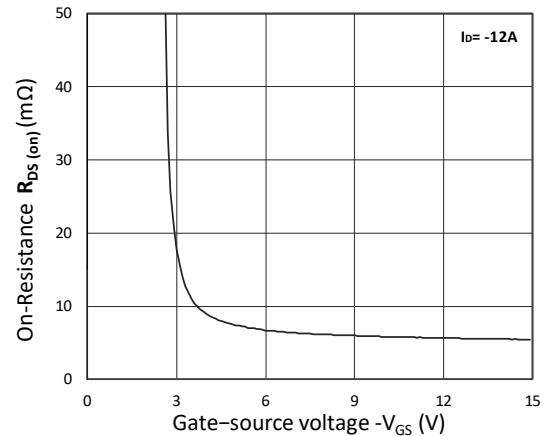


Figure 4. $R_{DS(ON)}$ vs. V_{GS}

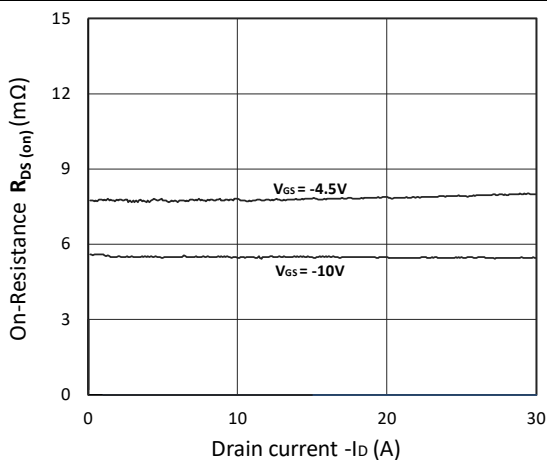


Figure 5. $R_{DS(ON)}$ vs. I_D

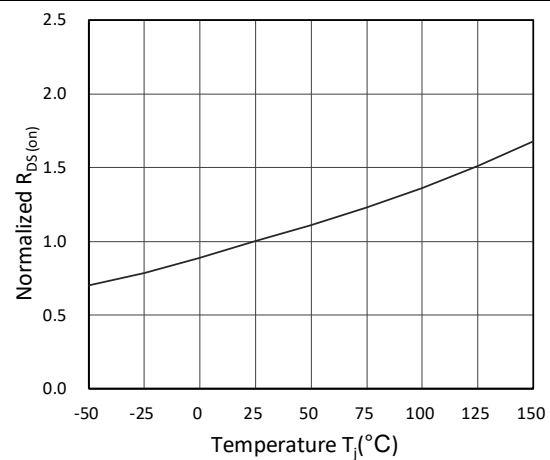


Figure 6. Normalized $R_{DS(on)}$ vs. Temperature

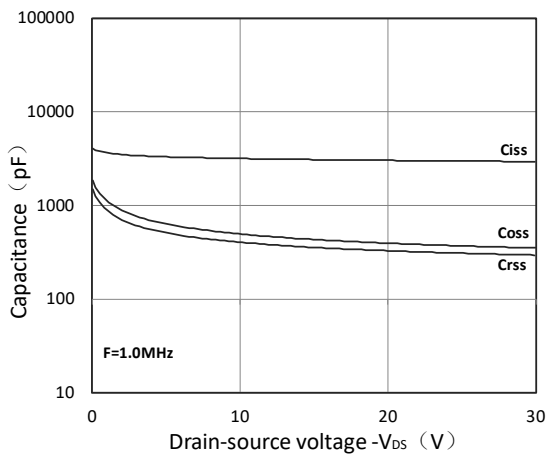


Figure 7. Capacitance Characteristics

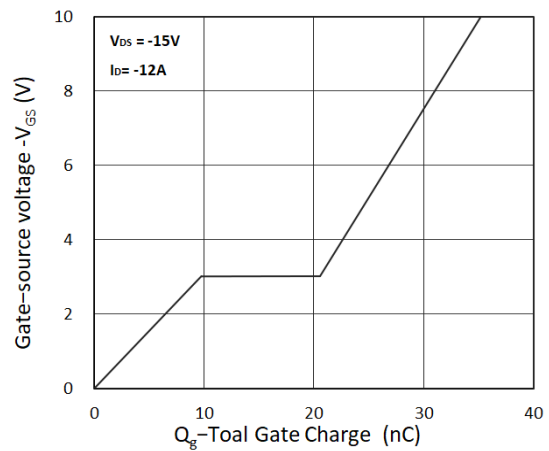


Figure 8. Gate Charge Characteristics

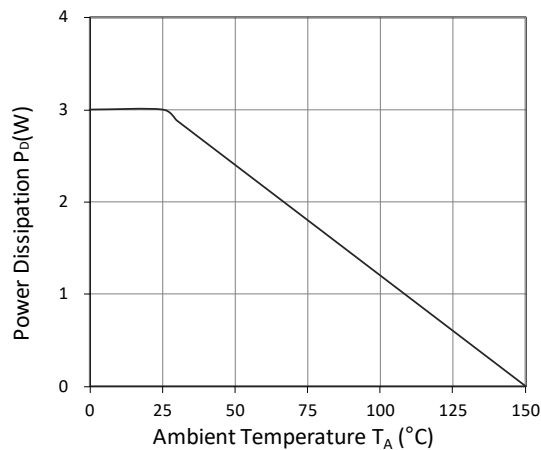


Figure 9. Power Dissipation

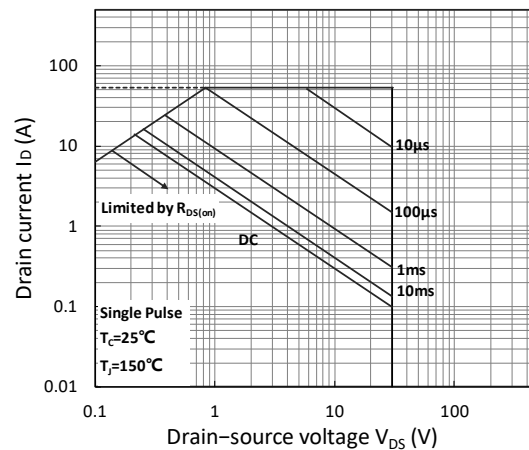


Figure 10. Safe Operating Area

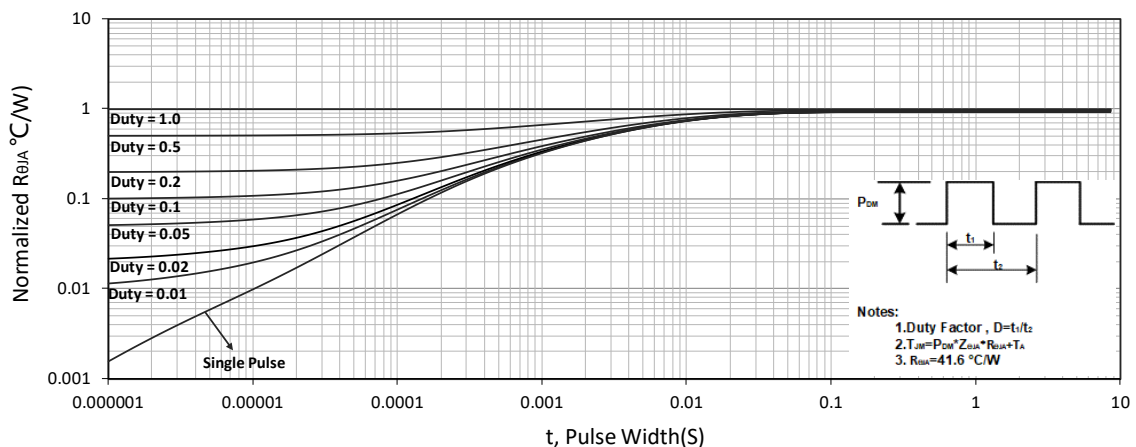
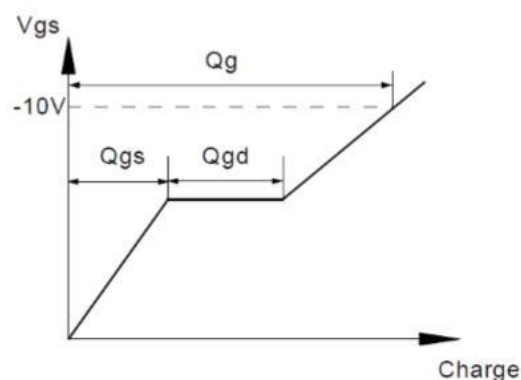
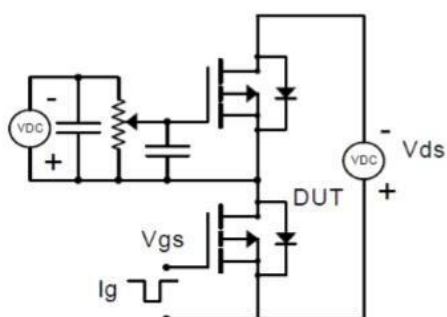


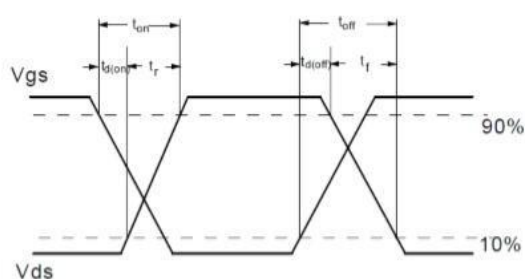
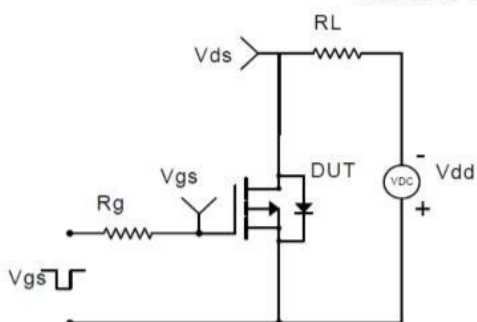
Figure 11. Normalized Maximum Transient Thermal Impedance

Test Circuit

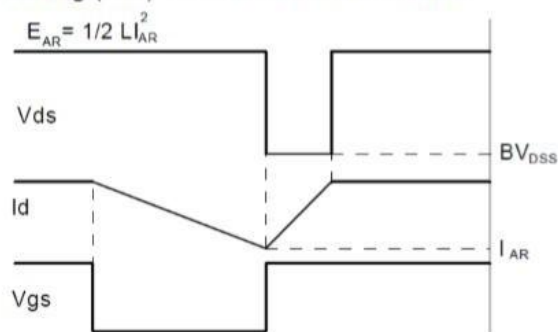
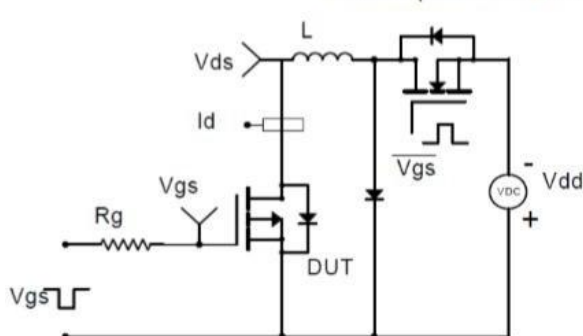
Gate Charge Test Circuit & Waveform



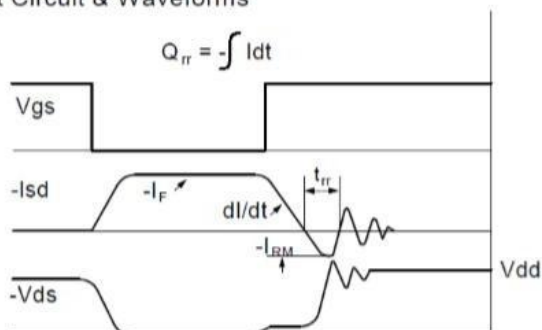
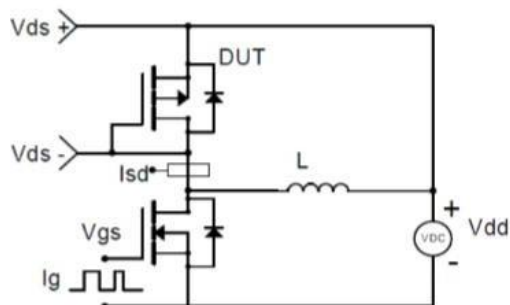
Resistive Switching Test Circuit & Waveforms

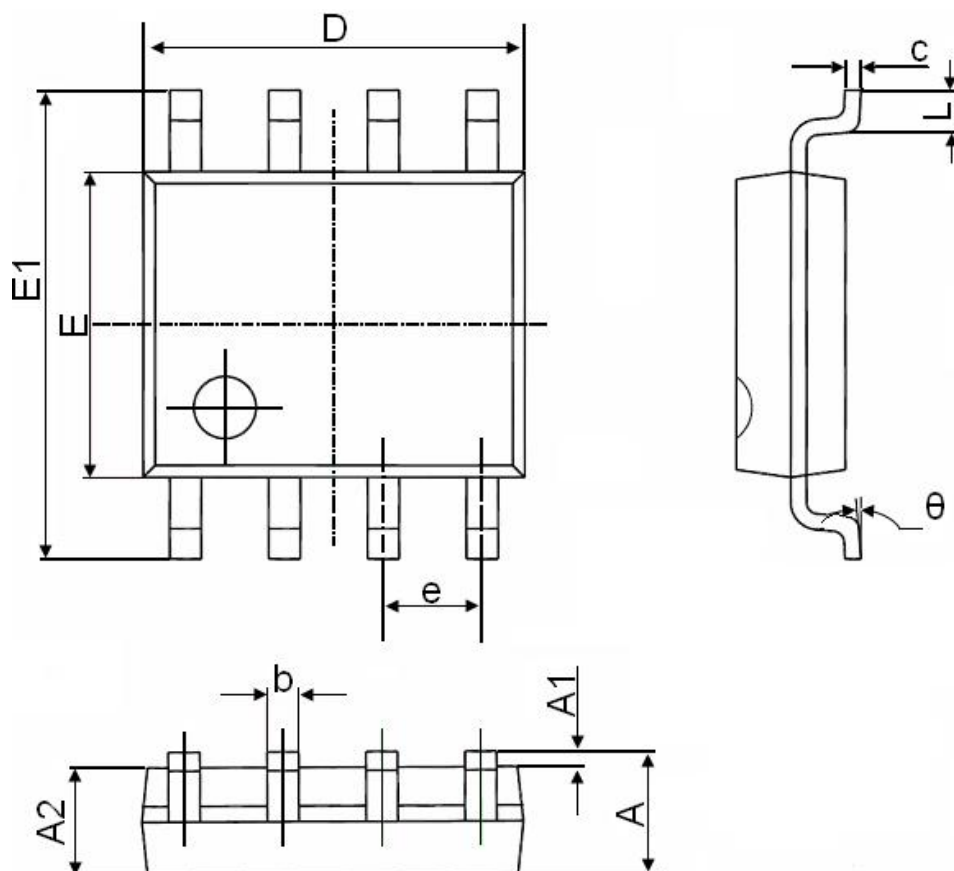


Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



SOP-8 Package Information


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

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