**ALPHA & OMEGA SEMICONDUCTOR**

# AON7401
## P-Channel Enhancement Mode Field Effect Transistor

### General Description

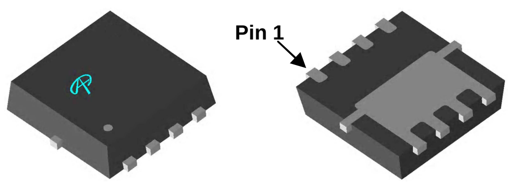
The AON7401/L uses advanced trench technology to provide excellent $R_{DS(ON)}$, and ultra-low low gate charge with a 25V gate rating. This device is suitable for use as a load switch or in PWM applications.
*AON7401 and AON7401L are electrically identical.*
*-RoHS Compliant*
*-AON7401L is Halogen Free*

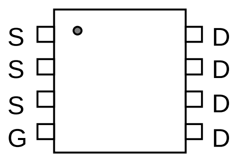
### Features

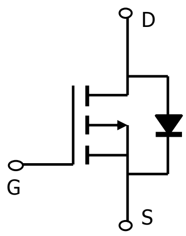
$V_{DS}$ (V) = -30V
$I_D$ = -9A (V$_{GS}$ = -10V)
$R_{DS(ON)}$ < 14mΩ ($V_{GS}$ = -10V)
$R_{DS(ON)}$ < 17mΩ ($V_{GS}$ = -6V)

**DFN 3x3**

**Top View** **Bottom View**




**Absolute Maximum Ratings $T_A$=25°C unless otherwise noted**

| Parameter | | Symbol | Maximum | Units |
|---|---|---|---|---|
| Drain-Source Voltage | | $V_{DS}$ | -30 | V |
| Gate-Source Voltage | | $V_{GS}$ | ±25 | V |
| Continuous Drain Current [B,G] | $T_C$=25°C | $I_D$ | -20 | |
| | $T_C$=100°C | $I_D$ | -20 | |
| Pulsed Drain Current [C] | | $I_{DM}$ | -80 | A |
| Continuous Drain Current | $T_A$=25°C | $I_{DSM}$ | -9 | |
| | $T_A$=70°C | $I_{DSM}$ | -7 | |
| Power Dissipation [B] | $T_C$=25°C | $P_D$ | 27 | |
| | $T_C$=100°C | $P_D$ | 11 | |
| Power Dissipation [A] | $T_A$=25°C | $P_{DSM}$ | 1.6 | W |
| | $T_A$=70°C | $P_{DSM}$ | 1 | |
| Junction and Storage Temperature Range | | $T_J$, $T_{STG}$ | -55 to 150 | °C |

**Thermal Characteristics**

| Parameter | | Symbol | Typ | Max | Units |
|---|---|---|---|---|---|
| Maximum Junction-to-Ambient [A] | t ≤ 10s | $R_{\theta JA}$ | 30 | 40 | °C/W |
| Maximum Junction-to-Ambient [A] | Steady-State | $R_{\theta JA}$ | 60 | 75 | °C/W |
| Maximum Junction-to-Case [D] | Steady-State | $R_{\theta JC}$ | 4 | 4.5 | °C/W |

**Electrical Characteristics ($T_J$=25℃ unless otherwise noted)**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| **STATIC PARAMETERS** | | | | | | | |
| $BV_{DSS}$ | Drain-Source Breakdown Voltage | $I_D$=-250µA, $V_{GS}$=0V | | -30 | | | V |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$=-30V, $V_{GS}$=0V | | | | -1 | µA |
| | | | $T_J$=55℃ | | | -5 | |
| $I_{GSS}$ | Gate-Body leakage current | $V_{DS}$=0V, $V_{GS}$= ±25V | | | | ±100 | nA |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$=$V_{GS}$ $I_D$=-250µA | | -1.7 | -2.2 | -3 | V |
| $I_{D(ON)}$ | On state drain current | $V_{GS}$=-10V, $V_{DS}$=-5V | | -80 | | | A |
| $R_{DS(ON)}$ | Static Drain-Source On-Resistance | $V_{GS}$=-10V, $I_D$=-9A | | | 11 | 14 | mΩ |
| | | | $T_J$=125℃ | | 16 | 19 | |
| | | $V_{GS}$=-6V, $I_D$=-7A | | | 12.9 | 17 | |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$=-5V, $I_D$=-10A | | | 27 | | S |
| $V_{SD}$ | Diode Forward Voltage | $I_S$=-1A,$V_{GS}$=0V | | | -0.7 | -1 | V |
| $I_S$ | Maximum Body-Diode Continuous Current | | | | | -3 | A |
| **DYNAMIC PARAMETERS** | | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{GS}$=0V, $V_{DS}$=-15V, f=1MHz | | | 2060 | 2600 | pF |
| $C_{oss}$ | Output Capacitance | | | | 370 | | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | | | 295 | | pF |
| $R_g$ | Gate resistance | $V_{GS}$=0V, $V_{DS}$=0V, f=1MHz | | | 2.4 | 3.6 | Ω |
| **SWITCHING PARAMETERS** | | | | | | | |
| $Q_g$ | Total Gate Charge | $V_{GS}$=-10V, $V_{DS}$=-15V, $I_D$=-9A | | | 30 | 39 | nC |
| $Q_{gs}$ | Gate Source Charge | | | | 4.6 | | nC |
| $Q_{gd}$ | Gate Drain Charge | | | | 10 | | nC |
| $t_{D(on)}$ | Turn-On DelayTime | $V_{GS}$=-10V, $V_{DS}$=-15V, $R_L$=1.6Ω, $R_{GEN}$=3Ω | | | 11 | | ns |
| $t_r$ | Turn-On Rise Time | | | | 9.4 | | ns |
| $t_{D(off)}$ | Turn-Off DelayTime | | | | 24 | | ns |
| $t_f$ | Turn-Off Fall Time | | | | 12 | | ns |
| $t_{rr}$ | Body Diode Reverse Recovery Time | $I_F$=-9A, dI/dt=500A/µs | | | 14 | 18 | ns |
| $Q_{rr}$ | Body Diode Reverse Recovery Charge | $I_F$=-9A, dI/dt=500A/µs | | | 35 | | nC |

A: The value of $R_{\theta JA}$ is measured with the device in a still air environment with $T_A$ =25℃. The power dissipation $P_{DSM}$ and current rating $I_{DSM}$ are based on $T_{J(MAX)}$=150℃, using steady state junction-to-ambient ther mal resistance.
B. The power dissipation $P_D$ is based on $T_{J(MAX)}$=150℃, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
C: Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150℃.
D. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to case $R_{\theta JC}$ and case to ambient.
E. The static characteristics in Figures 1 to 6 are obtained using <300 µs pulses, duty cycle 0.5% max.
F. These tests are performed with the device mounted on 1 $in^2$ FR-4 board with 2oz. Copper, in a still air environment with $T_A$=25℃. The SOA curve provides a single pulse rating.
G. The maximum current rating is limited by bond-wires.
Rev1: Mar 2009

## TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

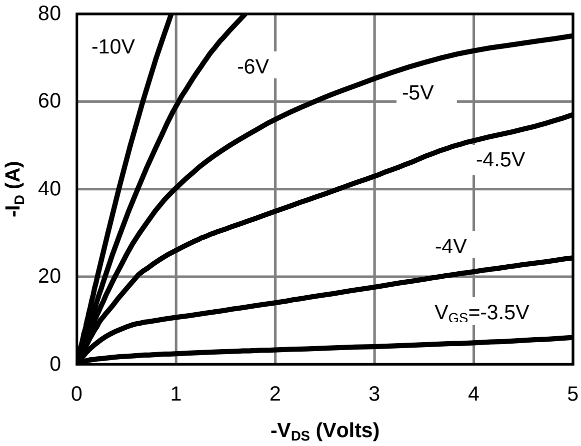



**Figure 1: On-Region Characteristics**

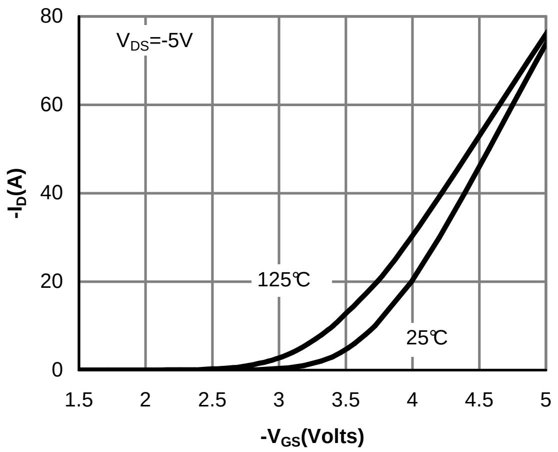



**Figure 2: Transfer Characteristics**

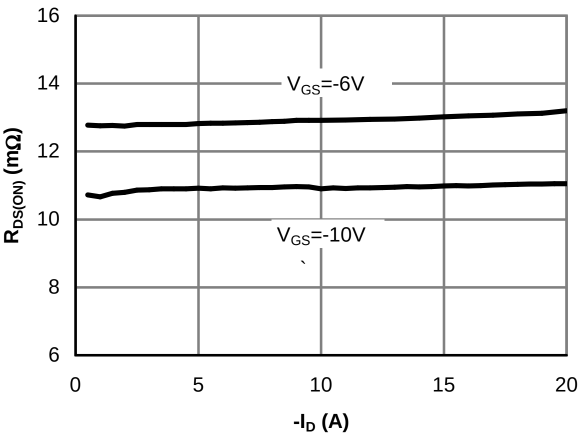



**Figure 3: On-Resistance vs. Drain Current and Gate Voltage**

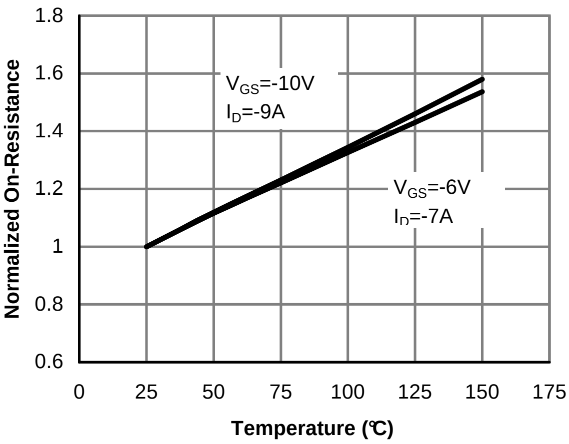



**Figure 4: On-Resistance vs. Junction Temperature**

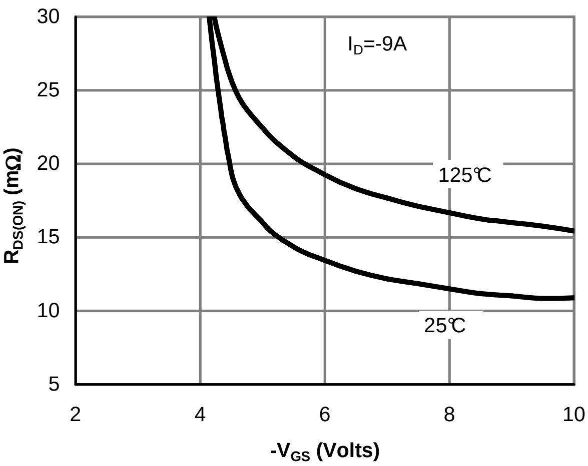



**Figure 5: On-Resistance vs. Gate-Source Voltage**

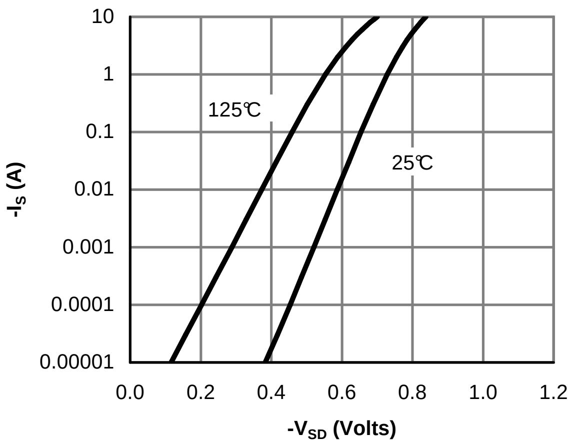



**Figure 6: Body-Diode Characteristics**

## TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

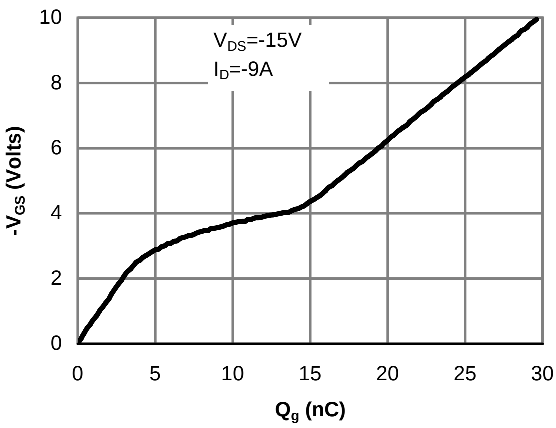



**Figure 7: Gate-Charge Characteristics**

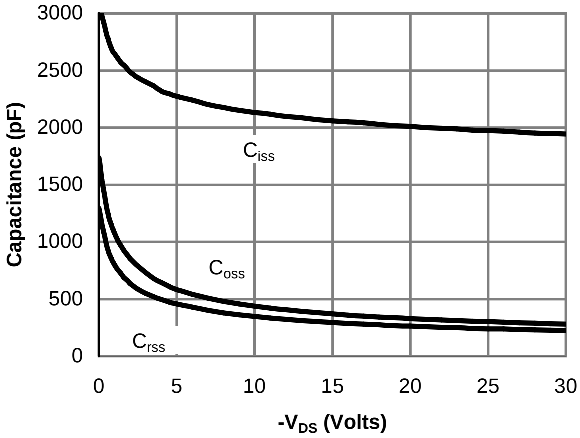



**Figure 8: Capacitance Characteristics**

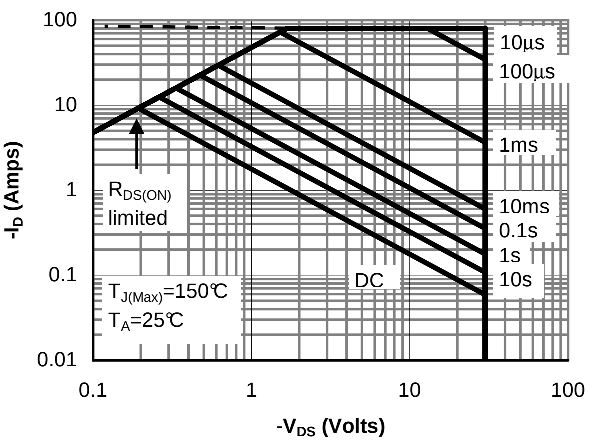



**Figure 9: Maximum Forward Biased Safe Operating Area (Note F)**

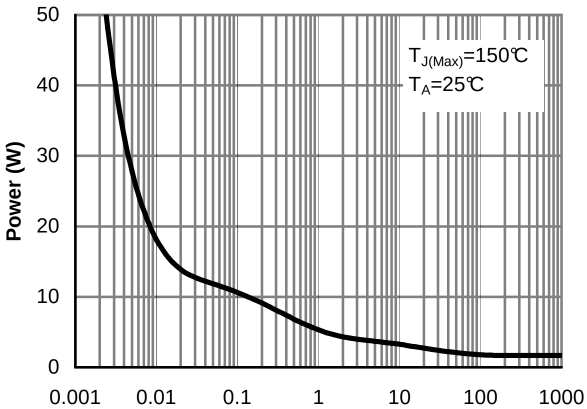



**Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)**

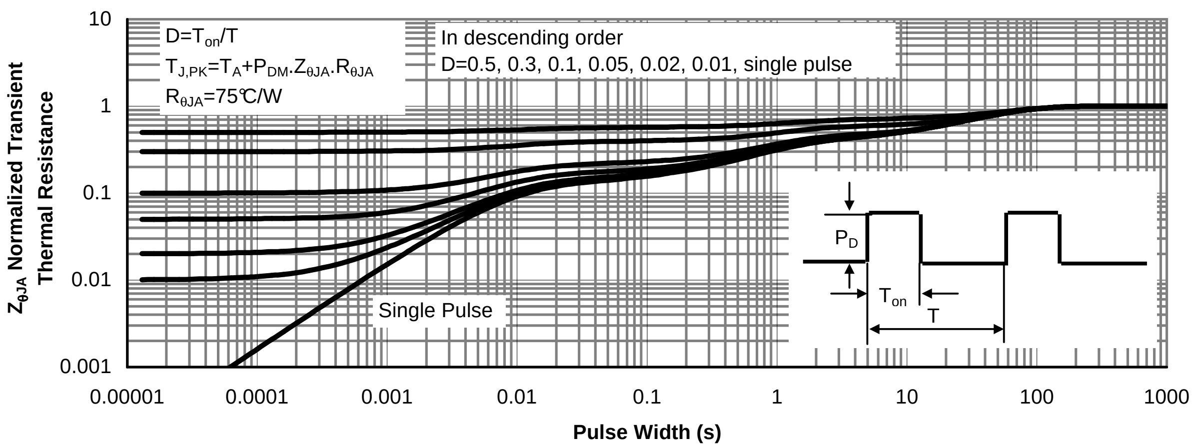
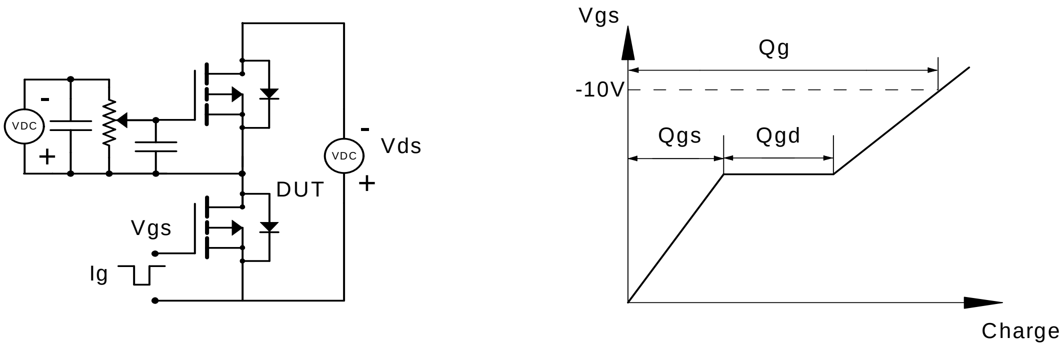
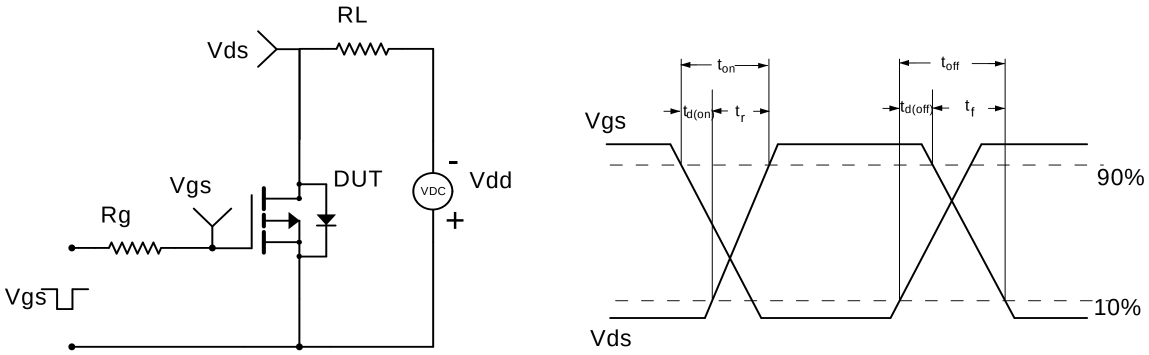



**Figure 11: Normalized Maximum Transient Thermal Impedance(Note F)**

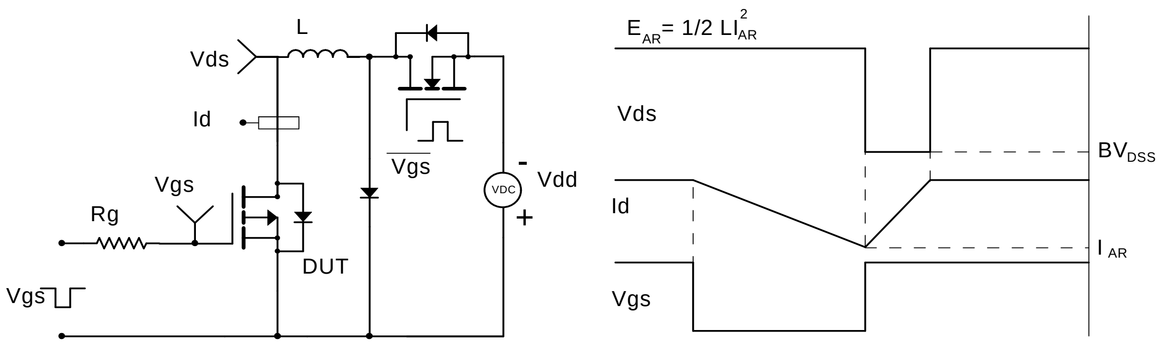
## Gate Charge Test Circuit & Waveform




## Resistive Switching Test Circuit & Waveforms




## Unclamped Inductive Switching (UIS) Test Circuit & Waveforms




## Diode Recovery Test Circuit & Waveforms