RHF1401

Rad-hard 14-bit 30 Msps A/D converter

Features

- Qml-V qualified, smd 5962-06260
- Rad hard: 300 kRad(Si) TID
- Failure immune (SEFI) and latchup immune (SEL) up to 120 MeV-cm^2/mg at 2.7 V and 125° C
- Hermetic package
- Tested at F_s = 20 Msps
- Low power: 85 mW at 20 Msps
- Optimized for 2 Vpp differential input
- High linearity and dynamic performances
- 2.5 V/3.3 V compatible digital I/O
- Internal reference voltage with external reference option

Ceramic SO-48 package

The upper metallic lid is not electrically connected to any pins, nor to the IC die inside the package.

Applications

- Digital communication satellites
- Space data acquisition systems
- Aerospace instrumentation
- Nuclear and high-energy physics

Description

The RHF1401 is a 14-bit analog-to-digital converter that uses pure (ELDRS-free) CMOS 0.25 µm technology combining high performance, radiation robustness and very low power consumption. The RHF1401 is based on a pipeline structure and digital error correction to provide excellent static linearity. Specifically designed to optimize power consumption, the RHF1401 only dissipates 85 mW at 20 Msps, while maintaining a high level of performance. The device integrates a proprietary track-and-hold structure to ensure a large effective resolution bandwidth. Voltage references are integrated in the circuit to simplify the design and minimize external components. A tri-state capability is available on the outputs to allow common bus sharing. A data-ready signal, which is raised when the data is valid on the output, can be used for synchronization purposes. The RHF1401 has an operating temperature range of -55° C to +125° C and is available in a small 48-pin ceramic SO-48 package.

Contents

1 Block diagram . . . 3

2 Pin connections . . . 4

3 Pin descriptions . . . 5

4 Equivalent circuits . . . 6

5 Timing characteristics . . . 8

5.1 Digital output load considerations . . . 9

6 Absolute maximum ratings and operating conditions . . . 10

7 Electrical characteristics (after 300 kRad) . . . 11

7.1 Operating modes . . . 19

7.1.1 Digital inputs . . . 19

7.1.2 Digital outputs . . . 19

7.2 Driving the analog input . . . 20

7.3 Reference connection . . . 24

7.3.1 Internal reference . . . 24

7.3.2 External reference . . . 24

7.4 Clock input . . . 26

7.5 Power consumption optimization . . . 27

7.6 PCB layout precautions . . . 28

8 Definitions of specified parameters . . . 29

8.1 Static parameters . . . 29

8.2 Dynamic parameters . . . 29

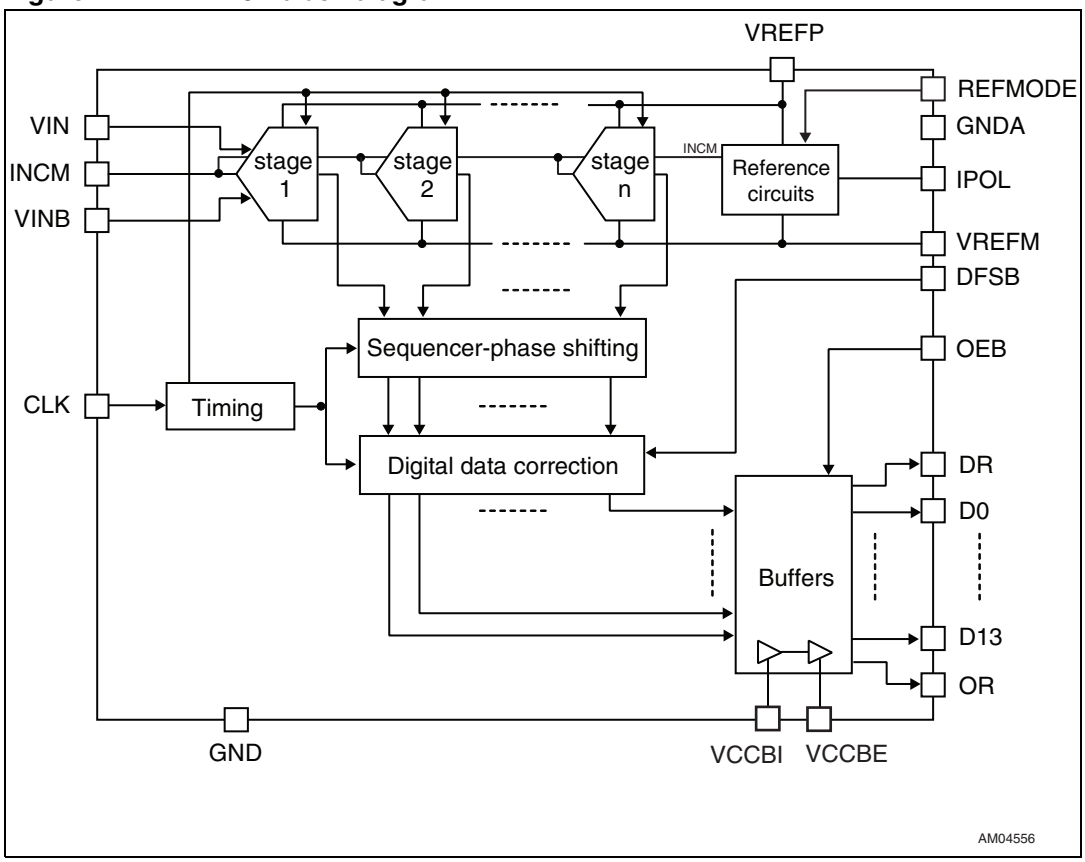
9 Package information . . . 30

10 Ordering information . . . 32

11 Revision history . . . 33

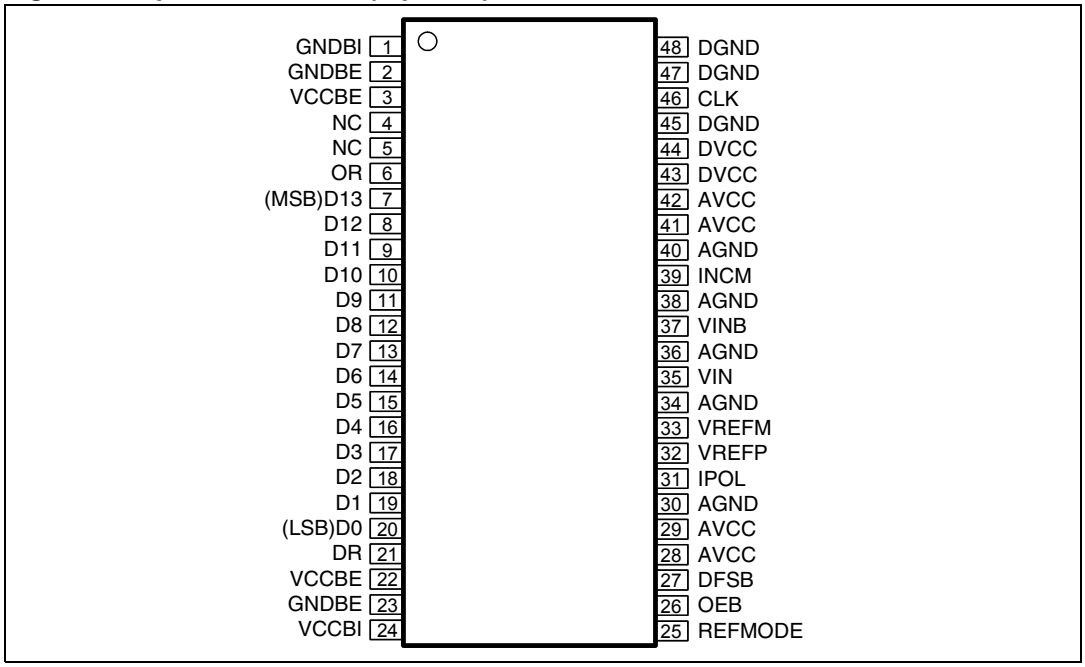
1 Block diagram

Figure 1. RHF1401 block diagram



2 Pin connections

Figure 2. pin connections (top view)



3 Pin descriptions

Table 1. Pin descriptions

Pin	Name	Description	Observations	Pin	Name	Description	Observations
1	GNDBI	Digital buffer ground	0 V	25	REFMODE	Ref. mode control input	2.5 V/3.3 V CMOS input
2	GNDBE	Digital buffer ground	0 V	26	OEB	Output enable input	2.5 V/3.3 V CMOS input
3	VCCBE	Digital buffer power supply	2.5 V/3.3 V	27	DFSB	Data format select input	2.5 V/3.3 V CMOS input
4		NC	Not connected to the dice	28	AVCC	Analog power supply	2.5 V
5		NC	Not connected to the dice	29	AVCC	Analog power supply	2.5 V
6	OR	Out of range output	CMOS output (2.5 V/3.3 V)	30	AGND	Analog ground	0 V
7	D13(MSB)	Most significant bit output	CMOS output (2.5 V/3.3 V)	31	IPOL	Analog bias current input	
8	D12	Digital output	CMOS output (2.5 V/3.3 V)	32	VREFP	Top voltage reference	Can be external or internal
9	D11	Digital output	CMOS output (2.5 V/3.3 V)	33	VREFM	Bottom voltage reference	0 V
10	D10	Digital output	CMOS output (2.5 V/3.3 V)	34	AGND	Analog ground	0 V
11	D9	Digital output	CMOS output (2.5 V/3.3 V)	35	VIN	Analog input	1 V_{pp}
12	D8	Digital output	CMOS output (2.5 V/3.3 V)	36	AGND	Analog ground	0 V
13	D7	Digital output	CMOS output (2.5 V/3.3 V)	37	VINB	Inverted analog input	1 V_{pp}
14	D6	Digital output	CMOS output (2.5 V/3.3 V)	38	AGND	Analog ground	0 V
15	D5	Digital output	CMOS output (2.5 V/3.3 V)	39	INCM	Input common mode	Can be external or internal
16	D4	Digital output	CMOS output (2.5 V/3.3 V)	40	AGND	Analog ground	0 V
17	D3	Digital output	CMOS output (2.5V /3.3 V)	41	AVCC	Analog power supply	2.5 V
18	D2	Digital output	CMOS output (2.5 V/3.3 V)	42	AVCC	Analog power supply	2.5 V
19	D1	Digital output	CMOS output (2.5 V/3.3 V)	43	DVCC	Digital power supply	2.5 V
20	D0(LSB)	Digital output LSB	CMOS output (2.5 V/3.3 V)	44	DVCC	Digital power supply	2.5 V
21	DR	Data ready output(1)	CMOS output (2.5 V/3.3 V)	45	DGND	Digital ground	0 V
22	VCCBE	Digital buffer power supply	2.5 V/3.3 V	46	CLK	Clock input	2.5 V compatible CMOS input
23	GNDBE	Digital buffer ground	0 V	47	DGND	Digital ground	0 V
24	VCCBI	Digital buffer power supply	2.5 V	48	DGND	Digital ground	0 V

1. See load considerations in *Chapter 5: Timing characteristics*.

4 Equivalent circuits

Figure 3. Analog inputs

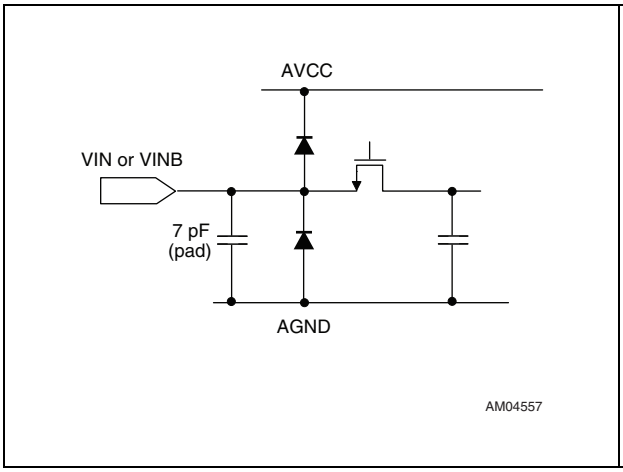


Figure 4. Output buffers

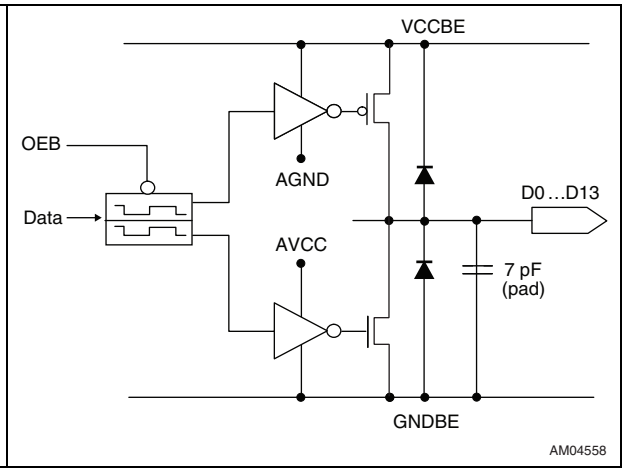


Figure 5. Clock input

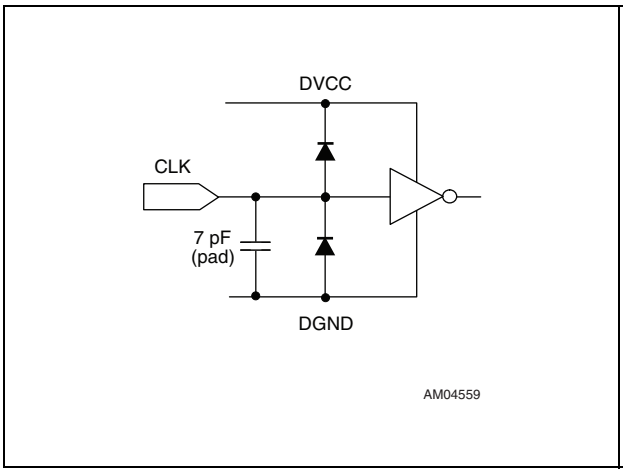


Figure 6. Data format input

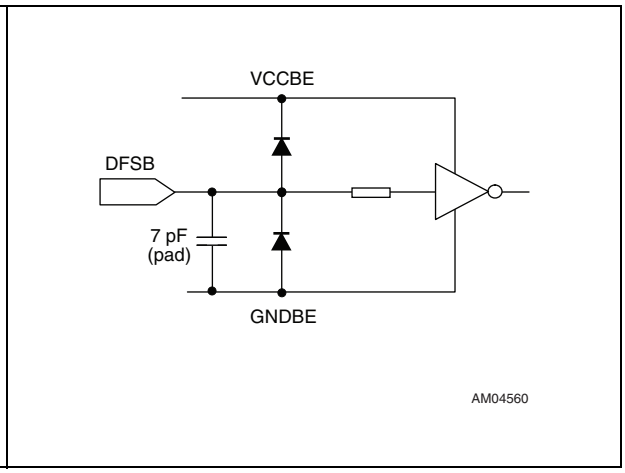


Figure 7. Reference mode control input

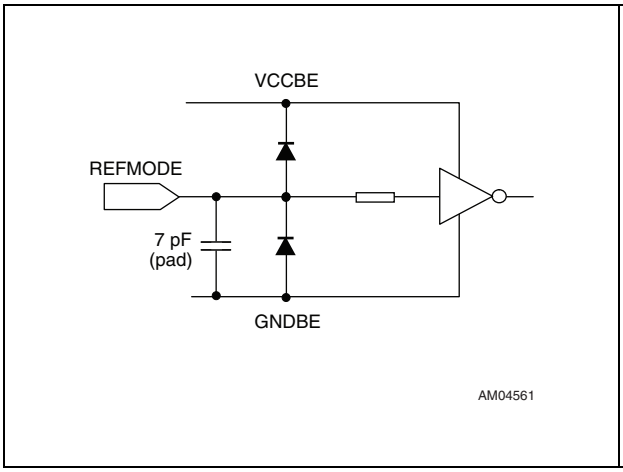


Figure 8. Output enable input

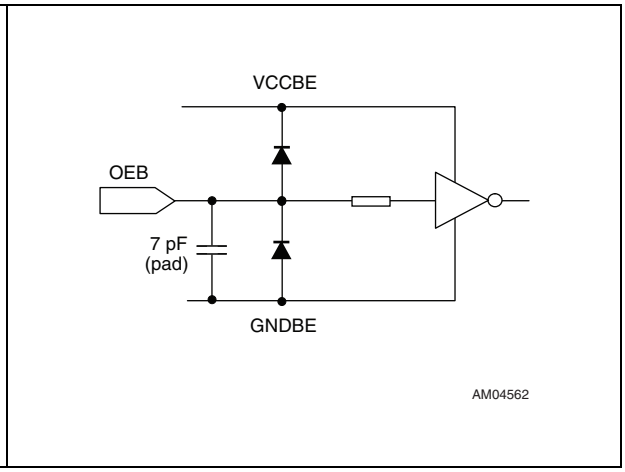


Figure 9. VREFP and INCM input

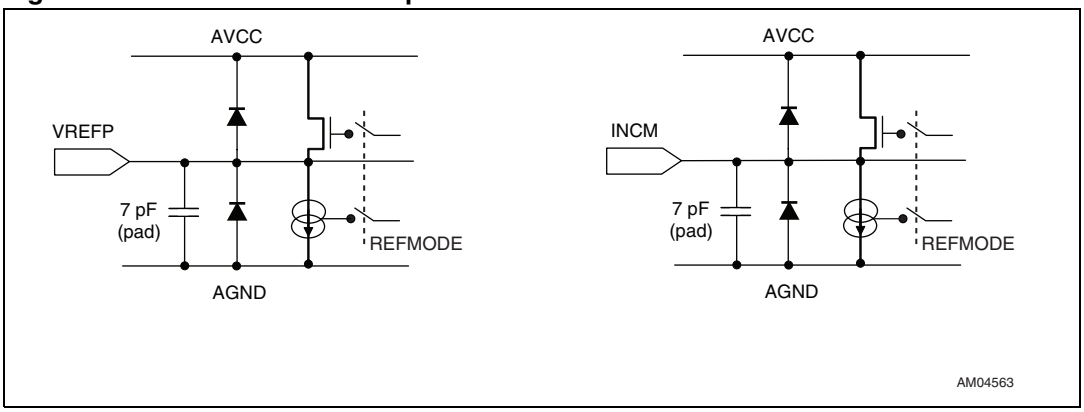
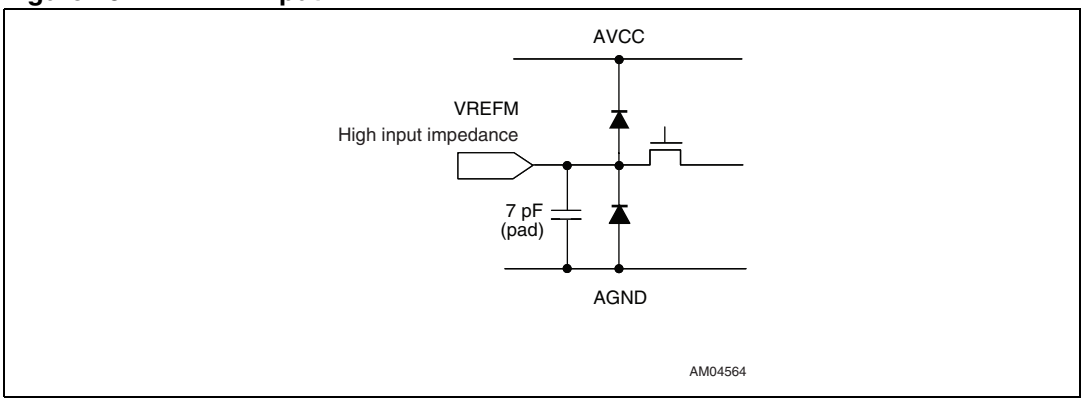


Figure 10. VREFM input



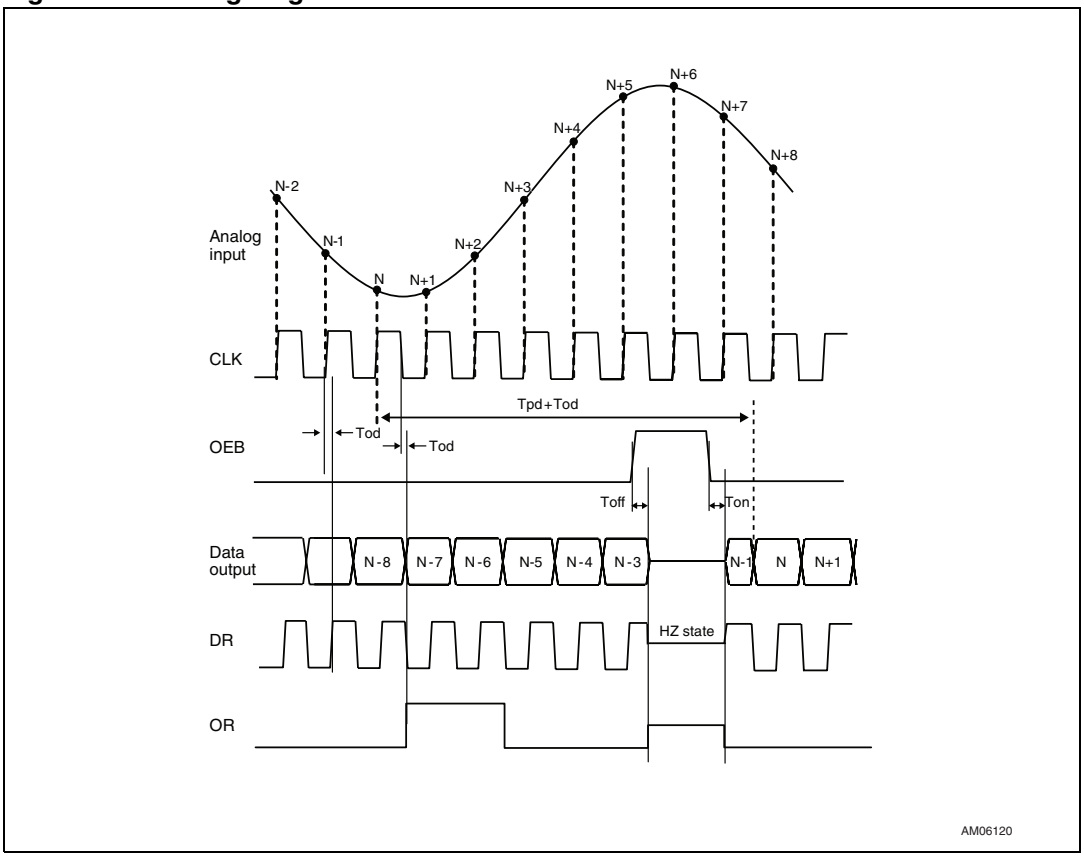
5 Timing characteristics

Table 2. Timing characteristics

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
DC	Clock duty cycle	F_s = 20 Msps	45	50	65	%
T_{od}	Data output delay (fall of clock to data valid) (1)	10 pF load capacitance	5	7.5	13	ns
T_{pd}	Data pipeline delay(2)	Duty cycle = 50%	7.5	7.5	7.5	cycles
T_{on}	Falling edge of OEB to digital output valid data			1		ns
T_{off}	Rising edge of OEB to digital output tri-state			1		ns
T_{rD}	Data rising time	10 pF load capacitance		6		ns
T_{fD}	Data falling time	10 pF load capacitance		3		ns

1. As per *Figure 11*.
2. If the duty cycle does not equal 50%: T_{pd} = 7 cycles + CLK pulse width.

Figure 11. Timing diagram



The input signal is sampled on the rising edge of the clock while the digital outputs are synchronized on the falling edge of the clock. The duty cycles on DR and CLK are the same.

The rising and falling edges of the OR pin are synchronized with the falling edge of the DR pin.

5.1 Digital output load considerations

The features of the internal output buffers limit the maximum load on the digital data output. In particular, the shape and amplitude of the Data Ready signal, toggling at the clock frequency, can be weakened by a higher equivalent load.

In applications that impose higher load conditions, it is recommended to use the falling edge of the master clock instead of the Data Ready signal. This is possible because the output transitions are internally synchronized with the falling edge of the clock.

Figure 12. Output buffer fall time

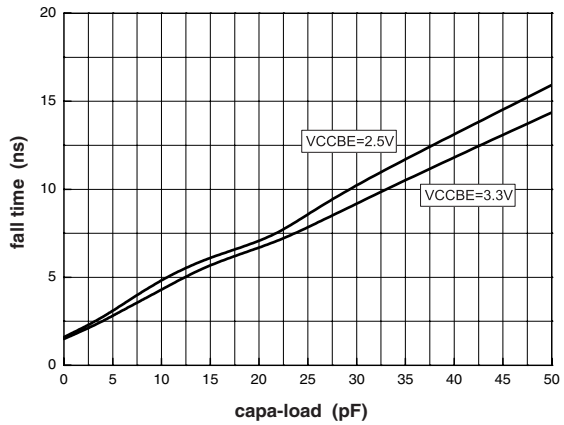
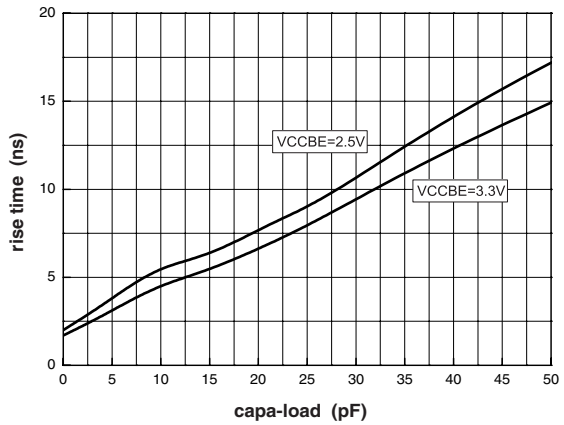


Figure 13. Output buffer rise time



6 Absolute maximum ratings and operating conditions

Table 3. Absolute maximum ratings

Symbol	Parameter	Values	Unit
AV_{CC}	Analog supply voltage	3.3	V
DV_{CC}	Digital supply voltage	3.3	V
V_{CCBI}	Digital buffer supply voltage	3.3	V
V_{CCBE}	Digital buffer supply voltage	3.6	V
V_{IN} V_{INB}	Analog inputs: bottom limit –> top limit	-0.6 V –> AV_{CC}+0.6 V	V
V_{REFP} V_{INCM}	External references: bottom limit –> top limit	-0.6 V –> AV_{CC}+0.6 V	V
I_{Dout}	Digital output current	-100 to 100	mA
T_{stg}	Storage temperature	-65 to +150	°C
R_{thjc}	Thermal resistance junction to case	22	°C/W
R_{thja}	Thermal resistance junction to ambient	125	°C/W
ESD	HBM (human body model)(1)	2	kV

1. Human body model: a 100 pF capacitor is charged to the specified voltage, then discharged through a 1.5 kΩ resistor between two pins of the device. This is done for all couples of connected pin combinations while the other pins are floating.

Table 4. Operating conditions

Symbol	Parameter	Min	Typ	Max	Unit
AV_{CC}	Analog supply voltage	2.3	2.5	2.7	V
DV_{CC}	Digital supply voltage	2.3	2.5	2.7	V
V_{CCBI}	Digital internal buffer supply	2.3	2.5	2.7	V
V_{CCBE}	Digital output buffer supply	2.3	2.5	3.4	V
V_{REFP}	Forced top voltage reference	0.8		1.4	V
V_{REFM}	Bottom internal reference voltage	0	0	0.5	V
V_{INCM}	Forced common mode voltage	0.2		1.1	V
V_{IN}	V_{IN} max. voltage versus GND		1.6		V
	V_{IN} min. voltage versus GND		-0.2		V
V_{INB}	V_{INB} max. voltage versus GND		1.6		V
	V_{INB} min. voltage versus GND		-0.2		V
DFSB	Digital inputs (see *Table 9* for thresholds)	0		V_{CCBE}	V
REFMODE					
OEB					

7 Electrical characteristics (after 300 kRad)

Unless otherwise specified, the test conditions in the following tables are:
AV_{CC} = DV_{CC} = V_{CCBI} =V_{CCBE} = 2.5 V, F_s=20 Msps, F_{IN}= 15 MHz, V_{IN} at -1 dBFS, V_{REFM} = 0 V, T_{amb} = 25°C.

Table 5. Analog inputs

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{IN}-V_{INB}	Full-scale reference voltage (FS)(1)	V_{REFP} = 1 V (forced)		2		V_{pp}
C_{IN}	Input capacitance			7		pF
Z_{IN}	Input impedance	F_s = 20 Msps		3.3		kΩ
ERB	Effective resolution bandwidth(1)			70		MHz

1. See *Chapter 8: Definitions of specified parameters on page 29* for more information.

Table 6. Internal reference voltage

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
R_{out}	Output resistance of internal reference	REFMODE = 0 internal reference on		30		Ω
		REFMODE = 1 internal reference off		7.5		kΩ
V_{REFP}	Top internal reference voltage(1)	REFMODE = 0	0.76	0.84	0.95	V
V_{INCM}	Input common mode voltage	REFMODE = 0	0.40	0.44	0.50	V

1. V_{REFM} connected to GND.

Table 7. External reference voltage(1)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{REFP}	Forced top reference voltage	REFMODE = 1	0.8		1.4	V
V_{REFM}	Forced bottom ref voltage	REFMODE = 1	0		0.5	V
V_{INCM}	Forced common mode voltage	REFMODE = 1	0.2		1.1	V

1. See *Figure 14*.

Table 8. Static accuracy

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
DNL	Differential non-linearity(1)	F_{in} = 1.5 Msps V_{in} at -1 dBFS F_s = 1.5 Msps		±0.4		LSB
INL	Integral non-linearity(2)			±3		LSB
	Monotonicity and no missing codes		Guaranteed			

1. See *Figure 33* and *Chapter 8* for more information. This parameter is not tested.
2. See *Figure 34* and *Chapter 8* for more information. This parameter is not tested.

Table 9. Digital inputs and outputs

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
Clock input						
CT	Clock threshold	DV_{CC} = 2.5 V		1.25		V
CA	Square clock amplitude (DC component = 1.25 V)	DV_{CC} = 2.5 V	0.8		2.5	Vp-p
Digital inputs						
V_{IL}	Logic "0" voltage	V_{CCBE} = 2.5 V	0		0.25 x V_{CCBE}	V
V_{IH}	Logic "1" voltage	V_{CCBE} = 2.5 V	0.75 x V_{CCBE}		V_{CCBE}	V
Digital outputs						
V_{OL}	Logic "0" voltage	I_{OL} = -10 µA		0	0.25	V
V_{OH}	Logic "1" voltage	I_{OH} = 10 µA	V_{CCBE} -0.25			V
I_{OZ}	High impedance leakage current	OEB set to V_{IH}	-15		15	µA
C_L	Output load capacitance	High CLK frequencies			15	pF

Table 10. Dynamic characteristics

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
SFDR	Spurious free dynamic range	F_{in} = 15 MHz F_s = 20 Msps V_{in} at -1 dBFS internal references C_L = 6 pF	70	91		dBFS
SNR	Signal to noise ratio		66	70		dB
THD	Total harmonic distortion		70	86		dB
SINAD	Signal to noise and distortion ratio		65	70		dB
ENOB	Effective number of bits		10.6	11.5		bits

Higher values of SNR, SINAD and ENOB can be obtained by increasing the full-scale range of the analog input. This is illustrated in *Figure 51* and *Figure 52* with V_{REFP} = 1.25 V.

Figure 14. Differential input configuration

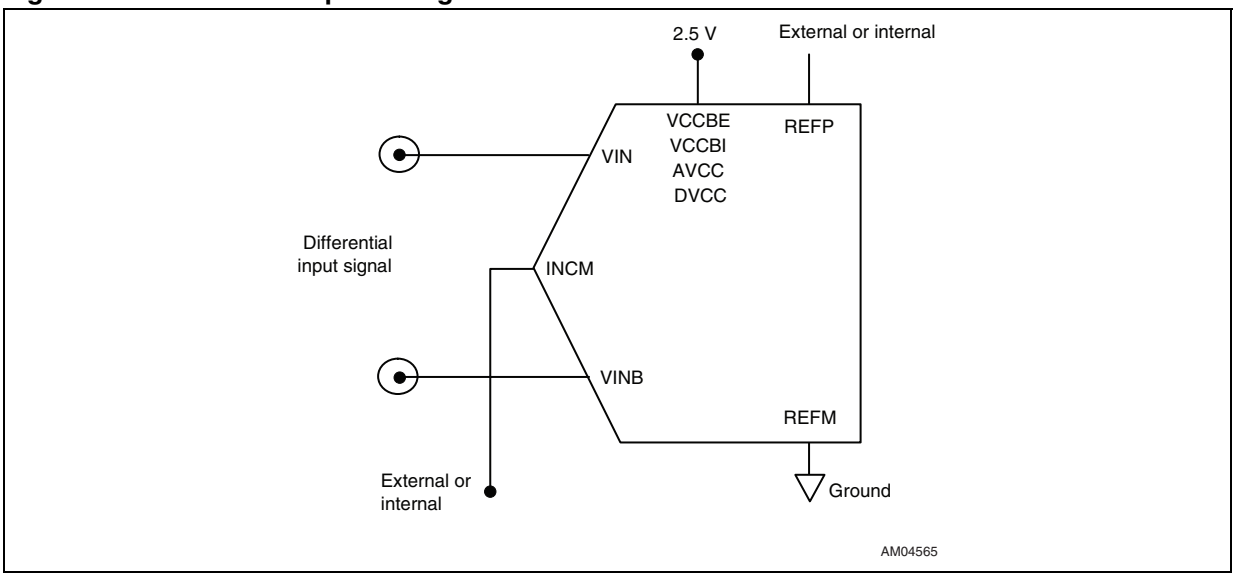


Figure 15. ENOB vs. input freq., square clock

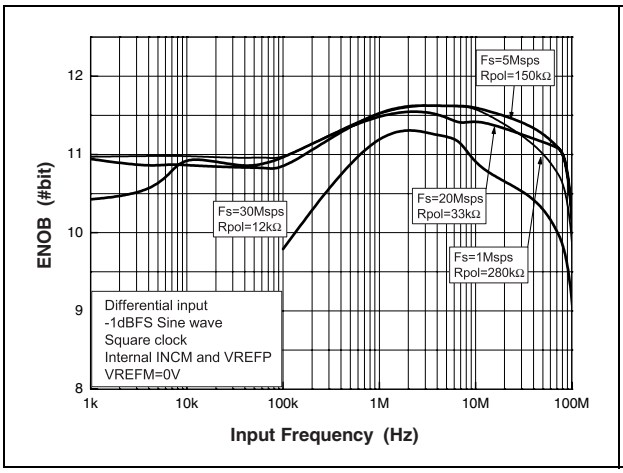


Figure 16. SINAD vs. input freq., square clock

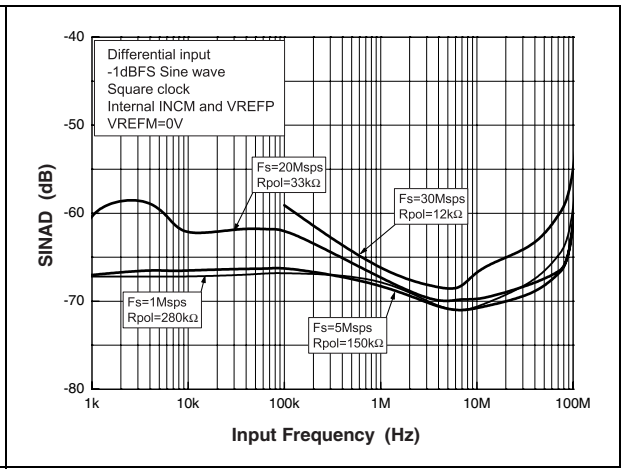


Figure 17. THD vs. input freq., square clock

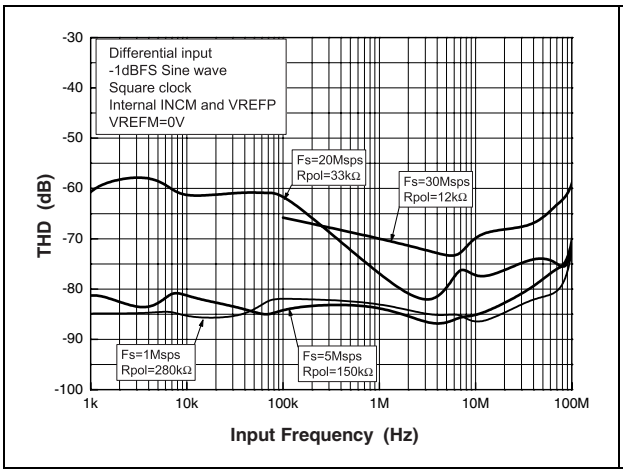


Figure 18. SNR vs. input freq., square clock

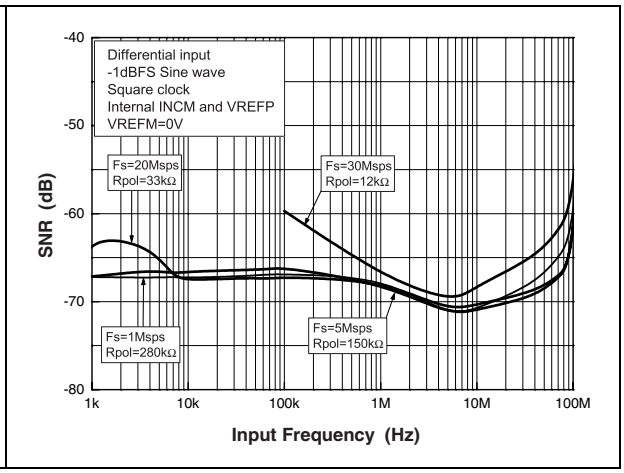


Figure 19. SFDR vs. input freq., square clock

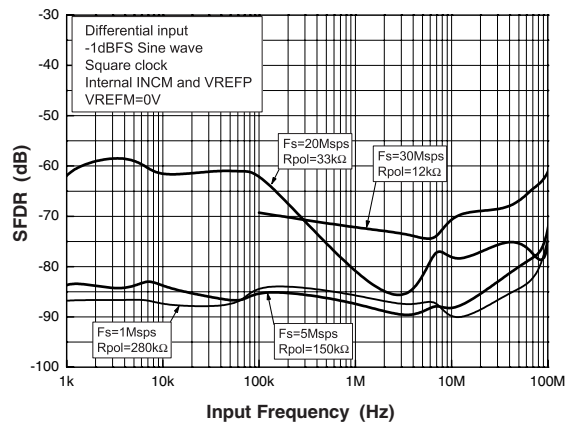


Figure 20. ENOB vs. V_{CC}BE

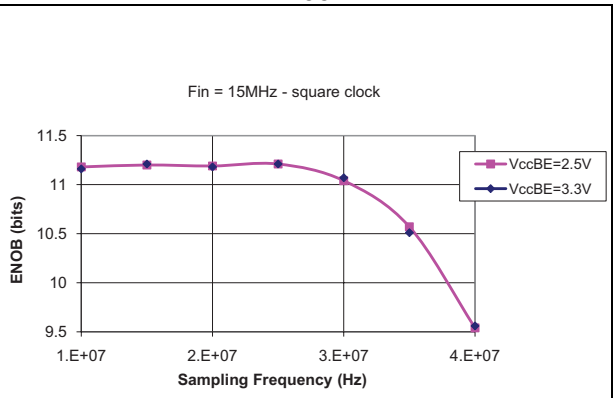


Figure 21. ENOB vs. input freq., ext. ref.

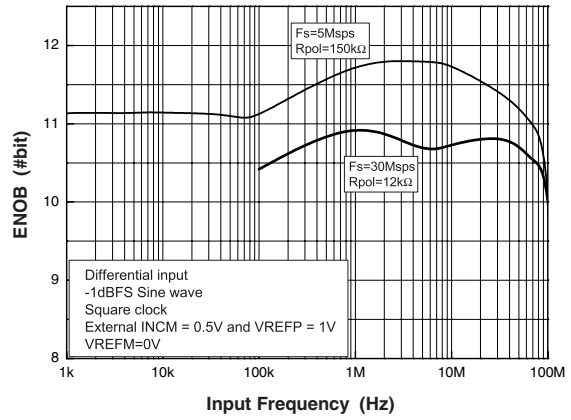


Figure 22. ENOB vs. REFP

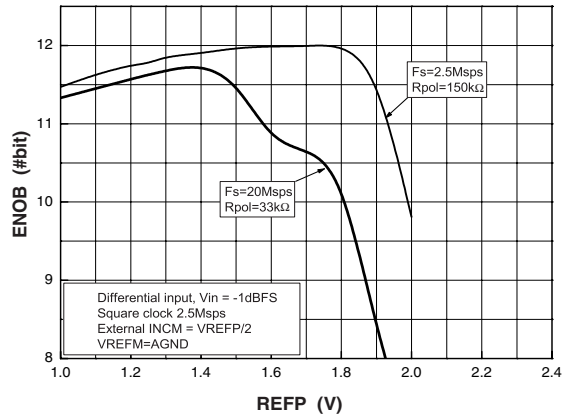


Figure 23. ENOB vs. clock duty cycle

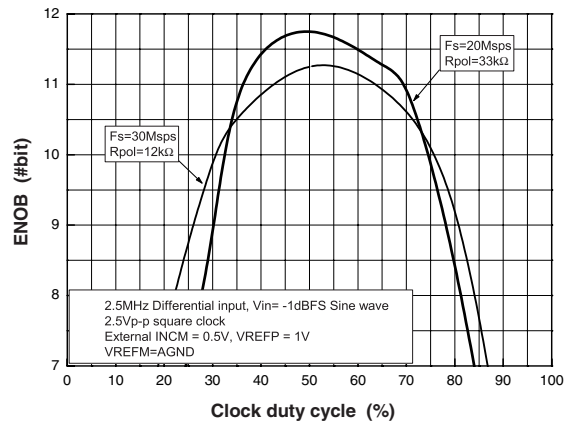


Figure 24. ENOB vs. INCM

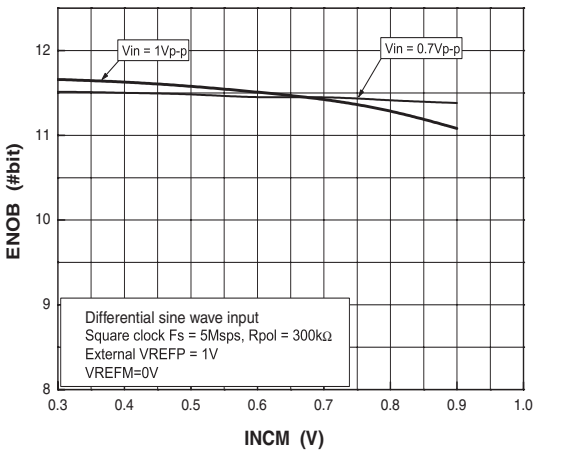


Figure 25. ENOB vs. Vin

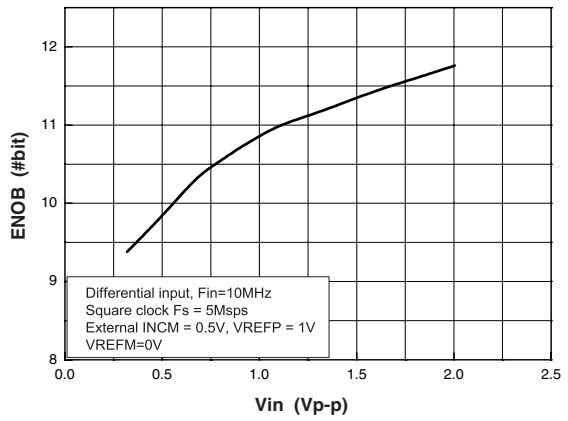


Figure 26. ENOB vs. square clock, diff. input

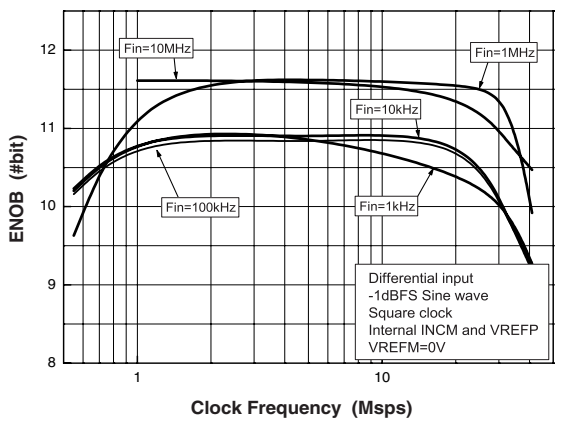


Figure 27. SFDR vs. square clock, diff. input

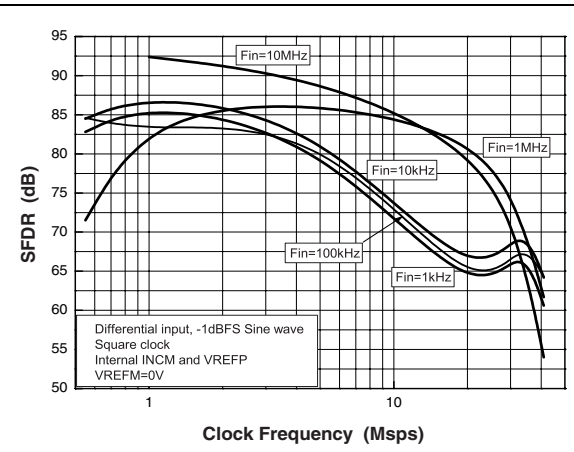


Figure 28. SINAD vs. square clock, diff. input

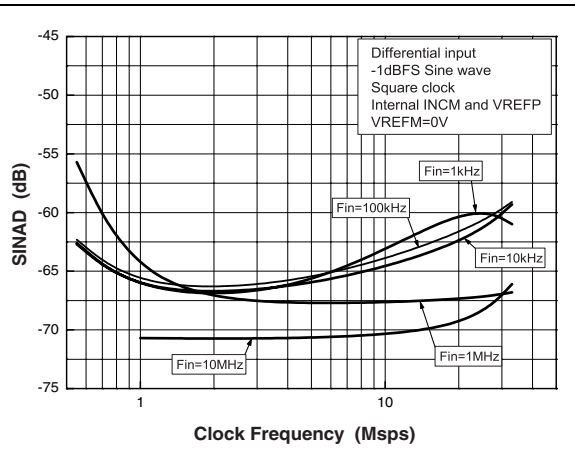


Figure 29. THD vs. square clock, diff. input

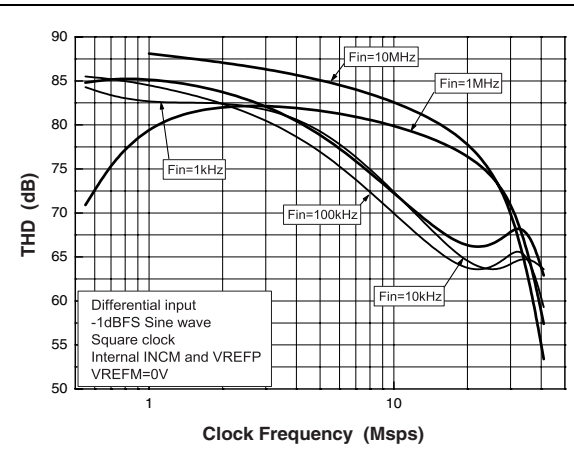


Figure 30. SNR vs. square clock, diff. input

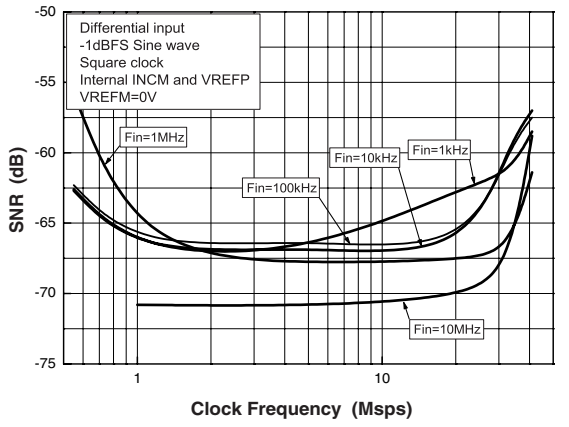


Figure 31. ENOB vs. sine clock, diff. input

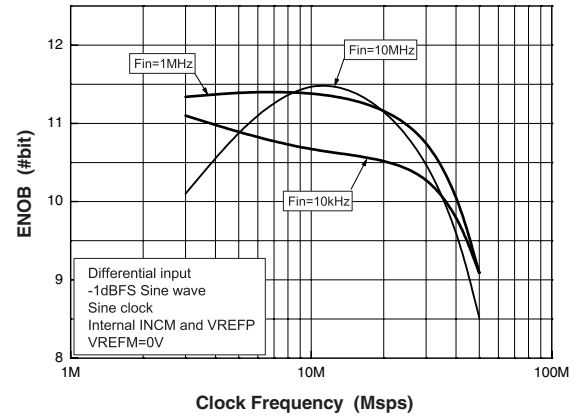


Figure 32. Clock threshold vs. temperature

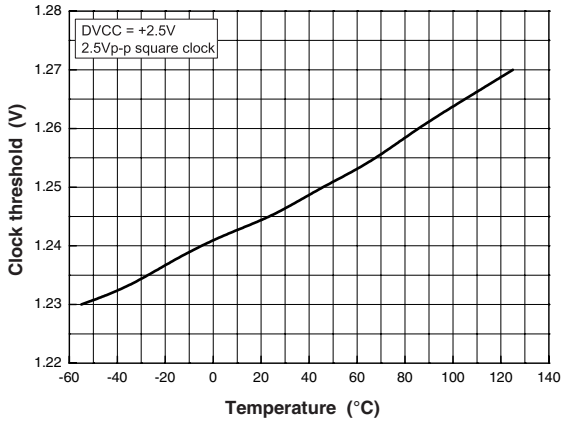


Figure 33. DNL, differential input

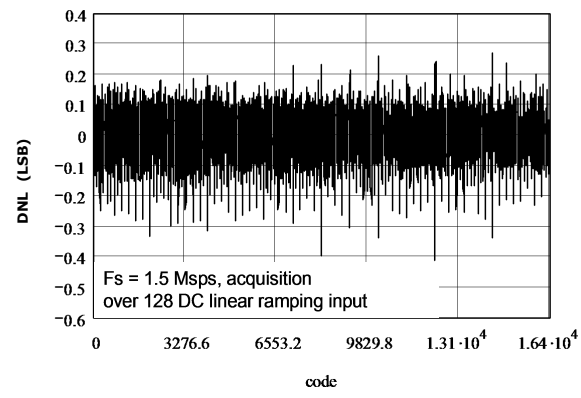


Figure 34. INL, differential input

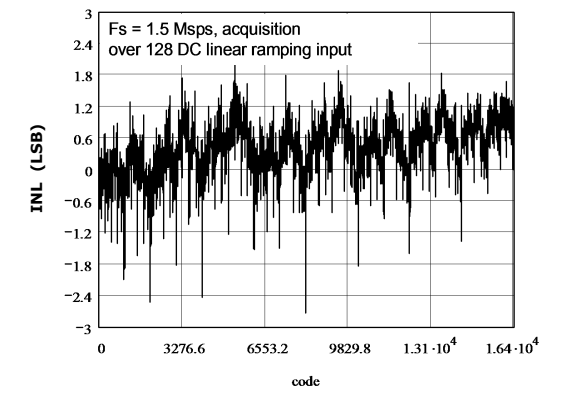


Figure 35. Single-ended input configuration

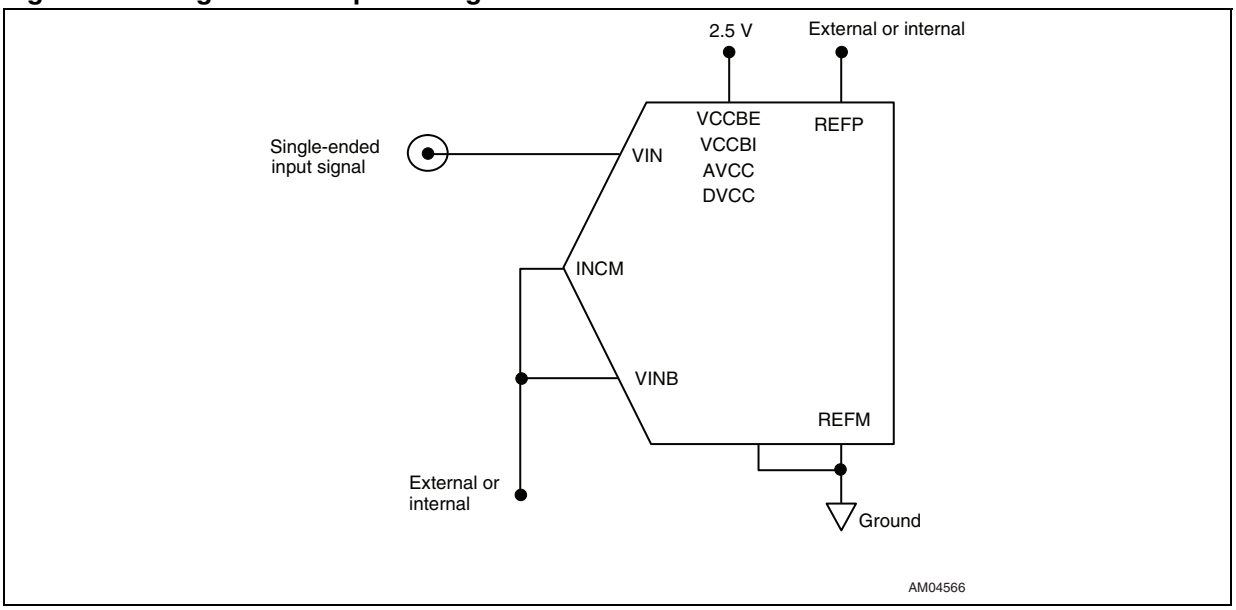


Figure 36. ENOB vs. Fin, single-ended

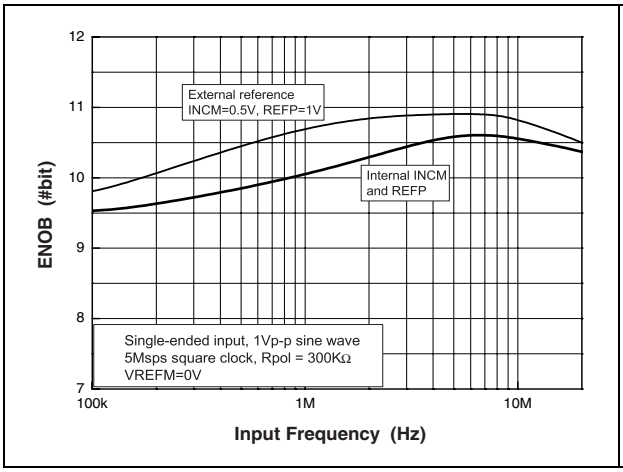


Figure 37. SINAD vs. Fin, single-ended

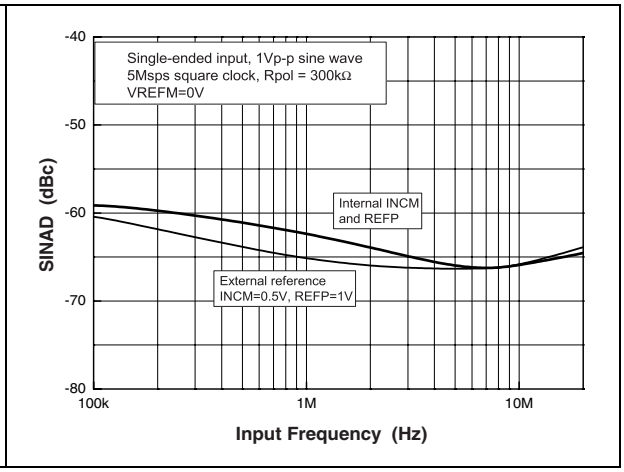


Figure 38. THD vs. Fin, single-ended

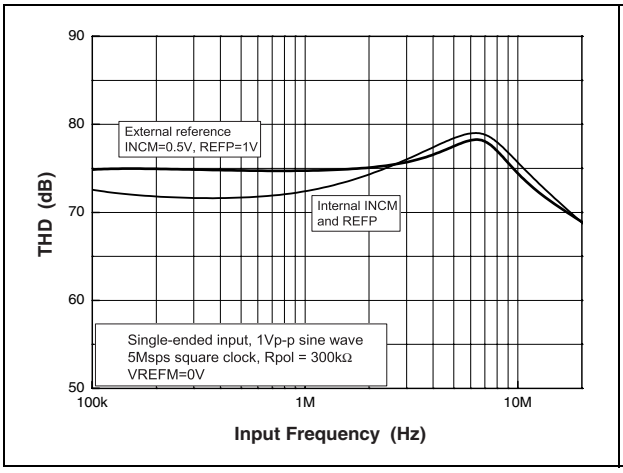


Figure 39. SNR vs. Fin, single-ended

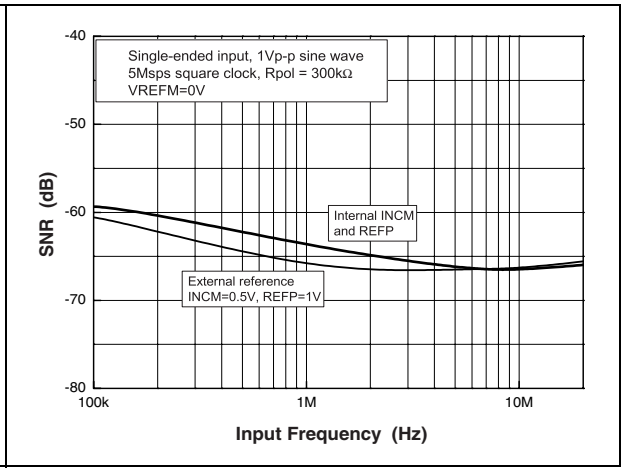
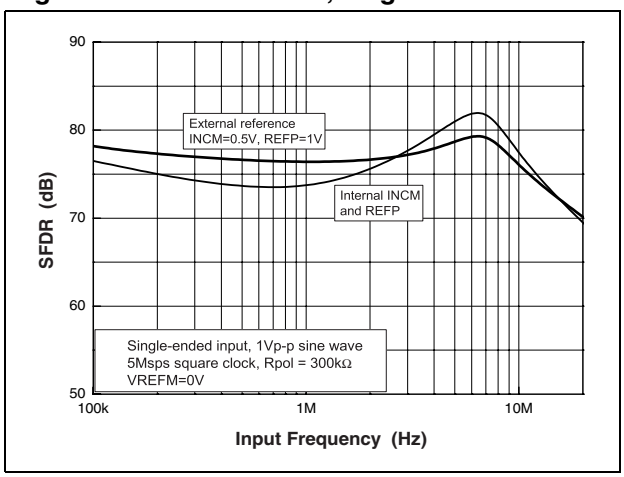


Figure 40. SFDR vs. Fin, single-ended



7.1 Operating modes

Extra functionalities are provided to simplify the application board as much as possible. The operating modes offered by the RHF1401 are described in *Table 11*.

Table 11. RHF1401 operating modes

Inputs			Outputs		
Analog input differential amplitude	**DFSB**	**OEB**	**OR**	**DR**	**Most significant bit (MSB)**
(V_{IN}-V_{INB}) above maximum range	H	L	H	CLK	D13
	L	L	H	CLK	D13 complemented
(V_{IN}-V_{INB}) below minimum range	H	L	H	CLK	D13
	L	L	H	CLK	D13 complemented
(V_{IN}-V_{INB}) within range	H	L	L	CLK	D13
	L	L	L	CLK	D13 complemented
X	X	H	HZ (1)	HZ	HZ (all digital outputs are in high impedance)

1. High impedance.

7.1.1 Digital inputs

Data format select bit (DFSB): when set to low level (V_{IL}), the digital input DFSB provides a two's complement digital output MSB. This can be of interest when performing some further signal processing. When set to high level (V_{IH}), DFSB provides standard binary output coding.

Output enable bit (OEB): when set to low level (V_{IL}), all digital outputs remain active. When set to high level (V_{IH}), all digital output buffers are in a high impedance state while the converter goes on sampling. When OEB is set to a low level again, the data arrives on the output with a very short T_{on} delay. This feature enables the chip select of the device. *Figure 11 on page 8* summarizes this functionality.

Reference mode control (REFMODE): this allows the internal or external settings of the voltage references VREFP and INCM. REFMODE = 0 for internal references, REFMODE = 1 for external references (and disables both references VREFP and INCM).

7.1.2 Digital outputs

Out of range (OR): this function is implemented on the output stage in order to set an "out-of-range" flag whenever the digital data is over the full-scale range. Typically, there is a detection of all data at '0' or all data at '1'. It sets an output signal OR, which is in a low level state (V_{OL}) when the data stays within the range, or in a high-level state (V_{OH}) when the data is out of range.

Data ready (DR): the Data Ready output is an image of the clock being synchronized on the output data (D0 to D13). This is a very helpful signal that simplifies the synchronization of the measurement equipment or of the controlling DSP. Like all other digital outputs, DR goes into high impedance when OEB is set to a high level, as shown in *Figure 11 on page 8*.

7.2 Driving the analog input

Figure 41. Equivalent VIN - VINB (differential input)

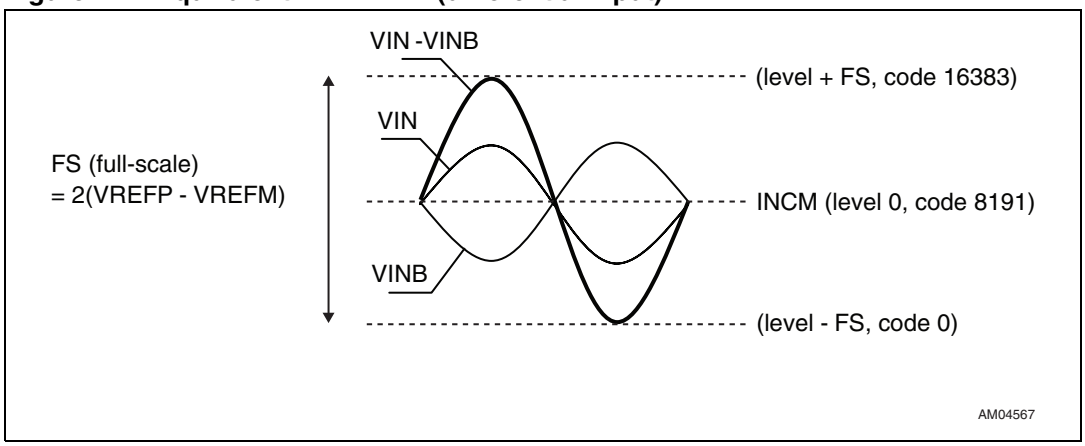


Figure 42. Maximum input swing on each VIN or VINB input

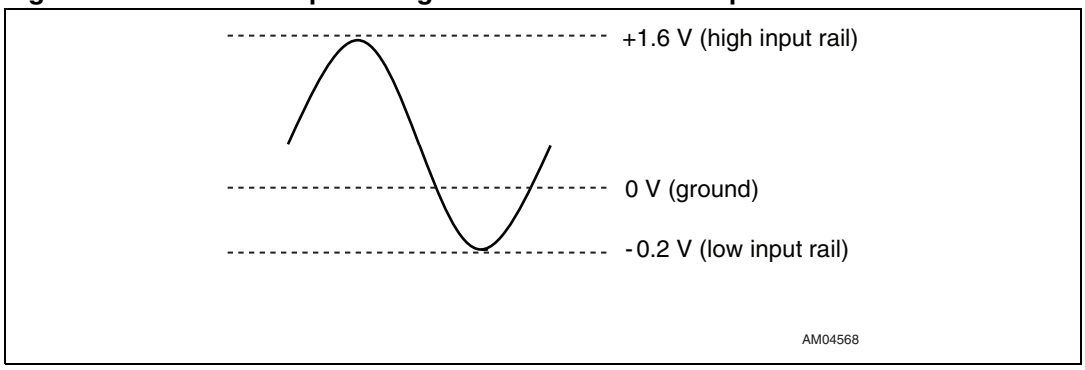


Figure 43. Optimized single-ended configuration (DC coupling), external REFP

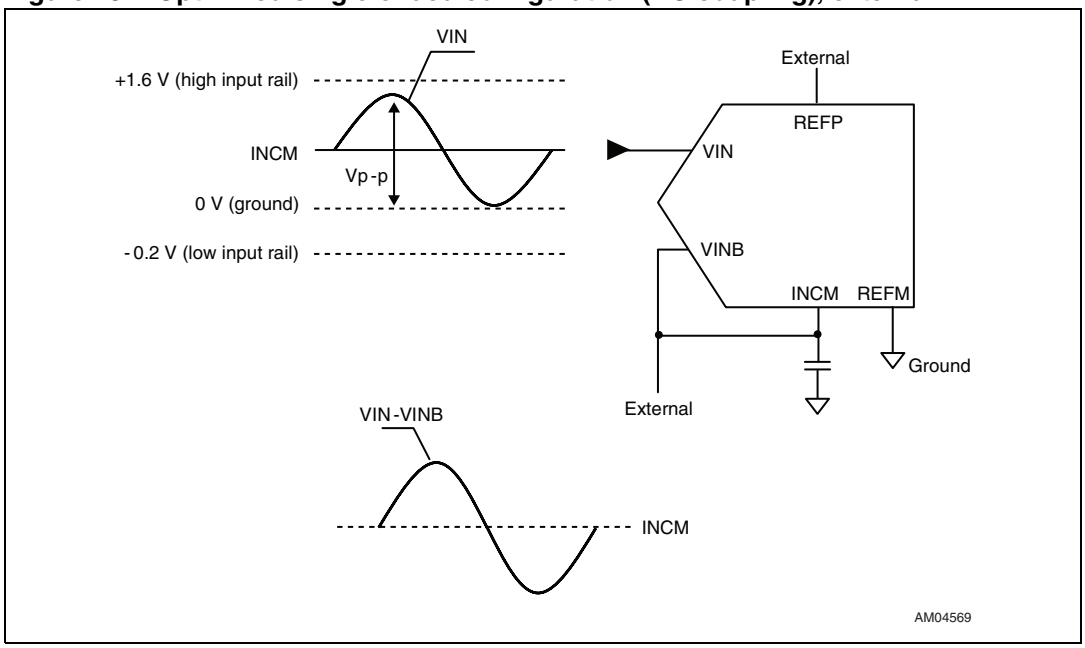
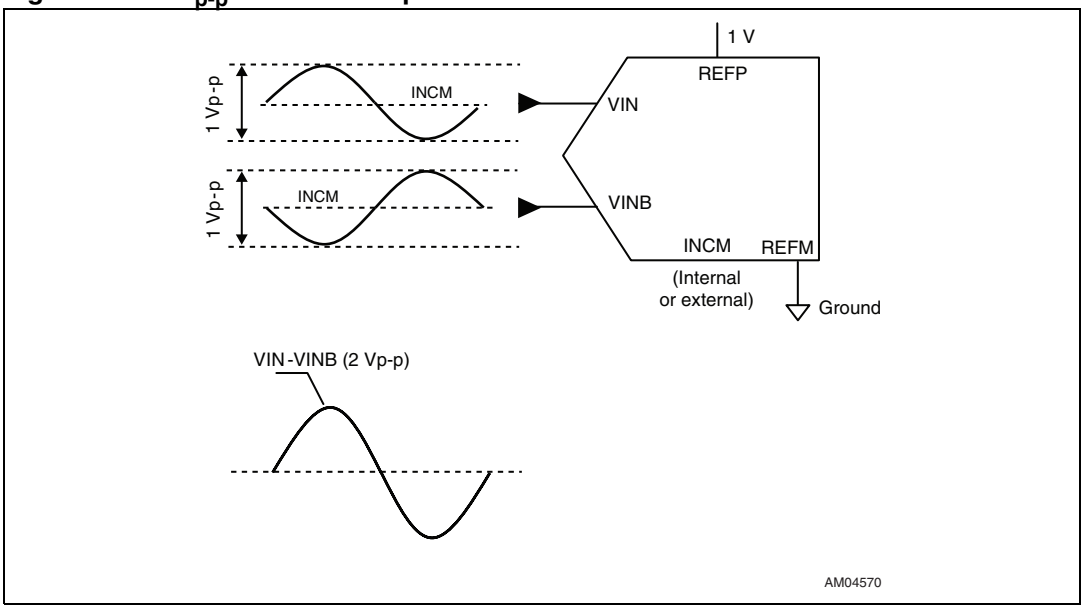


Table 12. Output codes for DFSB = 1

Vin - Vinb	Output code
+ range/2	16383
0	8191
- range/2	0

The RHF1401 is designed for use in a differential input configuration. Nevertheless, it can achieve good performance in a single-ended input configuration. In single-ended, a good quality conversion can be achieved by using an input amplitude up to 1.4 Vp-p by using the external references INCM and VREFP at 0.7 V and 1 V respectively (see *Figure 35 on page 17*).

Figure 44. 2 V_{p-p} differential input



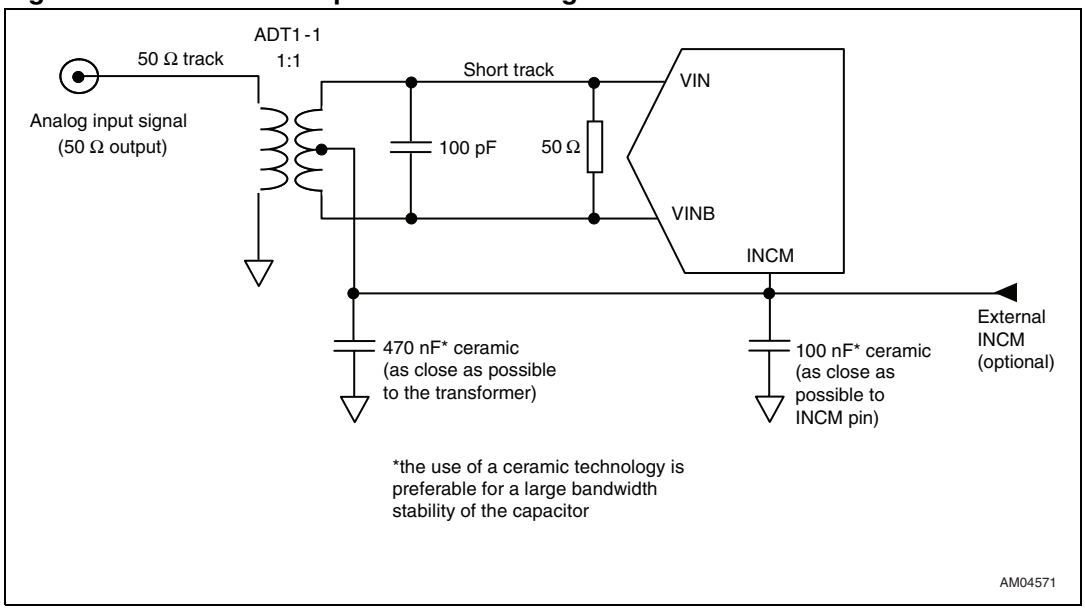
The RHF1401 is designed to obtain optimum performance when driven on differential inputs with a differential amplitude of two volts peak-to-peak (2 V_{p-p}). This is the result of 1 V_{p-p} on the VIN and VINB inputs in phase opposition.

The RHF1401 is specifically designed to meet sampling requirements for intermediate frequency (IF) input signals. In particular, the track-and-hold in the first stage of the pipeline is designed to minimize the linearity limitations as the analog frequency increases. This is achieved by making the input impedance independent of the input frequency.

Figure 45 on page 22 shows a differential input solution. The input signal is fed to the transformer's primary, while the secondary drives both ADC inputs. The transformer must be 50 Ω matched (for proper matching with a 50 Ω generator). Tracks between the secondary and VIN and VINB pins must be as short as possible.

The common-mode voltage of the ADC (INCM) is connected to the center tap of the transformer's secondary in order to bias the input signal around the common voltage (see *Table 6 on page 11*).The INCM is decoupled to maintain a low noise level on this node. Ceramic technology for decoupling provides good capacitor stability across a wide bandwidth.

Figure 45. Differential implementation using a balun



Some applications may require a single-ended input, which can easily be achieved with the configuration shown in *Figure 46*. However, with this type of configuration, a degradation in the rated performance of the RHF1401 may occur, compared with a differential configuration. A sufficiently decoupled DC reference should be used to bias the RHF1401 inputs. An AC-coupled analog input can also be used and the DC analog level set with a high value resistor R (10 kΩ to 100 kΩ) connected to a proper DC source. Cin and R behave like a high-pass filter and are calculated to set the lowest-possible cut-off frequency.

Figure 46. AC-coupling single-ended input configuration

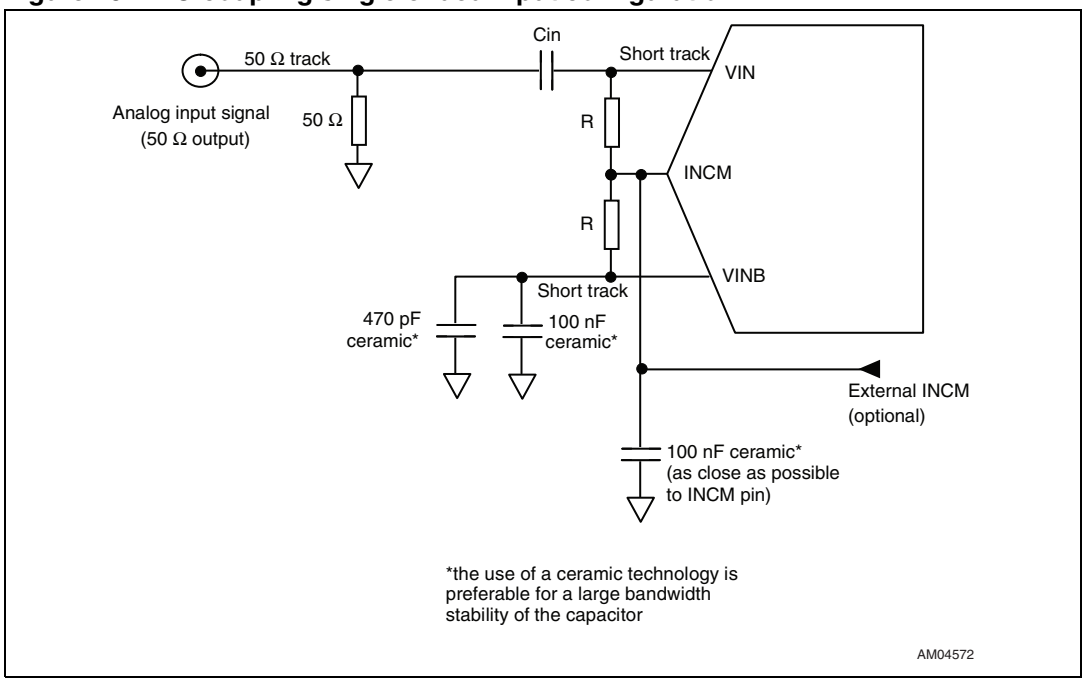
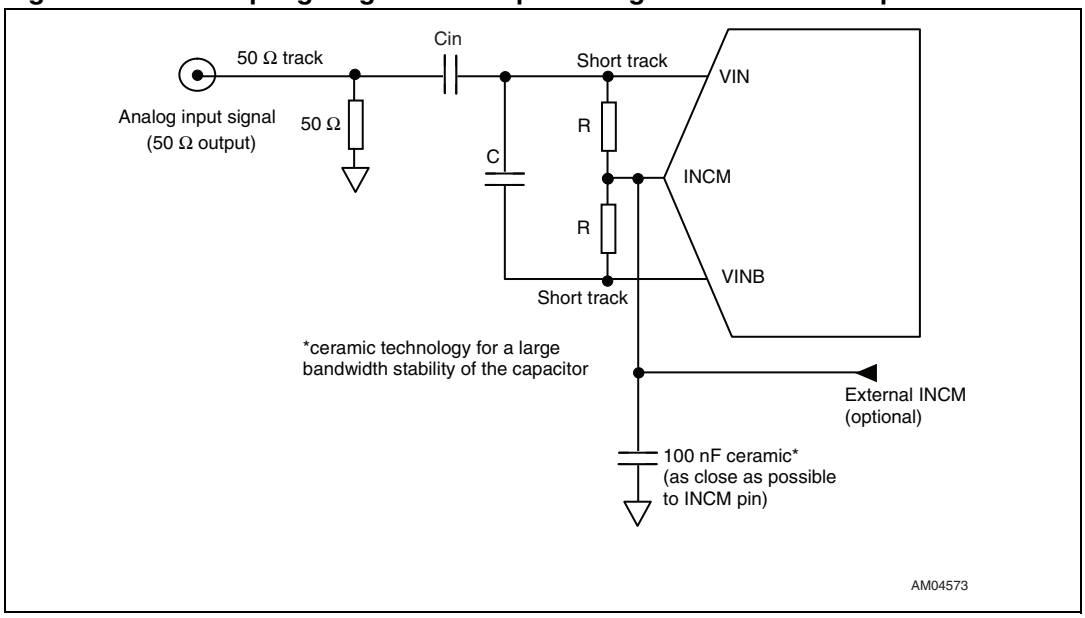


Figure 47. AC-coupling single-ended input configuration for low frequencies



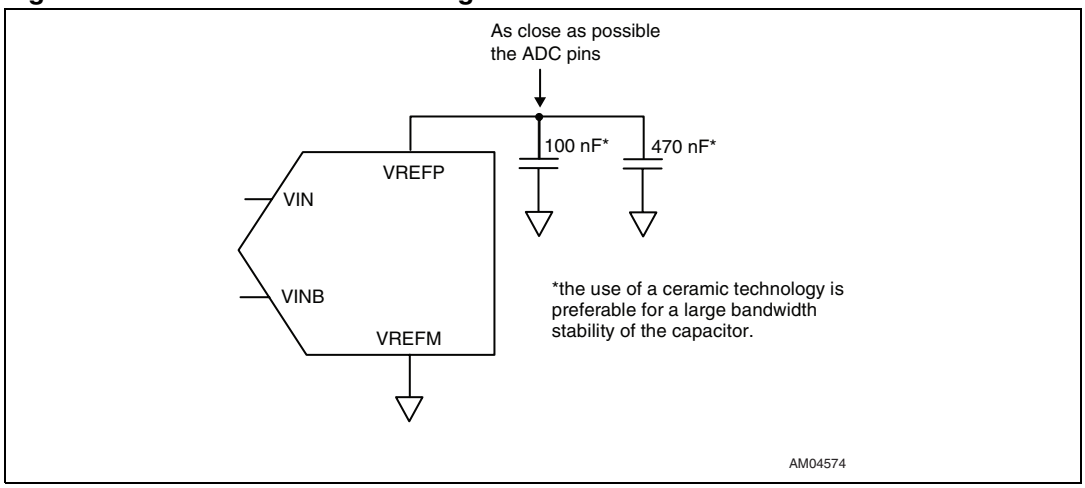
The C capacitor (in the range of 33 pF for example) is dedicated to a low input frequency range. This capacitor is efficient in reducing noise in the higher frequencies. When coupled with the resistors, R and C together behave like a high-pass filter. For example, if R = 10 k and C = 33 pF, the cut-off frequency of this filter equals 482 kHz.

7.3 Reference connection

7.3.1 Internal reference

In the standard configuration, the ADC is biased with the internal reference voltage. The V_{REFM} pin is connected to the analog ground while V_{REFP} is internally set to a voltage close to 1.0 V. V_{REFP} should be decoupled so as to minimize low and high frequency noise. Like V_{REFP}, INCN is internal and can be fixed externally. *Figure 48* shows the schematic.

Figure 48. Internal reference setting



7.3.2 External reference

An external reference voltage can be used for specific applications requiring even better linearity or enhanced temperature behavior (see *Table 6: Internal reference voltage on page 11*). An external voltage reference with the configuration shown in *Figure 49* and *Figure 50* can be used to obtain optimum performance. Decoupling is achieved by using ceramic capacitors, which provide optimum linearity versus frequency.

Figure 49. External reference setting

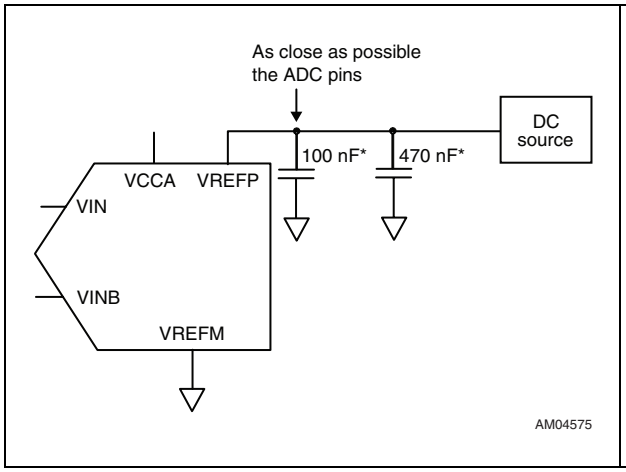
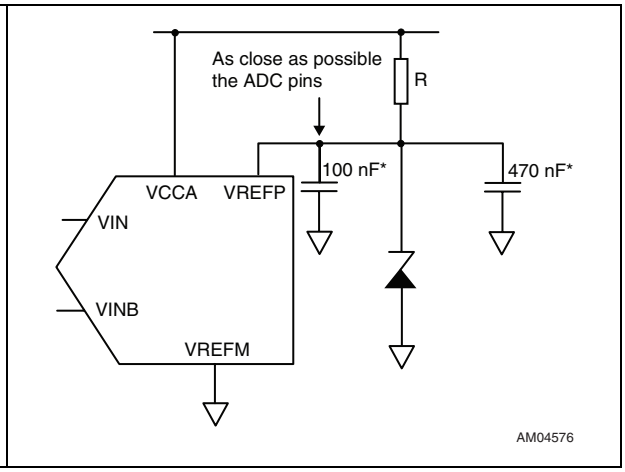


Figure 50. Example with a zener



*Note: * The use of ceramic technology is preferable to ensure large bandwidth stability of the capacitor.*

In multi-channel applications, the high impedance input of the references allows you to drive several ADCs with only one voltage reference device.

In the case of a 1.25 V external reference, the full scale is increased to 2.5 V_{pp} differential. The improved dynamic performance is shown in *Figure 51* and *Figure 52*.

Figure 51. ENOB at REFP = 1.25 V

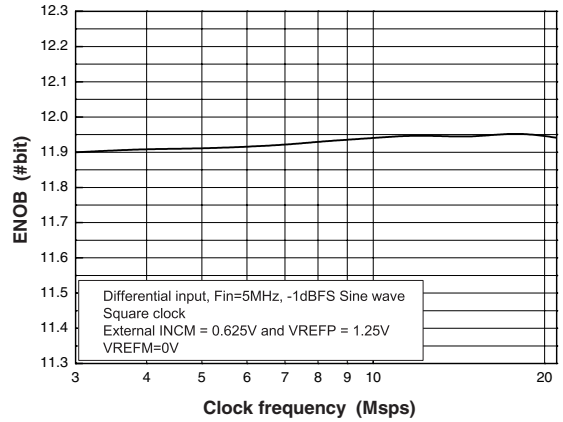
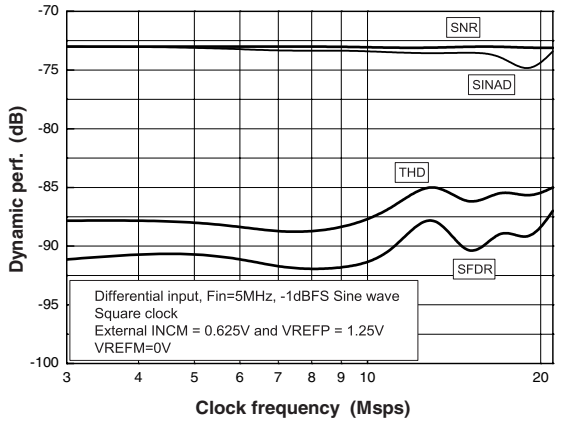


Figure 52. Dynamic performance at REFP = 1.25 V



The magnitude of the analog input common mode should stay close to $V_{REFP}/2$. Higher levels will introduce more distortion.

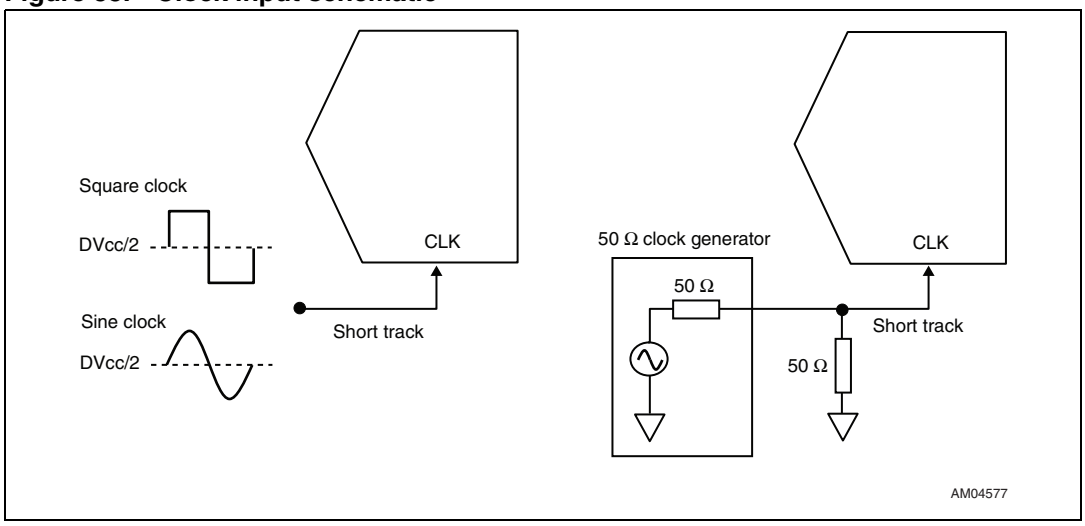
7.4 Clock input

The quality of the converter very much depends on the accuracy of the clock input in terms of jitter. The use of a low jitter crystal-controlled oscillator is recommended.

The following points should also be considered.

- The clock's power supplies must be independent of the ADC's output supplies to avoid digital noise modulation on the output.
- When powered-on, the circuit needs several clock periods to reach its normal operating conditions.

Figure 53. Clock input schematic



The signal applied to the CLK pin is critical to obtain full performance from the RHF1401. Below 10 MHz, the sine clock does not have transition times fast enough to achieve good performances. It is recommended to use a square signal with fast transition times and to place proper termination resistors as close as possible to the device.

The sampling instant is determined by the clock signal's rising edge. The jitter associated with this instant must be as low as possible to avoid SNR degradation on fast moving input signals. To make sure any error is less than 0.5 LSB, the total jitter T_j must satisfy the following condition for a full-scale input signal.

$$T_j < \frac{1}{\pi \cdot F_{in} \cdot 2^{n+1}}$$

For example, the total jitter with a 14-bit resolution for a 10 MHz full-scale input should be no more than 1 picosecond (rms).

In most cases, the clock signal jitter is responsible for noise. Therefore, you must pay attention to the clock signal when fast signals are acquired with a low frequency clock.

7.5 Power consumption optimization

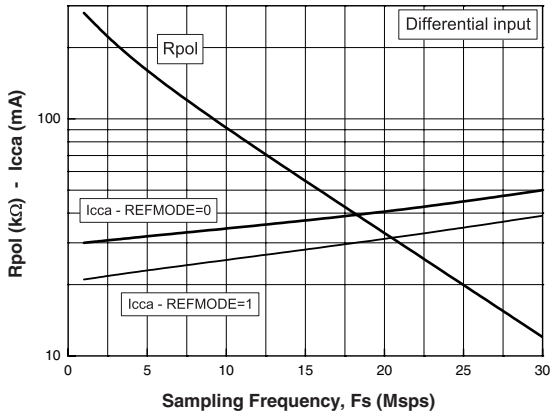
The internal architecture of the RHF1401 makes it possible to optimize the power consumption according to the sampling frequency of the application. For this purpose, an external R_{pol} resistor is placed between the IPOL pin and the analog ground. Therefore, the total dissipation can be adjusted across the entire sampling range to fulfill the requirements of applications where power saving is critical.

For low sampling frequencies, the resistor value may be adjusted to decrease the analog current without any deterioration of the dynamic performance.

The current consumption Icca, depending on the value of R_{pol}, is as shown in *Figure 54* for two different configurations.

- REFMODE = 0
- REFMODE = 1

Figure 54. Analog current consumption vs. F_s according to value of R_{pol}



7.6 PCB layout precautions

- Use of dedicated analog and digital ground planes on the PCB is recommended for high-speed circuit applications to provide low parasitic inductance and resistance. Ground planes under the digital pins and layers should be avoided to minimize parasitic capacitances.
- The separation of the analog signal from clock signal and digital outputs is mandatory to prevent noise from coupling onto the input signal.
- Power supply bypass capacitors must be placed as close as possible to the IC pins to improve high-frequency bypassing and reduce harmonic distortion.
- All leads must be as short as possible, especially for the analog input, so as to decrease parasitic capacitance and inductance.
- To minimize the transition current when the output changes, the capacitive load at the digital outputs must be reduced as much as possible by using the shortest-possible routing tracks.
- Choose the smallest-possible component sizes (SMD).

8 Definitions of specified parameters

8.1 Static parameters

Differential non-linearity (DNL)

The average deviation of any output code width from the ideal code width of 1 LSB.

Integral non-linearity (INL)

An ideal converter exhibits a transfer function that is a straight line from the starting code to the ending code. The INL is the deviation from this ideal line for each transition.

8.2 Dynamic parameters

Spurious free dynamic range (SFDR)

The ratio between the power of the worst spurious signal (not always a harmonic) and the amplitude of the fundamental tone (signal power) over the full Nyquist band. Expressed in dBc.

Total harmonic distortion (THD)

The ratio of the rms sum of the first five harmonic distortion components to the rms value of the fundamental line. Expressed in dB.

Signal to noise ratio (SNR)

The ratio of the rms value of the fundamental component to the rms sum of all other spectral components in the Nyquist band ($F_s/2$) excluding DC, fundamental and the first five harmonics. Reported in dB.

Signal-to-noise and distortion ratio (SINAD)

A similar ratio to the SNR but that includes the harmonic distortion components in the noise figure (not the DC signal). Expressed in dB. From SINAD, the effective number of bits (ENOB) can easily be deduced using the formula:

$$SINAD = 6.02 \times ENOB + 1.76\ dB$$

When the analog input signal is not full-scale (FS) but has an A_0 amplitude, the SINAD expression becomes:

$$SINAD = 6.02 \times ENOB + 1.76\ dB + 20\ log\ (A_0 / FS)$$

Analog input bandwidth

The maximum analog input frequency at which the spectral response of a full power signal is reduced by 3 dB. Higher values can be achieved with smaller input levels.

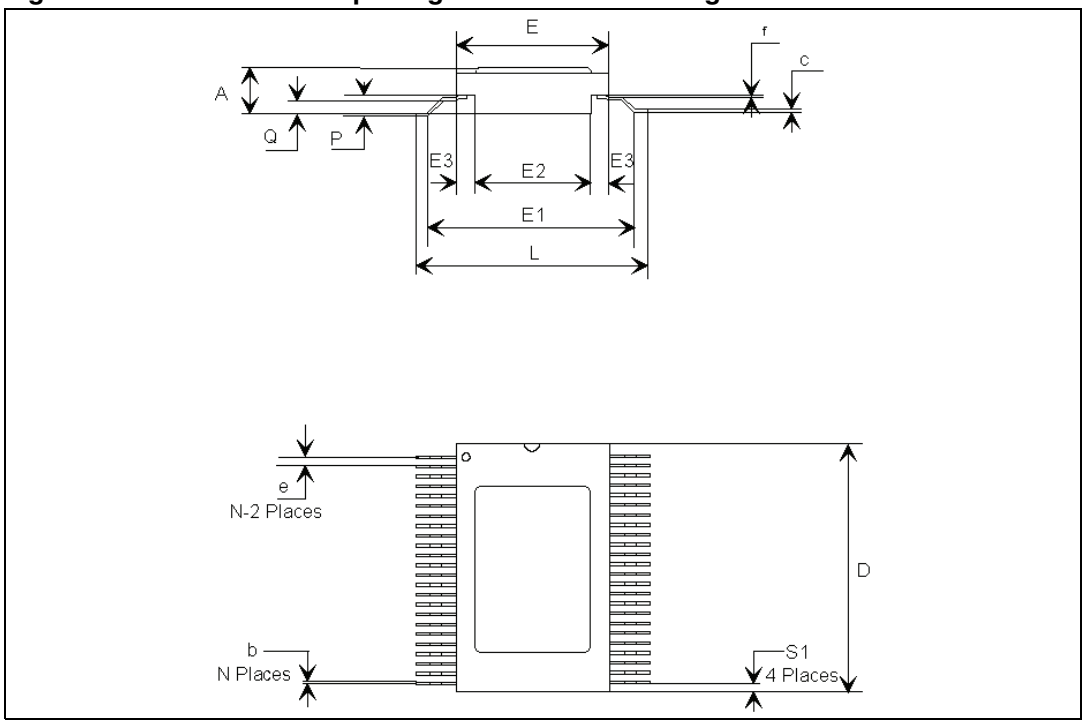
Pipeline delay

The delay between the initial sample of the analog input and the availability of the corresponding digital data output on the output bus. Also called data latency. Expressed as a number of clock cycles.

9 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*.
ECOPACK® is an ST trademark.

Figure 55. Ceramic SO-48 package mechanical drawing



Note: The upper metallic lid is not electrically connected to any pins, nor to the IC die inside the package. Connecting unused pins or metal lid to ground or to the power supply will not affect the electrical characteristics.

Table 13. Ceramic SO-48 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.18	2.47	2.72	0.086	0.097	0.107
b	0.20	0.254	0.30	0.008	0.010	0.012
c	0.12	0.15	0.18	0.005	0.006	0.007
D	15.57	15.75	15.92	0.613	0.620	0.627
E	9.52	9.65	9.78	0.375	0.380	0.385
E1		10.90			0.429	
E2	6.22	6.35	6.48	0.245	0.250	0.255
E3	1.52	1.65	1.78	0.060	0.065	0.070
e		0.635			0.025	
f		0.20			0.008	
L	12.28	12.58	12.88	0.483	0.495	0.507
P	1.30	1.45	1.60	0.051	0.057	0.063
Q	0.66	0.79	0.92	0.026	0.031	0.036
S1	0.25	0.43	0.61	0.010	0.017	0.024

10 Ordering information

Table 14. Order codes

Order code	SMD pin	Quality level	Package	Lead finish	Packing	Marking	EPPL
RHF1401KSO1	-	Engineering model	SO-48	Gold	Strip pack	RHF1401KSO1	-
RHF1401KSO-01V	5962F0626001VXC	QMLV-Flight	SO-48	Gold	Strip pack	5962F0626001VXC	-

Note: Contact your local ST sales office for information regarding the specific conditions for products in die form and QML-Q versions.

11 Revision history

Table 15. Document revision history

Date	Revision	Changes
29-Jun-2007	1	First public release. Failure immune and latchup immune value increased to 120 MeV-cm2/mg. Updated package mechanical information. Removed reference to non rad-hard components from *External references, common mode: on page 16*.
29-Oct-2007	2	Updated *Figure 1: RHF1401 block diagram*. Added explanation on *Figure 3: Timing diagram*. Added introduction to *Section 6: Typical performance characteristics*. Updated *Section 7.2: Clock signal requirements* and *Section 7.3: Power consumption optimization.* Added *Section 7.4: Low sampling rate recommendations.* Updated information on Data Ready signal in *Section 7.5: Digital inputs/outputs*. Added *Figure 24: Impact of clock frequency on RHF1401 performance* and *Figure 25: CLK signal derivation*.
09-Nov-2009	3	Changed input clock features in *Table 9*. Modified *Table 13*. Added *Figure 12* to *Figure 42*.
26-Feb-2010	4	Modified *Figure 1: RHF1401 block diagram*. Added details for Tdr and changed values for Tpd in *Table 2: Timing characteristics*. Modified *Figure 11: Timing diagram*. Changed values for VREFP in *Table 4*. Changed Vin operating conditions in *Table 4*, *Figure 42* and *Figure 43*. Changed values for DNL in *Table 8*.
13-Sep-2010	5	Modified *Figure 1 on page 3* and *Figure 9 on page 7*. Added note *2. on page 8*. Modified C_{IN} typ value in *Table 5: Analog inputs* as per *Figure 3*. Modified *Figure 11: Timing diagram*. Replaced *Figure 20*. Added *Table 12: Output codes for DFSB = 1*. Modified *Figure 44: 2 V_{p-p} differential input*.
29-Jul-2011	6	Added *Note: on page 31* and in the "Pin connections" diagram on the coverpage.