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Kind regards,

Team Nexperia

# PHK28NQ03LT

## N-channel TrenchMOS logic level FET

Rev. 03 — 8 December 2009

Product data sheet

## 1. Product profile

### 1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product is designed and qualified for use in computing, communications, consumer and industrial applications only.

### 1.2 Features and benefits

- Simple gate drive required due to low gate charge
- Suitable for logic level gate drive sources

### 1.3 Applications

- DC-to-DC converters
- Switched-mode power supplies

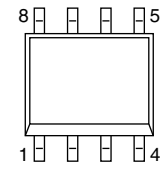
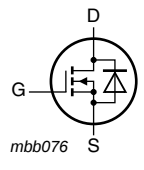
### 1.4 Quick reference data

Table 1. Quick reference

| Symbol                         | Parameter                        | Conditions                                                                                                                          | Min | Typ  | Max  | Unit       |
|--------------------------------|----------------------------------|-------------------------------------------------------------------------------------------------------------------------------------|-----|------|------|------------|
| $V_{DS}$                       | drain-source voltage             | $T_j \geq 25\text{ °C}$ ; $T_j \leq 150\text{ °C}$                                                                                  | -   | -    | 30   | V          |
| $I_D$                          | drain current                    | $T_{sp} = 25\text{ °C}$ ; $V_{GS} = 10\text{ V}$ ;<br>see <a href="#">Figure 1</a> and <a href="#">3</a>                            | -   | -    | 23.7 | A          |
| $P_{tot}$                      | total power dissipation          | $T_{sp} = 25\text{ °C}$ ;<br>see <a href="#">Figure 2</a>                                                                           | -   | -    | 6.25 | W          |
| <b>Dynamic characteristics</b> |                                  |                                                                                                                                     |     |      |      |            |
| $Q_{GD}$                       | gate-drain charge                | $V_{GS} = 4.5\text{ V}$ ; $I_D = 14\text{ A}$ ;<br>$V_{DS} = 15\text{ V}$ ; $T_j = 25\text{ °C}$ ;<br>see <a href="#">Figure 11</a> | -   | 11.4 | -    | nC         |
| <b>Static characteristics</b>  |                                  |                                                                                                                                     |     |      |      |            |
| $R_{DS(on)}$                   | drain-source on-state resistance | $V_{GS} = 10\text{ V}$ ; $I_D = 14\text{ A}$ ;<br>$T_j = 25\text{ °C}$ ; see <a href="#">Figure 9</a> and <a href="#">10</a>        | -   | 5.5  | 6.5  | m $\Omega$ |

## 2. Pinning information

**Table 2.** Pinning information

| Pin | Symbol | Description | Simplified outline                                                                                             | Graphic symbol                                                                      |
|-----|--------|-------------|----------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------|
| 1   | S      | source      |  <p><b>SOT96-1 (SO8)</b></p> |  |
| 2   | S      | source      |                                                                                                                |                                                                                     |
| 3   | S      | source      |                                                                                                                |                                                                                     |
| 4   | G      | gate        |                                                                                                                |                                                                                     |
| 5   | D      | drain       |                                                                                                                |                                                                                     |
| 6   | D      | drain       |                                                                                                                |                                                                                     |
| 7   | D      | drain       |                                                                                                                |                                                                                     |
| 8   | D      | drain       |                                                                                                                |                                                                                     |

## 3. Ordering information

**Table 3.** Ordering information

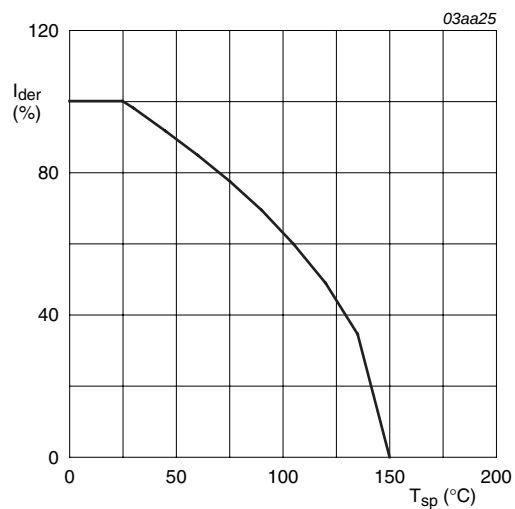
| Type number | Package |                                                           | Version |
|-------------|---------|-----------------------------------------------------------|---------|
|             | Name    | Description                                               |         |
| PHK28NQ03LT | SO8     | plastic small outline package; 8 leads; body width 3.9 mm | SOT96-1 |

## 4. Limiting values

**Table 4.** Limiting values

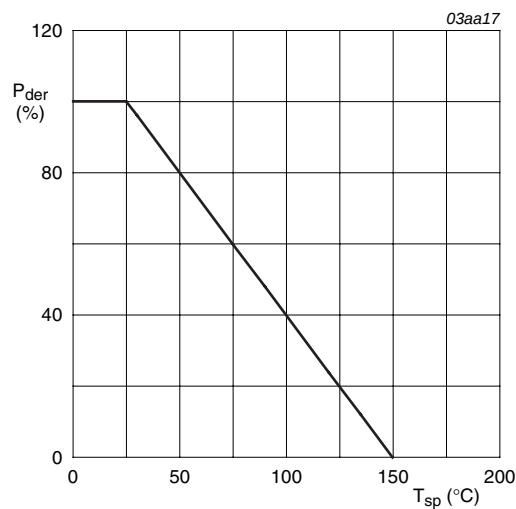
In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol                    | Parameter               | Conditions                                                                                            | Min | Max  | Unit |
|---------------------------|-------------------------|-------------------------------------------------------------------------------------------------------|-----|------|------|
| $V_{DS}$                  | drain-source voltage    | $T_j \geq 25\text{ °C}$ ; $T_j \leq 150\text{ °C}$                                                    | -   | 30   | V    |
| $V_{DGR}$                 | drain-gate voltage      | $T_j \leq 150\text{ °C}$ ; $T_j \geq 25\text{ °C}$ ; $R_{GS} = 20\text{ k}\Omega$                     | -   | 30   | V    |
| $V_{GS}$                  | gate-source voltage     |                                                                                                       | -   | 20   | V    |
| $I_D$                     | limiting drain current  | $T_{sp} = 100\text{ °C}$ ; $V_{GS} = 10\text{ V}$ ; see <a href="#">Figure 1</a>                      | -   | 15   | A    |
|                           | drain current           | $T_{sp} = 25\text{ °C}$ ; $V_{GS} = 10\text{ V}$ ; see <a href="#">Figure 1</a> and <a href="#">3</a> | -   | 23.7 | A    |
| $I_{DM}$                  | peak drain current      | $T_{sp} = 25\text{ °C}$ ; $t_p \leq 10\text{ }\mu\text{s}$ ; pulsed; see <a href="#">Figure 3</a>     | -   | 60   | A    |
| $P_{tot}$                 | total power dissipation | $T_{sp} = 25\text{ °C}$ ; see <a href="#">Figure 2</a>                                                | -   | 6.25 | W    |
| $T_{stg}$                 | storage temperature     |                                                                                                       | -55 | 150  | °C   |
| $T_j$                     | junction temperature    |                                                                                                       | -55 | 150  | °C   |
| <b>Source-drain diode</b> |                         |                                                                                                       |     |      |      |
| $I_S$                     | source current          | $T_{sp} = 25\text{ °C}$                                                                               | -   | 5.2  | A    |
| $I_{SM}$                  | peak source current     | $T_{sp} = 25\text{ °C}$ ; $t_p \leq 10\text{ }\mu\text{s}$ ; pulsed                                   | -   | 20.8 | A    |



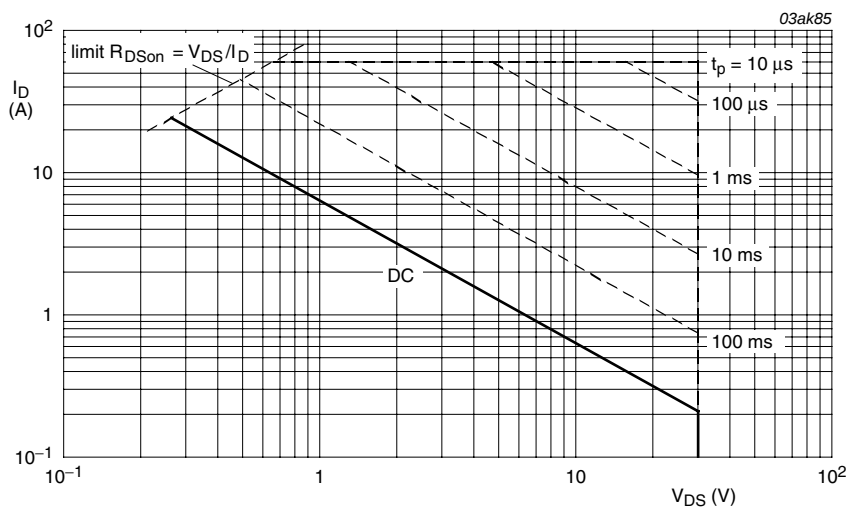
$$I_{der} = \frac{I_D}{I_{D(25^\circ\text{C})}} \times 100\%$$

**Fig 1. Normalized continuous drain current as a function of solder point temperature**



$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ\text{C})}} \times 100\%$$

**Fig 2. Normalized total power dissipation as a function of solder point temperature**



$T_{sp} = 25^\circ\text{C}$ ;  $I_{DM}$  is single pulse;  $V_{GS} = 10\text{V}$

**Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage**

5. Thermal characteristics

Table 5. Thermal characteristics

| Symbol         | Parameter                                        | Conditions                   | Min | Typ | Max | Unit |
|----------------|--------------------------------------------------|------------------------------|-----|-----|-----|------|
| $R_{th(j-sp)}$ | thermal resistance from junction to solder point | see <a href="#">Figure 4</a> | -   | -   | 20  | K/W  |

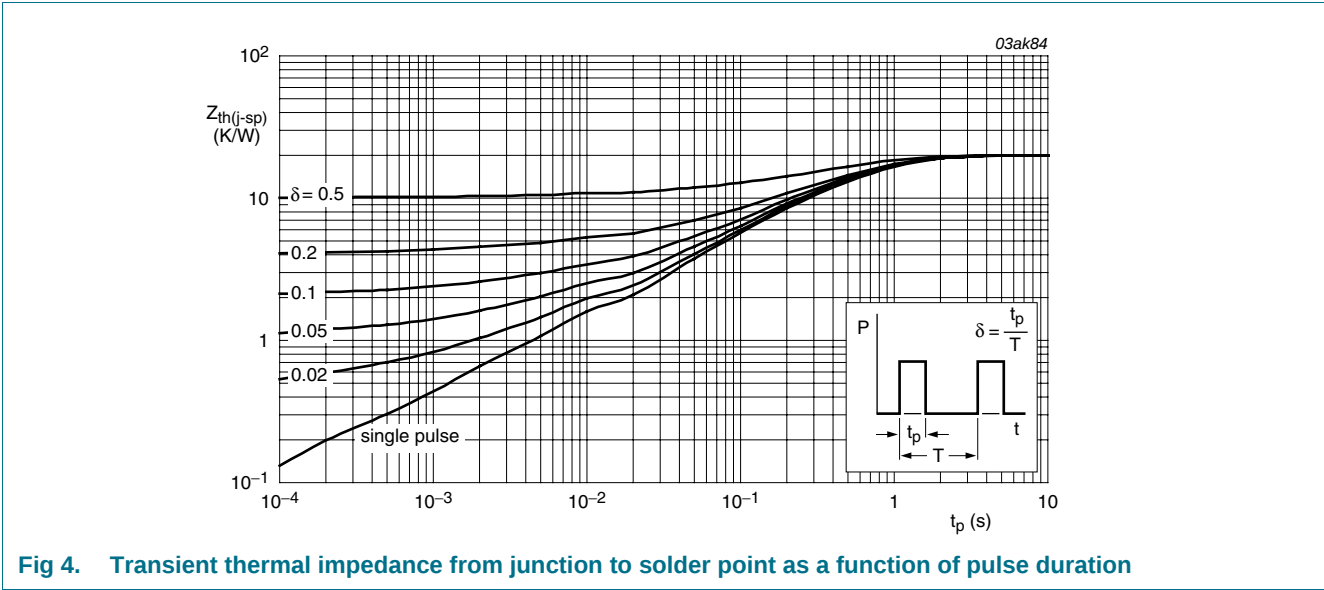
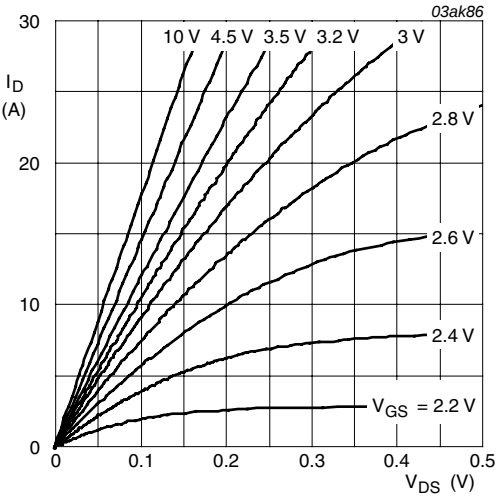


Fig 4. Transient thermal impedance from junction to solder point as a function of pulse duration

## 6. Characteristics

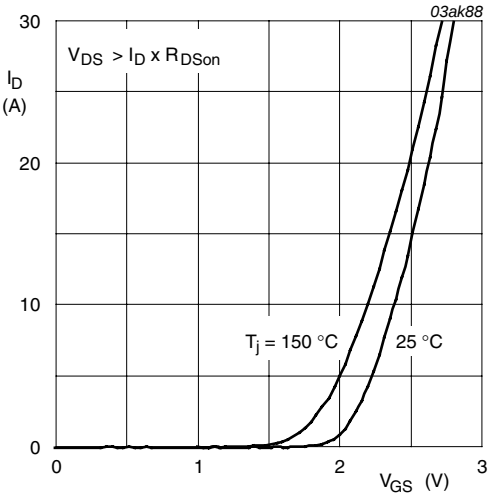
**Table 6. Characteristics**

| Symbol                  | Parameter                        | Conditions                                                                                                                    | Min | Typ  | Max  | Unit |
|-------------------------|----------------------------------|-------------------------------------------------------------------------------------------------------------------------------|-----|------|------|------|
| Static characteristics  |                                  |                                                                                                                               |     |      |      |      |
| V <sub>(BR)DSS</sub>    | drain-source breakdown voltage   | I <sub>D</sub> = 250 μA; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C                                                        | 30  | -    | -    | V    |
|                         |                                  | I <sub>D</sub> = 250 μA; V <sub>GS</sub> = 0 V; T <sub>j</sub> = -55 °C                                                       | 27  | -    | -    | V    |
| V <sub>GS(th)</sub>     | gate-source threshold voltage    | I <sub>D</sub> = 1 mA; V <sub>DS</sub> = V <sub>GS</sub> ; T <sub>j</sub> = 150 °C; see <a href="#">Figure 8</a>              | 0.6 | -    | -    | V    |
|                         |                                  | I <sub>D</sub> = 1 mA; V <sub>DS</sub> = V <sub>GS</sub> ; T <sub>j</sub> = -55 °C; see <a href="#">Figure 8</a>              | -   | -    | 2.2  | V    |
|                         |                                  | I <sub>D</sub> = 1 mA; V <sub>DS</sub> = V <sub>GS</sub> ; T <sub>j</sub> = 25 °C; see <a href="#">Figure 8</a>               | 1   | 1.5  | 2    | V    |
| I <sub>DSS</sub>        | drain leakage current            | V <sub>DS</sub> = 30 V; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 150 °C                                                        | -   | -    | 500  | μA   |
|                         |                                  | V <sub>DS</sub> = 30 V; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C                                                         | -   | 0.05 | 1    | μA   |
| I <sub>GSS</sub>        | gate leakage current             | V <sub>GS</sub> = 16 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C                                                         | -   | 10   | 100  | nA   |
|                         |                                  | V <sub>GS</sub> = -16 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C                                                        | -   | 10   | 100  | nA   |
| R <sub>DSon</sub>       | drain-source on-state resistance | V <sub>GS</sub> = 4.5 V; I <sub>D</sub> = 13 A; T <sub>j</sub> = 150 °C; see <a href="#">Figure 9</a> and <a href="#">10</a>  | -   | 11.2 | 13.1 | mΩ   |
|                         |                                  | V <sub>GS</sub> = 10 V; I <sub>D</sub> = 14 A; T <sub>j</sub> = 25 °C; see <a href="#">Figure 9</a> and <a href="#">10</a>    | -   | 5.5  | 6.5  | mΩ   |
|                         |                                  | V <sub>GS</sub> = 4.5 V; I <sub>D</sub> = 13 A; T <sub>j</sub> = 25 °C; see <a href="#">Figure 9</a> and <a href="#">10</a>   | -   | 6.6  | 7.7  | mΩ   |
| Dynamic characteristics |                                  |                                                                                                                               |     |      |      |      |
| Q <sub>G(tot)</sub>     | total gate charge                | I <sub>D</sub> = 14 A; V <sub>DS</sub> = 15 V; V <sub>GS</sub> = 4.5 V; T <sub>j</sub> = 25 °C; see <a href="#">Figure 11</a> | -   | 30.3 | -    | nC   |
| Q <sub>GS</sub>         | gate-source charge               |                                                                                                                               | -   | 7.8  | -    | nC   |
| Q <sub>GD</sub>         | gate-drain charge                |                                                                                                                               | -   | 11.4 | -    | nC   |
| C <sub>iss</sub>        | input capacitance                | V <sub>DS</sub> = 20 V; V <sub>GS</sub> = 0 V; f = 1 MHz; T <sub>j</sub> = 25 °C; see <a href="#">Figure 12</a>               | -   | 2800 | -    | pF   |
| C <sub>oss</sub>        | output capacitance               |                                                                                                                               | -   | 670  | -    | pF   |
| C <sub>rss</sub>        | reverse transfer capacitance     |                                                                                                                               | -   | 320  | -    | pF   |
| t <sub>d(on)</sub>      | turn-on delay time               | V <sub>DS</sub> = 15 V; R <sub>L</sub> = 15 Ω; V <sub>GS</sub> = 10 V; R <sub>G(ext)</sub> = 6 Ω; T <sub>j</sub> = 25 °C      | -   | 11   | -    | ns   |
| t <sub>r</sub>          | rise time                        |                                                                                                                               | -   | 10   | -    | ns   |
| t <sub>d(off)</sub>     | turn-off delay time              |                                                                                                                               | -   | 80   | -    | ns   |
| t <sub>f</sub>          | fall time                        |                                                                                                                               | -   | 40   | -    | ns   |
| Source-drain diode      |                                  |                                                                                                                               |     |      |      |      |
| V <sub>SD</sub>         | source-drain voltage             | I <sub>S</sub> = 2.3 A; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C; see <a href="#">Figure 13</a>                          | -   | 0.72 | 1.2  | V    |



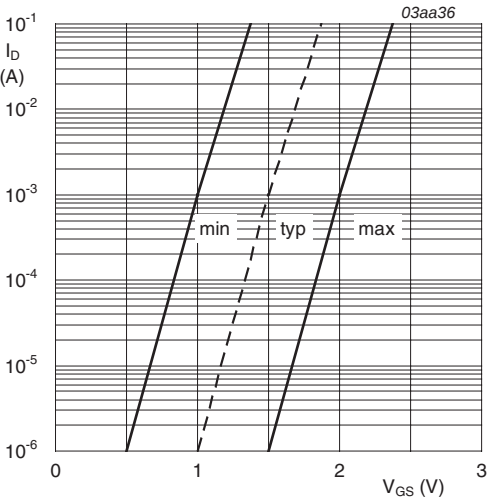
$T_j = 25^{\circ}\text{C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values



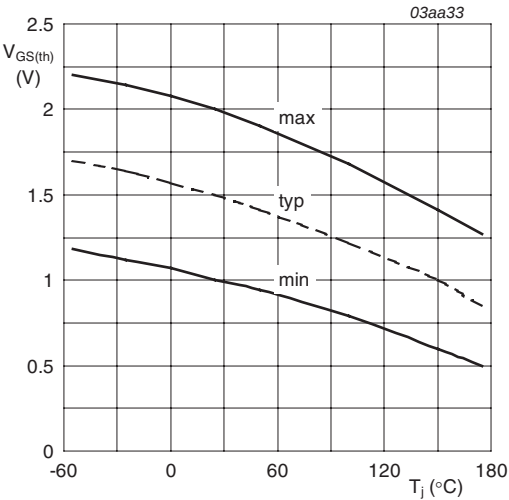
$T_j = 25^{\circ}\text{C}$  and  $150^{\circ}\text{C}$ ;  $V_{DS} > I_D \times R_{DSon}$

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values



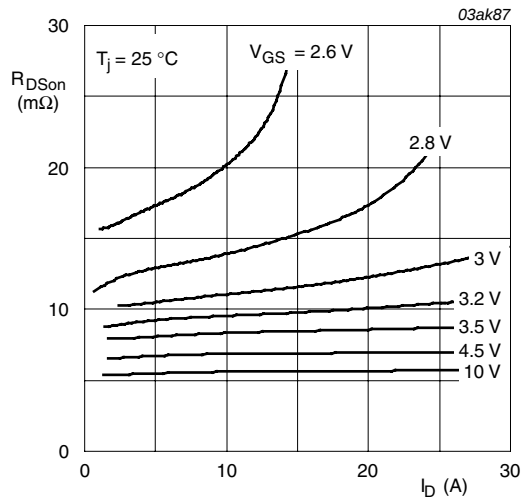
$T_j = 25^{\circ}\text{C}$ ;  $V_{DS} = V_{GS}$

Fig 7. Sub-threshold drain current as a function of gate-source voltage



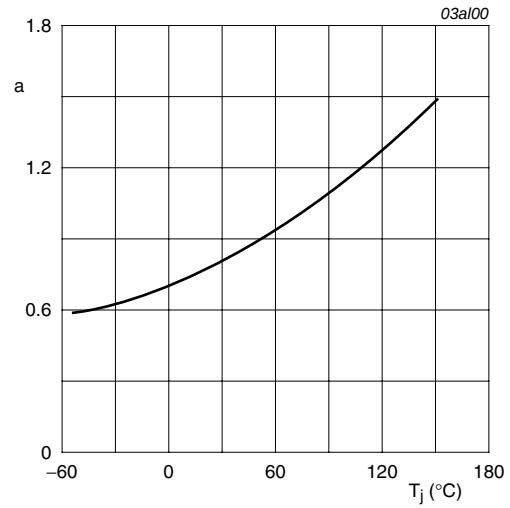
$I_D = 1\text{ mA}$ ;  $V_{DS} = V_{GS}$

Fig 8. Gate-source threshold voltage as a function of junction temperature



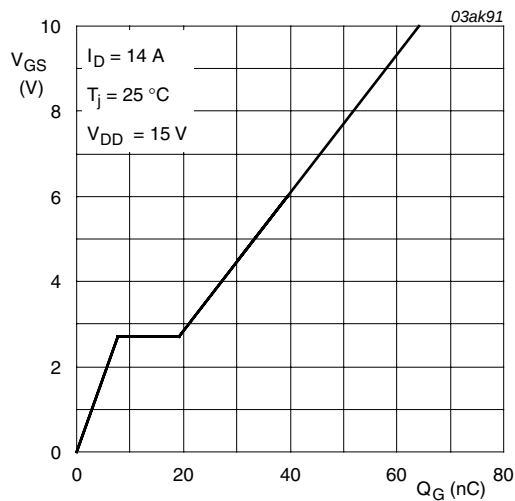
$T_j = 25\text{ °C}$

**Fig 9.** Drain-source on-state resistance as a function of drain current; typical values



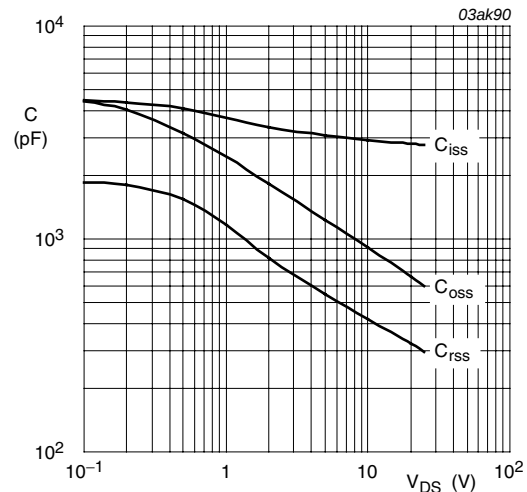
$$a = \frac{R_{DS(on)}}{R_{DS(on)(25\text{ °C})}}$$

**Fig 10.** Normalized drain-source on-state resistance factor as a function of junction temperature



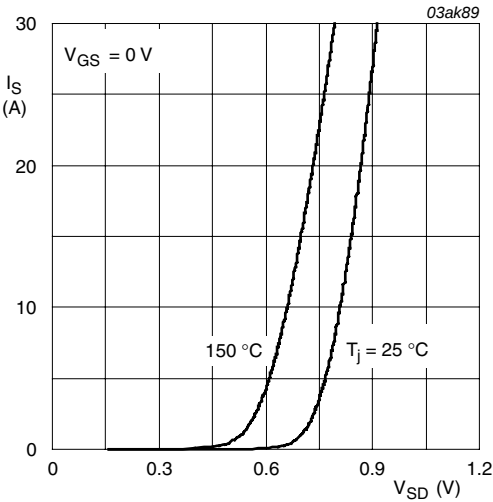
$I_D = 14\text{ A}; V_{DD} = 15\text{ V}$

**Fig 11.** Gate-source voltage as a function of gate charge; typical values



$V_{GS} = 0\text{ V}; f = 1\text{ MHz}$

**Fig 12.** Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$T_j = 25^\circ\text{C}$  and  $150^\circ\text{C}$ ;  $V_{GS} = 0\text{ V}$

Fig 13. Source current as a function of source-drain voltage; typical values

7. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm

SOT96-1

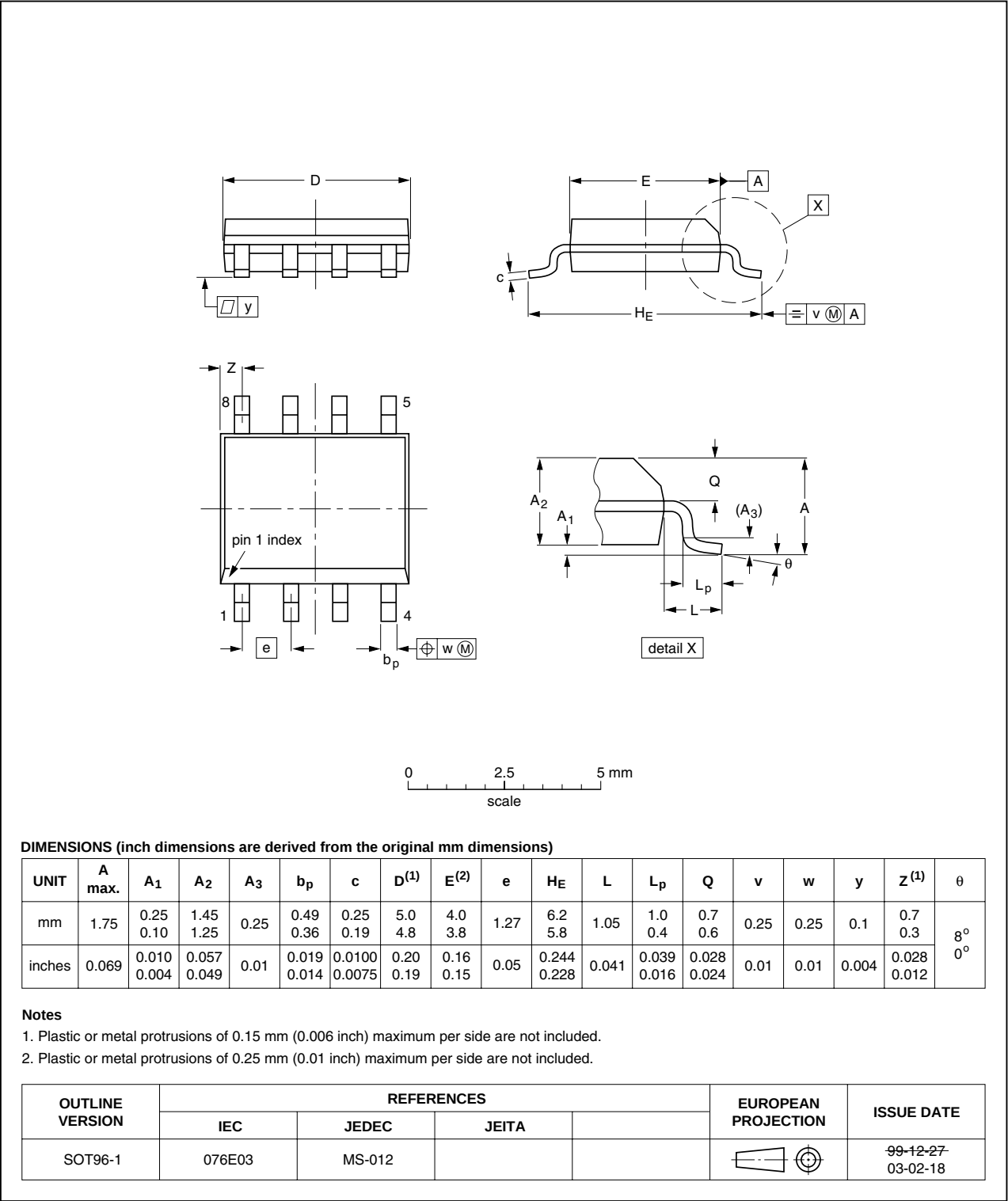


Fig 14. Package outline SOT96-1 (SO8)

## 8. Revision history

Table 7. Revision history

| Document ID                        | Release date                                                                                                                                                                                                                                         | Data sheet status  | Change notice | Supersedes     |
|------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------|---------------|----------------|
| PHK28NQ03LT_3                      | 20091208                                                                                                                                                                                                                                             | Product data sheet | -             | PHK28NQ03LT-02 |
| Modifications:                     | <ul style="list-style-type: none"><li>The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li><li>Legal texts have been adapted to the new company name where appropriate.</li></ul> |                    |               |                |
| PHK28NQ03LT-02<br>(9397 750 11367) | 20030410                                                                                                                                                                                                                                             | Product data       | -             | PHK28NQ03LT-01 |
| PHK28NQ03LT-01<br>(9397 750 10743) | 20021212                                                                                                                                                                                                                                             | Product data       | -             | -              |

## 9. Legal information

### 9.1 Data sheet status

| Document status <sup>[1][2]</sup> | Product status <sup>[3]</sup> | Definition                                                                            |
|-----------------------------------|-------------------------------|---------------------------------------------------------------------------------------|
| Objective [short] data sheet      | Development                   | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet    | Qualification                 | This document contains data from the preliminary specification.                       |
| Product [short] data sheet        | Production                    | This document contains the product specification.                                     |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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## 10. Contact information

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